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Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I ² C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 13x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f128d-50i-ml |

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

| Pin Name | Pin Number ⁽¹⁾ | | | | Pin Type | Buffer Type | Description |
|----------|---------------------------|--------------------------|-------------------|------------------------|----------|-------------|---|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| USBID | 11 ⁽³⁾ | 14 ⁽³⁾ | 15 ⁽³⁾ | 41 ⁽³⁾ | I | ST | USB OTG ID detect |
| CTED1 | 27 | 2 | 33 | 19 | I | ST | CTMU External Edge Input |
| CTED2 | 28 | 3 | 34 | 20 | I | ST | |
| CTED3 | 13 | 16 | 17 | 43 | I | ST | |
| CTED4 | 15 | 18 | 19 | 1 | I | ST | |
| CTED5 | 22 | 25 | 28 | 14 | I | ST | |
| CTED6 | 23 | 26 | 29 | 15 | I | ST | |
| CTED7 | — | — | 20 | 5 | I | ST | |
| CTED8 | — | — | — | 13 | I | ST | |
| CTED9 | 9 | 12 | 10 | 34 | I | ST | |
| CTED10 | 14 | 17 | 18 | 44 | I | ST | |
| CTED11 | 18 | 21 | 24 | 8 | I | ST | |
| CTED12 | 2 | 5 | 36 | 22 | I | ST | |
| CTED13 | 3 | 6 | 1 | 23 | I | ST | |
| CTPLS | 21 | 24 | 27 | 11 | O | — | CTMU Pulse Output |
| PGED1 | 1 | 4 | 35 | 21 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 1 |
| PGEC1 | 2 | 5 | 36 | 22 | I | ST | Clock input pin for Programming/Debugging Communication Channel 1 |
| PGED2 | 18 | 21 | 24 | 8 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 2 |
| PGEC2 | 19 | 22 | 25 | 9 | I | ST | Clock input pin for Programming/Debugging Communication Channel 2 |
| PGED3 | 11 ⁽²⁾ | 14 ⁽²⁾ | 15 ⁽²⁾ | 41 ⁽²⁾ | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 3 |
| | 27 ⁽³⁾ | 2 ⁽³⁾ | 33 ⁽³⁾ | 19 ⁽³⁾ | | | |
| PGEC3 | 12 ⁽²⁾ | 15 ⁽²⁾ | 16 ⁽²⁾ | 42 ⁽²⁾ | I | ST | Clock input pin for Programming/Debugging Communication Channel 3 |
| | 28 ⁽³⁾ | 3 ⁽³⁾ | 34 ⁽³⁾ | 20 ⁽³⁾ | | | |
| PGED4 | — | — | 3 | 12 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 4 |
| PGEC4 | — | — | 4 | 13 | I | ST | Clock input pin for Programming/Debugging Communication Channel 4 |

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input
— = N/A

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

2.9 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-5 and Figure 2-6.

FIGURE 2-5: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION

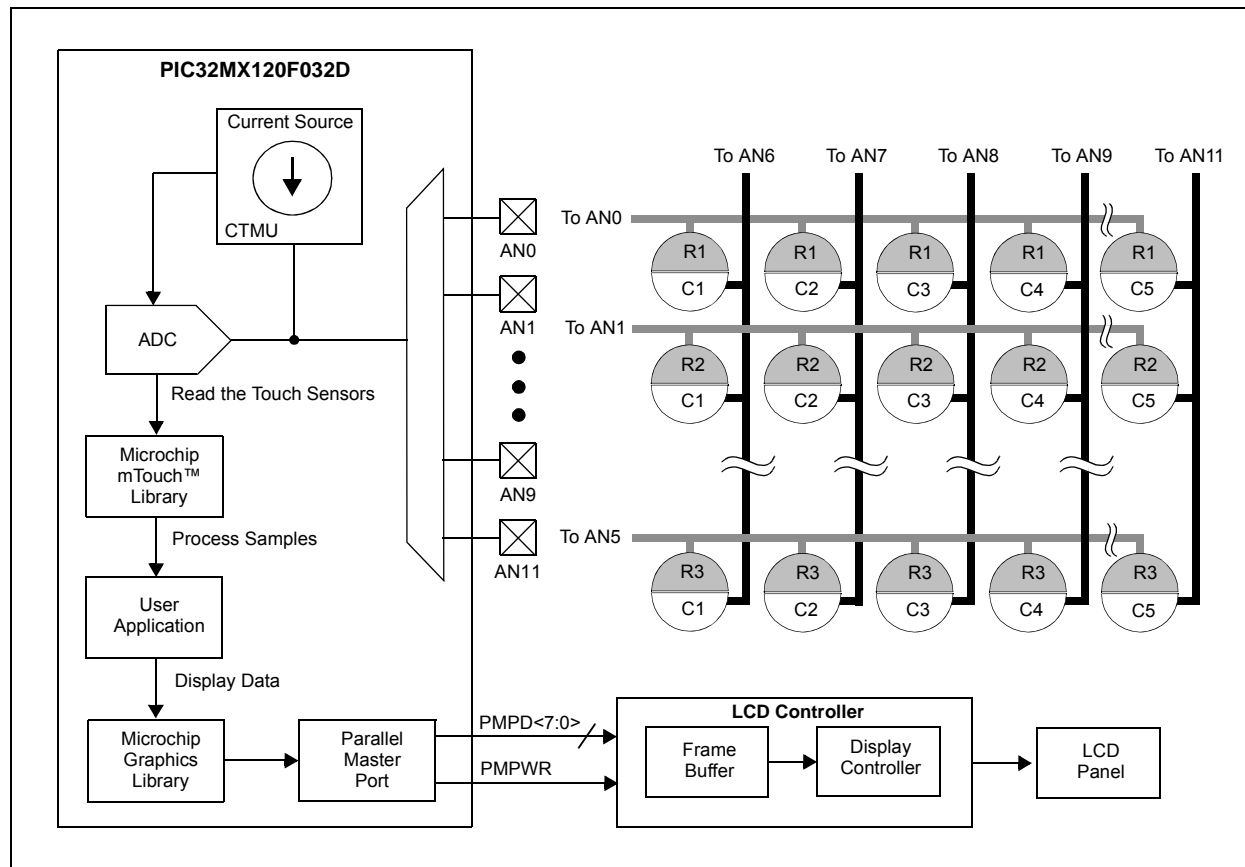
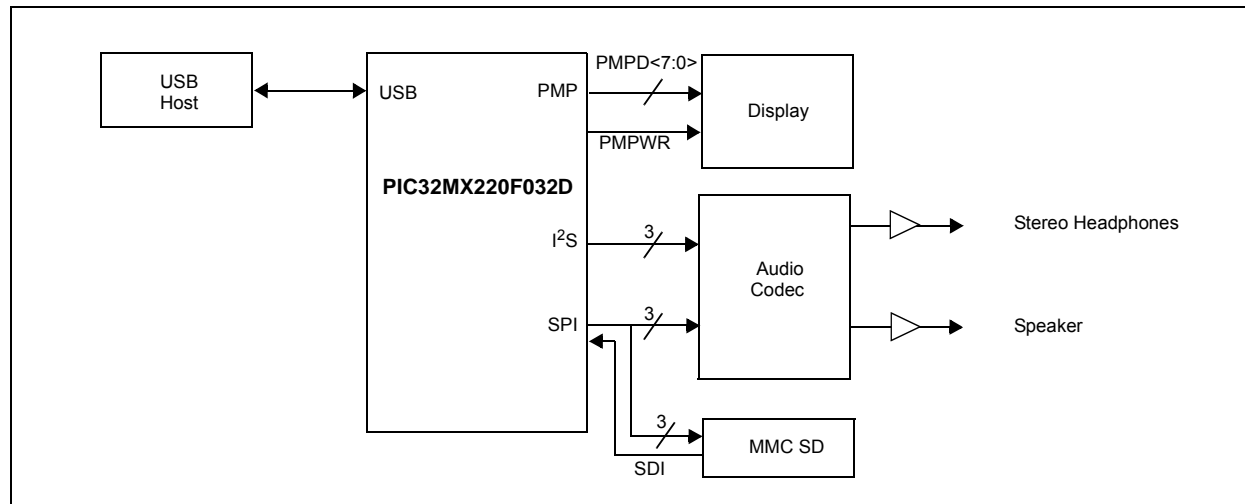


FIGURE 2-6: AUDIO PLAYBACK APPLICATION



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS31 | IFS30 | IFS29 | IFS28 | IFS27 | IFS26 | IFS25 | IFS24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS23 | IFS22 | IFS21 | IFS20 | IFS19 | IFS18 | IFS17 | IFS16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS15 | IFS14 | IFS13 | IFS12 | IFS11 | IFS10 | IFS09 | IFS08 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS07 | IFS06 | IFS05 | IFS04 | IFS03 | IFS02 | IFS01 | IFS00 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IFS31-IFS00:** Interrupt Flag Status bits

1 = Interrupt request has occurred

0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC31 | IEC30 | IEC29 | IEC28 | IEC27 | IEC26 | IEC25 | IEC24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC23 | IEC22 | IEC21 | IEC20 | IEC19 | IEC18 | IEC17 | IEC16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC15 | IEC14 | IEC13 | IEC12 | IEC11 | IEC10 | IEC09 | IEC08 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC07 | IEC06 | IEC05 | IEC04 | IEC03 | IEC02 | IEC01 | IEC00 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IEC31-IEC00:** Interrupt Enable bits

1 = Interrupt is enabled

0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 — | U-0 — | U-0 — | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IP03<2:0> | | | | | | IS03<1:0> | |
| 23:16 | U-0 — | U-0 — | U-0 — | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IP02<2:0> | | | | | | IS02<1:0> | |
| 15:8 | U-0 — | U-0 — | U-0 — | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IP01<2:0> | | | | | | IS01<1:0> | |
| 7:0 | U-0 — | U-0 — | U-0 — | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IP00<2:0> | | | | | | IS00<1:0> | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP03<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

.

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS03<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP02<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

.

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS02<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP01<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

.

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending
- bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending
- bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending
- bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending
- bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected (either the source or the destination address is invalid)
0 = No interrupt is pending

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-12: U1ADDR: USB ADDRESS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | LSPDEN | DEVADDR<6:0> | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit

1 = Next token command to be executed at Low-Speed

0 = Next token command to be executed at Full-Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 10-13: U1FRML: USB FRAME NUMBER LOW REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FRML<7:0> | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-16: U1SOF: USB SOF THRESHOLD REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CNT<7:0> | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:

01001010 = 64-byte packet

00101010 = 32-byte packet

00011010 = 16-byte packet

00010010 = 8-byte packet

REGISTER 10-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| | BDTPTRL<15:9> | | | | | | | — |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** Buffer Descriptor Table Base Address bits

This 7-bit value provides address bits 15 through 9 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'

11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable port number.

11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin.

Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

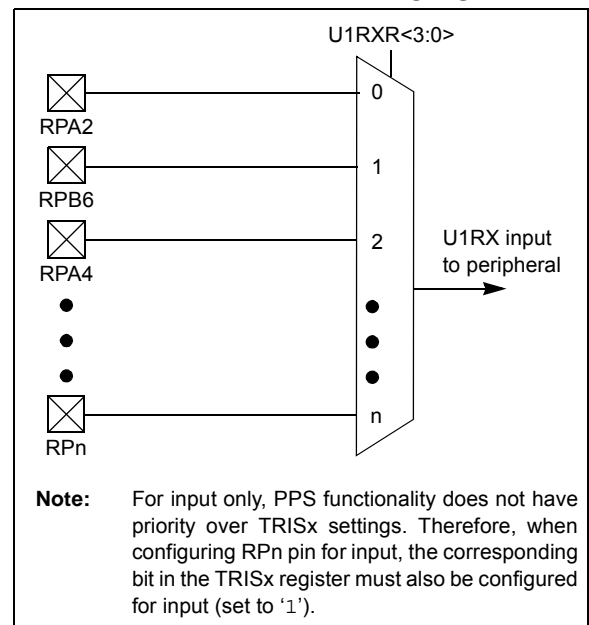
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [pin name]R registers, where [pin name] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 11-2: OUTPUT PIN SELECTION

| RPn Port Pin | RPnR SFR | RPnR bits | RPnR Value to Peripheral Selection |
|--------------|----------|-------------|--|
| RPA0 | RPA0R | RPA0R<3:0> | 0000 = No Connect 0001 = U1TX 0010 = U2RTS 0011 = SS1 0100 = Reserved 0101 = OC1 0110 = Reserved 0111 = C2OUT 1000 = Reserved . . 1111 = Reserved |
| RPB3 | RPB3R | RPB3R<3:0> | |
| RPB4 | RPB4R | RPB4R<3:0> | |
| RPB15 | RPB15R | RPB15R<3:0> | |
| RPB7 | RPB7R | RPB7R<3:0> | |
| RPC7 | RPC7R | RPC7R<3:0> | |
| RPC0 | RPC0R | RPC0R<3:0> | |
| RPC5 | RPC5R | RPC5R<3:0> | |
| RPA1 | RPA1R | RPA1R<3:0> | 0000 = No Connect 0001 = Reserved 0010 = Reserved 0011 = SDO1 0100 = SDO2 0101 = OC2 0110 = Reserved 0111 = C3OUT . . . 1111 = Reserved |
| RPB5 | RPB5R | RPB5R<3:0> | |
| RPB1 | RPB1R | RPB1R<3:0> | |
| RPB11 | RPB11R | RPB11R<3:0> | |
| RPB8 | RPB8R | RPB8R<3:0> | |
| RPA8 | RPA8R | RPA8R<3:0> | |
| RPC8 | RPC8R | RPC8R<3:0> | |
| RPA9 | RPA9R | RPA9R<3:0> | |
| RPA2 | RPA2R | RPA2R<3:0> | 0000 = No Connect 0001 = Reserved 0010 = Reserved 0011 = SDO1 0100 = SDO2 0101 = OC4 0110 = OC5 0111 = REFCLKO 1000 = Reserved . . . 1111 = Reserved |
| RPB6 | RPB6R | RPB6R<3:0> | |
| RPA4 | RPA4R | RPA4R<3:0> | |
| RPB13 | RPB13R | RPB13R<3:0> | |
| RPB2 | RPB2R | RPB2R<3:0> | |
| RPC6 | RPC6R | RPC6R<3:0> | |
| RPC1 | RPC1R | RPC1R<3:0> | |
| RPC3 | RPC3R | RPC3R<3:0> | |
| RPA3 | RPA3R | RPA3R<3:0> | 0000 = No Connect 0001 = U1RTS 0010 = U2TX 0011 = Reserved 0100 = SS2 0101 = OC3 0110 = Reserved 0111 = C1OUT 1000 = Reserved . . . 1111 = Reserved |
| RPB14 | RPB14R | RPB14R<3:0> | |
| RPB0 | RPB0R | RPB0R<3:0> | |
| RPB10 | RPB10R | RPB10R<3:0> | |
| RPB9 | RPB9R | RPB9R<3:0> | |
| RPC9 | RPC9R | RPC9R<3:0> | |
| RPC2 | RPC2R | RPC2R<3:0> | |
| RPC4 | RPC4R | RPC4R<3:0> | |

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

12.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “Timers”** (DS60001105), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (Sosc) for Real-Time Clock (RTC) applications.

The following modes are supported:

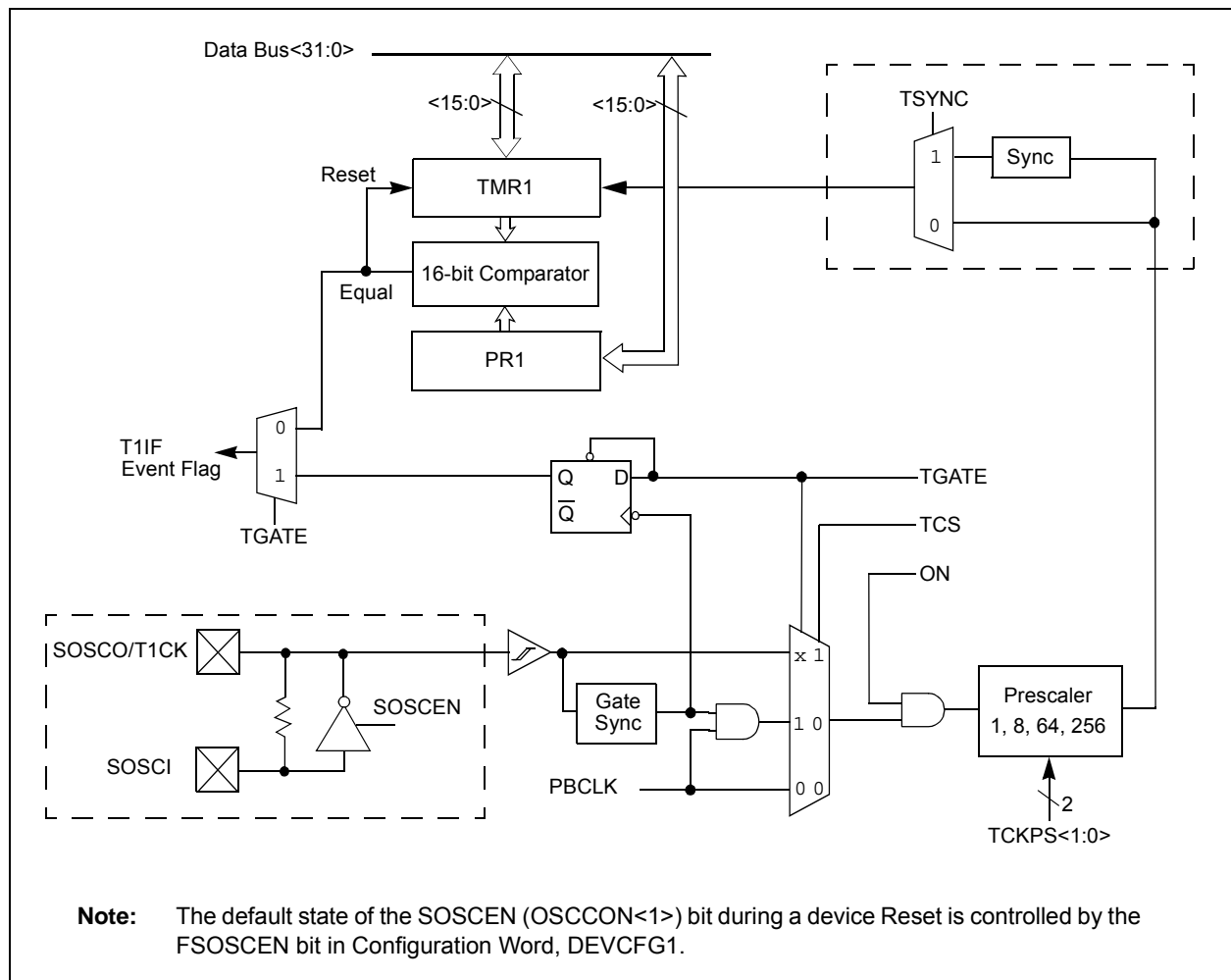
- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

12.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)

Figure 12-1 illustrates a general block diagram of Timer1.

FIGURE 12-1: TIMER1 BLOCK DIAGRAM



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|---------------------------------|-----------------------------|-----------------|-----------------|------------------|-----------------|----------------|--------------------------------|
| 31:24 | R/W-0 FRMEN | R/W-0 FRMSYNC | R/W-0 FRMPOL | R/W-0 MSSEN | R/W-0 FRMSYPW | FRMCNT<2:0> | | |
| 23:16 | R/W-0 MCLKSEL ⁽²⁾ | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | R/W-0 SPIFE | R/W-0 ENHBUF ⁽²⁾ |
| 15:8 | R/W-0 ON ⁽¹⁾ | U-0 — | R/W-0 SIDL | R/W-0 DISSDO | R/W-0 MODE32 | R/W-0 MODE16 | R/W-0 SMP | R/W-0 CKE ⁽³⁾ |
| 7:0 | R/W-0 SSEN | R/W-0 CKP ⁽⁴⁾ | R/W-0 MSTEN | R/W-0 DISSDI | STXISEL<1:0> | | SRXISEL<1:0> | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled (\overline{SSx} pin used as FSYNC input/output)
0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on \overline{SSx} pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)
- bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low
- bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The \overline{SS} pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.
- bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in FRAMED_SYNC mode.
111 = Reserved; do not use
110 = Reserved; do not use
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character
- bit 23 **MCLKSEL:** Master Clock Enable bit⁽²⁾
1 = REFCLK is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator
- bit 22-18 **Unimplemented:** Read as '0'

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLOCK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit can only be written when the ON bit = 0.
- 3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 20-4: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | PTEN14 | — | — | — | PTEN<10:8> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTEN<7:0> | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 15-14 **PTEN14:** PMCS1 Address Port Enable bits

1 = PMA14 functions as either PMA14 or PMCS1⁽¹⁾

0 = PMA14 functions as port I/O

bit 13-11 **Unimplemented:** Read as '0'

bit 10-2 **PTEN<10:2>:** PMP Address Port Enable bits

1 = PMA<10:2> function as PMP address lines

0 = PMA<10:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits

1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL⁽²⁾

0 = PMA1 and PMA0 pads functions as port I/O

Note 1: The use of this pin as PMA14 or CS1 is selected by the CSF<1:0> bits in the PMCON register.

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by bits ADRMUX<1:0> in the PMCON register.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | — | — | — | MONTH10 | MONTH01<3:0> | | | |
| 15:8 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | — | — | DAY10<1:0> | | DAY01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x |
| | — | — | — | — | — | WDAY01<2:0> | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MONTH10:** Binary Coded Decimal value of months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAY10<1:0>:** Binary Coded Decimal value of days bits, 10s place digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY01<2:0>:** Binary Coded Decimal value of weekdays bits; contains a value from 0 to 6

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

26.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

Note 1: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a Posc of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.

- 2: Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from Posc to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to Posc, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

26.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P |
| | — | — | — | — | — | — | FWDTWINSZ<1:0> | |
| 23:16 | R/P | R/P | r-1 | R/P | R/P | R/P | R/P | R/P |
| | FWDTEN | WINDIS | — | WDTPS<4:0> | | | | |
| 15:8 | R/P | R/P | R/P | R/P | r-1 | R/P | R/P | R/P |
| | FCKSM<1:0> | | FPBDIV<1:0> | | — | OSCIOFNC | POSCMOD<1:0> | |
| 7:0 | R/P | r-1 | R/P | r-1 | r-1 | R/P | R/P | R/P |
| | IESO | — | FSOSCEN | — | — | FNOSC<2:0> | | |

| | | |
|-------------------|------------------|--|
| Legend: | r = Reserved bit | P = Programmable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits

11 = Window size is 25%
 10 = Window size is 37.5%
 01 = Window size is 50%
 00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit

1 = Watchdog Timer is enabled and cannot be disabled by software
 0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit

1 = Watchdog Timer is in non-Window mode
 0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576
 10011 = 1:524288
 10010 = 1:262144
 10001 = 1:131072
 10000 = 1:65536
 01111 = 1:32768
 01110 = 1:16384
 01101 = 1:8192
 01100 = 1:4096
 01011 = 1:2048
 01010 = 1:1024
 01001 = 1:512
 01000 = 1:256
 00111 = 1:128
 00110 = 1:64
 00101 = 1:32
 00100 = 1:16
 00011 = 1:8
 00010 = 1:4
 00001 = 1:2
 00000 = 1:1
 All other combinations not shown result in operation = 10100

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-41: CTMU CURRENT SOURCE SPECIFICATIONS

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 3): 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp | | | | |
|----------------------------|--------|--|--|-------|------|-------|--|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
| CTMU CURRENT SOURCE | | | | | | | |
| CTMUI1 | IOUT1 | Base Range ⁽¹⁾ | — | 0.55 | — | μA | CTMUCON<9:8> = 01 |
| CTMUI2 | IOUT2 | 10x Range ⁽¹⁾ | — | 5.5 | — | μA | CTMUCON<9:8> = 10 |
| CTMUI3 | IOUT3 | 100x Range ⁽¹⁾ | — | 55 | — | μA | CTMUCON<9:8> = 11 |
| CTMUI4 | IOUT4 | 1000x Range ⁽¹⁾ | — | 550 | — | μA | CTMUCON<9:8> = 00 |
| CTMUUFV1 | VF | Temperature Diode Forward Voltage ^(1,2) | — | 0.598 | — | V | T _A = +25°C, CTMUCON<9:8> = 01 |
| | | | — | 0.658 | — | V | T _A = +25°C, CTMUCON<9:8> = 10 |
| | | | — | 0.721 | — | V | T _A = +25°C, CTMUCON<9:8> = 11 |
| CTMUUFV2 | VFVR | Temperature Diode Rate of Change ^(1,2) | — | -1.92 | — | mV/°C | CTMUCON<9:8> = 01 |
| | | | — | -1.74 | — | mV/°C | CTMUCON<9:8> = 10 |
| | | | — | -1.56 | — | mV/°C | CTMUCON<9:8> = 11 |

Note 1: Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksp/s
- All PMD bits are cleared (PMDx = 0)
- Executing a `while(1)` statement
- Device operating from the FRC with no PLL

3: The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

31.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX 28/36/44-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 30.0 “Electrical Characteristics”**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter “M”, which denotes 50 MHz operation. For example, parameter DC29a in **Section 30.0 “Electrical Characteristics”**, is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/36/44-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

| | |
|--|---------------------------|
| Ambient temperature under bias | -40°C to +85°C |
| Storage temperature | -65°C to +150°C |
| Voltage on VDD with respect to VSS | -0.3V to +4.0V |
| Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3) | -0.3V to (VDD + 0.3V) |
| Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V (Note 3) | -0.3V to +5.5V |
| Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V (Note 3) | -0.3V to +3.6V |
| Voltage on D+ or D- pin with respect to VUSB3V3 | -0.3V to (VUSB3V3 + 0.3V) |
| Voltage on VBUS with respect to VSS | -0.3V to +5.5V |
| Maximum current out of VSS pin(s) | 300 mA |
| Maximum current into VDD pin(s) (Note 2) | 300 mA |
| Maximum output current sunk by any I/O pin | 15 mA |
| Maximum output current sourced by any I/O pin | 15 mA |
| Maximum current sunk by all ports | 200 mA |
| Maximum current sourced by all ports (Note 2) | 200 mA |

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: See the “**Pin Diagrams**” section for the 5V tolerant pins.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

| Section | Update Description |
|--|--|
| 29.0 “Electrical Characteristics” | <p>Updated the Absolute Maximum Ratings (removed Voltage on V_{CORE} with respect to V_{SS}).</p> <p>Added the SPDIP specification to the Thermal Packaging Characteristics (see Table 29-2).</p> <p>Updated the Typical values for parameters DC20-DC24 in the Operating Current (I_{DD}) specification (see Table 29-5).</p> <p>Updated the Typical values for parameters DC30a-DC34a in the Idle Current (I_{IDLE}) specification (see Table 29-6).</p> <p>Updated the Typical values for parameters DC40i and DC40n and removed parameter DC40m in the Power-down Current (I_{PD}) specification (see Table 29-7).</p> <p>Removed parameter D320 (V_{CORE}) from the Internal Voltage Regulator Specifications and updated the Comments (see Table 29-13).</p> <p>Updated the Minimum, Typical, and Maximum values for parameter F20b in the Internal FRC Accuracy specification (see Table 29-17).</p> <p>Removed parameter SY01 (TPWRT) and removed all Conditions from Resets Timing (see Table 29-20).</p> <p>Updated all parameters in the CTMU Specifications (see Table 29-39).</p> |
| 31.0 “Packaging Information” | Added the 28-lead SPDIP package diagram information (see 31.1 “Package Marking Information” and 31.2 “Package Details”). |
| “Product Identification System” | Added the SPDIP (SP) package definition. |

Revision C (November 2011)

All major changes are referenced by their respective section in Table A-2.

TABLE A-2: MAJOR SECTION UPDATES

| Section | Update Description |
|--|---|
| “32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog” | <p>Revised the source/sink on I/O pins (see “Input/Output” on page 1).</p> <p>Added the SPDIP package to the PIC32MX220F032B device in the PIC32MX2XX USB Family Features (see Table 2).</p> |
| 4.0 “Memory Organization” | Removed ANSB6 from the ANSELB register and added the ODCB6, ODCB10, and ODCB11 bits in the PORTB Register Map (see Table 4-20). |
| 29.0 “Electrical Characteristics” | Updated the minimum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 29-16). |

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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