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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFl

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f128d-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	_	—	—		—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:10	—	—	_	—	—	—	—	—	
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	
15:8	BMXDKPBA<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
				BMXDK	PBA<7:0>				

REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Legend:

Legenu.					
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-16 Unimplemented: Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 BMXDKPBA<9:0>: Read-Only bits This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R	R	R	R	R	R	R	R	
31:24	BMXDRMSZ<31:24>								
00.40	R	R	R	R	R	R	R	R	
23:10	BMXDRMSZ<23:16>								
45.0	R	R	R	R	R	R	R	R	
15:8	BMXDRMSZ<15:8>								
7:0	R	R	R	R	R	R	R	R	
				BMXDR	MSZ<7:0>				

BMXDRMSZ: DATA RAM SIZE REGISTER REGISTER 4-5:

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BMXDRMSZ<31:0>: Data RAM Memory (DRM) Size bits

Static value that indicates the size of the Data RAM in bytes: 0x00001000 = Device has 4 KB RAM 0x00002000 = Device has 8 KB RAM 0x00004000 = Device has 16 KB RAM 0x00008000 = Device has 32 KB RAM 0x00010000 = Device has 64 KB RAM

REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	_	_	_	—	BMXPUPBA<19:16>				
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	
15:8	BMXPUPBA<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
				BMXPU	PBA<7:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 Unimplemented: Read as '0'

bit 19-11 BMXPUPBA<19:11>: Program Flash (PFM) User Program Base Address bits

bit 10-0 BMXPUPBA<10:0>: Read-Only bits This value is always '0', which forces 2 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXPFMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	_	—	_		_	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R-0	R-0	R-0	U-0	U-0	U-0
15:8	WR	WREN	WRERR ⁽¹⁾	LVDERR ⁽¹⁾	LVDSTAT ⁽¹⁾	—	_	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	_	_		_	NVMOP<3:0>			

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	id as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15	WR: Write Control bit
	This bit is writable when WREN = 1 and the unlock sequence is followed.
	 1 = Initiate a Flash operation. Hardware clears this bit when the operation completes 0 = Flash operation is complete or inactive
bit 14	WREN: Write Enable bit
	This is the only bit in this register reset by a device Reset.
	 1 = Enable writes to WR bit and enables LVD circuit 0 = Disable writes to WR bit and disables LVD circuit
bit 13	WRERR: Write Error bit ⁽¹⁾
	This bit is read-only and is automatically set by hardware.
	 1 = Program or erase sequence did not complete successfully 0 = Program or erase sequence completed normally
bit 12	LVDERR: Low-Voltage Detect Error bit (LVD circuit must be enabled) ⁽¹⁾
	This bit is read-only and is automatically set by hardware.
	 1 = Low-voltage detected (possible data corruption, if WRERR is set) 0 = Voltage level is acceptable for programming
bit 11	LVDSTAT: Low-Voltage Detect Status bit (LVD circuit must be enabled) ⁽¹⁾
	This bit is read-only and is automatically set and cleared by the hardware.
	1 = Low-voltage event is active
	0 = Low-voltage event is not active
bit 10-4	Unimplemented: Read as '0'
bit 3-0	NVMOP<3:0>: NVM Operation bits
	These bits are writable when WREN = 0.
	1111 = Reserved
	•
	0111 = Reserved
	0110 = No operation
	 0101 = Program Flash Memory (PFM) erase operation: erases PFM, if all pages are not write-protected 0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected 0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected
	0010 = No operation
	0000 = No operation

Note 1: This bit is cleared by setting NVMOP == `b0000, and initiating a Flash operation (i.e., WR).

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	-	—	—	-	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	_		_	_		—	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	_		_	_		—	_
7.0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
7.0	UACTPND			USLPGRD	USBBUSY ⁽¹⁾		USUSPEND	USBPWR

REGISTER 10-5: U1PWRC: USB POWER CONTROL REGISTER

Legend:

R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-8 Unimplemented: Read as '0'

- bit 7 UACTPND: USB Activity Pending bit
 - 1 = USB bus activity has been detected; however, an interrupt is pending, which has yet to be generated
 0 = An interrupt is not pending
- bit 6-5 Unimplemented: Read as '0'
- bit 4 USLPGRD: USB Sleep Entry Guard bit
 - 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
 - 0 = USB module does not block Sleep entry
- bit 3 USBBUSY: USB Module Busy bit⁽¹⁾
 - 1 = USB module is active or disabled, but not ready to be enabled
 - 0 = USB module is not active and is ready to be enabled
- bit 2 Unimplemented: Read as '0'
- bit 1 USUSPEND: USB Suspend Mode bit
 - 1 = USB module is placed in Suspend mode
 - (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
 - 0 = USB module operates normally
- bit 0 USBPWR: USB Operation Enable bit
 - 1 = USB module is turned on
 - 0 = USB module is disabled

(Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

Note 1: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—			—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	—	_	_	_			_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—			—
7.0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
7.0							FRMH<2:0>	

REGISTER 10-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 Unimplemented: Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits The register bits are updated with the current frame number whenever a SOF TOKEN is received.

Bit Bit Bit Bit Bit Bit Bit Bit Bit 30/22/14/6 27/19/11/3 26/18/10/2 25/17/9/1 24/16/8/0 Range 31/23/15/7 29/21/13/5 28/20/12/4 U-0 U-0 U-0 U-0 U-0 U-0 U-0 U-0 31:24 ___ ___ ____ ____ ____ ____ ___ ____ U-0 U-0 U-0 U-0 U-0 U-0 U-0 U-0 23:16 ____ ___ ____ ____ ____ ____ ____ ___ U-0 U-0 U-0 U-0 U-0 U-0 U-0 U-0 15:8 _ ___ ____ ____ ____ ___ ____ ____ R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 7:0 PID < 3:0 > (1)EP<3:0>

REGISTER 10-15: U1TOK: USB TOKEN REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits⁽¹⁾

1101 = SETUP (TX) token type transaction

- 1001 = IN (RX) token type transaction
- 0001 = OUT (TX) token type transaction

Note: All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits The four bit value must specify a valid endpoint.

Note 1: All other values are reserved and must not be used.

12.2 Timer1 Control Registers

TABLE 12-1: TIMER1 REGISTER MAP

ess		0								В	its								6
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0600		31:16	_	—	—	—	-	—	—	—	-	—	—	-	—	-	-	—	0000
0000	TICON	15:0	ON	_	SIDL	TWDIS	TWIP	—	_	—	TGATE	_	TCKP	S<1:0>	—	TSYNC	TCS	_	0000
0610		31:16	_	_	—	—	—	—	_	—	—	_	_	—	—	—	—	_	0000
0010		15:0								TMR1	<15:0>								0000
0620	DD1	31:16	_	_	_	_	_	_	_	_	_	_		_	_	_	_	_	0000
0020	FÅL	15:0								PR1<	<15:0>								FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
15.6	ON ⁽¹⁾	—	SIDL	TWDIS	TWIP	—	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
7.0	TGATE		TCKP	S<1:0>		TSYNC	TCS	_

REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Timer On bit⁽¹⁾
 - 1 = Timer is enabled
 - 0 = Timer is disabled

bit 14 Unimplemented: Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit

- 1 = Writes to Timer1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:

- 1 = Asynchronous write to the Timer1 register in progress
- 0 = Asynchronous write to Timer1 register is complete
- In Synchronous Timer mode:

This bit is read as '0'.

- bit 10-8 **Unimplemented:** Read as '0'
- bit 7 TGATE: Timer Gated Time Accumulation Enable bit
 - When TCS = 1:

This bit is ignored.

When TCS = 0:

- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 Unimplemented: Read as '0'

bit 5-4 TCKPS<1:0>: Timer Input Clock Prescale Select bits

- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value
- **Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

15.1 **Input Capture Control Registers**

AB	LE 15-1:	IN	PUT CA	PTURE	E 1-INPU		URE 5	REGIST	ER MA	2							
ess		â								Bi	ts						
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1
2000		31:16				—	—	_	—						—	—	—
2000	IC ICON.	15:0	ON		SIDL	_	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2010	IC1BUF	31:16 15:0								IC1BUF	<31:0>						
2200		31:16	_	_	_	—	—	_	—	—	_	-	-	_	—	—	_
2200	1020011	15:0	ON		SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2210	IC2BUF	31:16 15:0								IC2BUF	<31:0>						
2400		31:16	—	—	_	_	—	_	_	—	_	—	_	—	_	—	_
2400	IC3CON /	15:0	ON	_	SIDL	—	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2410	IC3BUF	31:16 15:0								IC3BUF	<31:0>						
2600		31:16	_		_	-	-		—	—	_				—	—	_
2000	1040011	15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2610	IC4BUF	31:16 15:0								IC4BUF	<31:0>						
2800		31:16	_		_	-	-		—	—	_				—	—	—
2000	1000010	15:0	ON	_	SIDL	—	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2810	IC5BUF	31:16 15:0								IC5BUF	<31:0>						

T

Legend:

This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information. Note 1:

All Resets

0000

0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx

16/0

—

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	—	FEDGE	C32
7.0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
7:0	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>	

REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unkno	own)	P = Programmable bit	r = Reserved bit

bit 31-16	Unimplemented: Read as '0'
bit 15	ON: Input Capture Module Enable bit ⁽¹⁾
	1 = Module is enabled
	0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Stop in Idle Control bit
	1 = Halt in Idle mode0 = Continue to operate in Idle mode
bit 12-10	Unimplemented: Read as '0'
bit 9	FEDGE: First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
	1 = Capture rising edge first
	0 = Capture falling edge first
bit 8	C32: 32-bit Capture Select bit
	1 = 32-bit timer resource capture
	0 = 16-bit timer resource capture
bit 7	ICTMR: Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
	0 = Timer3 is the counter source for capture
DIT 6-5	ICI<1:0>: Interrupt Control bits
	10 = Interrupt on every tourth capture event
	01 = Interrupt on every second capture event
	00 = Interrupt on every capture event
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
	1 = Input capture overflow has occurred
	0 = No input capture overflow has occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	 1 = Input capture buffer is not empty; at least one more capture value can be read 0 = Input capture buffer is empty
Note 1:	When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the
	STOCEN Gyole infinediately following the instruction that deals the module's ON bit.

REGISTER 15-1: ICXCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

ICM<2:0>: Input Capture Mode Select bits

bit 2-0

- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode every sixteenth rising edge
- 100 = Prescaled Capture Event mode every fourth rising edge
- 011 = Simple Capture Event mode every rising edge
- 010 = Simple Capture Event mode every falling edge
- 001 = Edge Detect mode every edge (rising and falling)
- 000 = Input Capture module is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	_	_		—	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ⁽¹⁾	—	SIDL	_	_		—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0			OC32	OCFLT ⁽²⁾	OCTSEL		OCM<2:0>	

REGISTER 16-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Output Compare Peripheral On bit⁽¹⁾
 - 1 = Output Compare peripheral is enabled
 - 0 = Output Compare peripheral is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when the device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode

bit 12-6 Unimplemented: Read as '0'

- bit 5 OC32: 32-bit Compare Mode bit
 - 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source
- bit 4 OCFLT: PWM Fault Condition Status bit⁽²⁾
 - 1 = PWM Fault condition has occurred (cleared in hardware only)
 - 0 = No PWM Fault condition has occurred
- bit 3 **OCTSEL:** Output Compare Timer Select bit
 - 1 = Timer3 is the clock source for this Output Compare module
 - 0 = Timer2 is the clock source for this Output Compare module
- bit 2-0 OCM<2:0>: Output Compare Mode Select bits
 - 111 = PWM mode on OCx; Fault pin enabled
 - 110 = PWM mode on OCx; Fault pin disabled
 - 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
 - 100 = Initialize OCx pin low; generate single output pulse on OCx pin
 - 011 = Compare event toggles OCx pin
 - 010 = Initialize OCx pin high; compare event forces OCx pin low
 - 001 = Initialize OCx pin low; compare event forces OCx pin high
 - 000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED) bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bit 11 = Reserved; do not use 10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters) 01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters) 00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character) bit 5 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect. 0 = Address Detect mode is disabled bit 4 **RIDLE:** Receiver Idle bit (read-only) 1 =Receiver is Idle 0 = Data is being received PERR: Parity Error Status bit (read-only) bit 3 1 = Parity error has been detected for the current character 0 = Parity error has not been detected bit 2 FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character 0 = Framing error has not been detected **OERR:** Receive Buffer Overrun Error Status bit. bit 1 This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state. 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)

- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P	
	—	—	—	—	—	— FWDTWINSZ<1:0>			
00.40	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P	
23:10	FWDTEN	WINDIS	—	WDTPS<4:0>					
45.0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P	
15:8	FCKSM	/<1:0>	FPBDIV<1:0> —		—	OSCIOFNC	POSCM	OD<1:0>	
7.0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P	
7:0	IESO	—	FSOSCEN	—	— — FNOSC<2:0>				

REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Legend: r = Reserved bit		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 Reserved: Write '1'

bit 25-24 FWDTWINSZ<1:0>: Watchdog Timer Window Size bits

- 11 = Window size is 25%
- 10 = Window size is 37.5%
- 01 = Window size is 50%
- 00 = Window size is 75%

bit 23 FWDTEN: Watchdog Timer Enable bit

- 1 = Watchdog Timer is enabled and cannot be disabled by software
- 0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 WINDIS: Watchdog Timer Window Enable bit

- 1 = Watchdog Timer is in non-Window mode
- 0 = Watchdog Timer is in Window mode

bit 21 Reserved: Write '1'

bit 20-16 WDTPS<4:0>: Watchdog Timer Postscale Select bits

0
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

REGISTER 27-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

- bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
 - 111 = 12x divider
 - 110 = 10x divider
 - 101 = 6x divider
 - 100 = 5x divider
 - 011 = 4x divider
 - 010 = 3x divider
 - 001 = 2x divider
 - 000 = 1x divider
- Note 1: This bit is only available on PIC32MX2XX devices.

TABLE 30-9: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param. No.	Symbol	Characteristics	Min. Typ. ⁽¹⁾ Max. Units Conditions				Conditions
DI60a	licl	Input Low Injection Current	0	_	₋₅ (2,5)	mA	This parameter applies to all pins, with the exception of the power pins.
DI60b	Іісн	Input High Injection Current	0	_	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, and the SOSCI, SOSCO, OSC1, D+, and D- pins.
DI60c	∑lict	Total Input Injection Current (sum of all I/O and Control pins)	-20 (6)	_	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (IICL + IICH) $\leq \sum$ IICT)

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If Note 2, IICL = (((Vss - 0.3) - VIL source) / Rs). If Note 3, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (Vss - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4		40 40	MHz MHz	EC (Note 4) ECPLL (Note 3)
OS11		Oscillator Crystal Frequency	3	_	10	MHz	XT (Note 4)
OS12			4	—	10	MHz	XTPLL (Notes 3,4)
OS13			10	—	25	MHz	HS (Note 5)
OS14			10	—	25	MHz	HSPLL (Notes 3,4)
OS15			32	32.768	100	kHz	Sosc (Note 4)
OS20	Tosc	Tosc = 1/Fosc = Tcy (Note 2)	_	_			See parameter OS10 for Fosc value
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.45 x Tosc	—	_	ns	EC (Note 4)
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x Tosc	ns	EC (Note 4)
OS40	Тоѕт	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	_	1024	_	Tosc	(Note 4)
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 4)
OS42	Gм	External Oscillator Transconductance (Primary Oscillator only)		12		mA/V	VDD = 3.3V, TA = +25°C (Note 4)

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

2: Instruction cycle period (Tcr) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

3: PLL input requirements: 4 MHz \leq FPLLIN \leq 5 MHz (use PLL prescaler to reduce FOSC). This parameter is characterized, but tested at 10 MHz only at manufacturing.

4: This parameter is characterized, but not tested in manufacturing.

TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

АС СНА	RACTER	ISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Трв * (BRG + 2)	_	μs	_
			400 kHz mode	Трв * (BRG + 2)	_	μs	—
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs	_
IM11	THI:SCL	Clock High Time	100 kHz mode	Трв * (BRG + 2)	—	μS	—
			400 kHz mode	Трв * (BRG + 2)	—	μS	—
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS	_
IM20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF
			1 MHz mode (Note 2)	_	100	ns	
IM21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF
			1 MHz mode (Note 2)	—	300	ns	
IM25	TSU:DAT	Data Input	100 kHz mode	250		ns	
		Setup Time	400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μS	—
			400 kHz mode	0	0.9	μS	
			1 MHz mode (Note 2)	0	0.3	μS	
IM30	TSU:STA	A Start Condition Setup Time	100 kHz mode	Трв * (BRG + 2)		μS	Only relevant for
			400 kHz mode	Трв * (BRG + 2)	—	μS	Repeated Start
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition	100 kHz mode	Трв * (BRG + 2)		μs	After this period, the
		Hold Time	400 kHz mode	Трв * (BRG + 2)	—	μS	first clock pulse is
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs	generaleu
IM33	Tsu:sto	Stop Condition	100 kHz mode	Трв * (BRG + 2)		μs	
		Setup Time	400 kHz mode	Трв * (BRG + 2)		μs	
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS	
IM34	THD:STO	Stop Condition	100 kHz mode	Трв * (BRG + 2)		ns	—
		Hold Time	400 kHz mode	Трв * (BRG + 2)		ns	
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	ns	

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

TABLE 30-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industria} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Charact	eristics	Min.	Max.	Units	Conditions	
IS34	THD:STO	Stop Condition	100 kHz mode	4000	_	ns	_	
		Hold Time	400 kHz mode	600	—	ns		
			1 MHz mode (Note 1)	250		ns		
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—	
			400 kHz mode	0	1000	ns		
			1 MHz mode (Note 1)	0	350	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus	
			400 kHz mode	1.3	—	μs	must be free before a new	
			1 MHz mode (Note 1)	0.5	—	μS	transmission can start	
IS50	Св	Bus Capacitive Loading		_	400	pF	—	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS					
Dimension	Limits	MIN	NOM	MAX		
Number of Pins	N	28				
Pitch	е		1.27 BSC			
Overall Height	A	-	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D	17.90 BSC				
Chamfer (Optional)	h	0.25	-	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1	1.40 REF				
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

Revision G (April 2015)

This revision includes the addition of the following devices:

- PIC32MX130F256B PIC32MX230F256B
- PIC32MX130F256D PIC32MX230F256D

The title of the document was updated to avoid confusion with the PIC32MX1XX/2XX/5XX 64/100-pin Family data sheet.

TABLE A-6: MAJOR SECTION UPDATES

All peripheral SFR maps have been relocated from the Memory chapter to their respective peripheral chapters.

In addition, this revision includes the following major changes as described in Table A-6, as well as minor updates to text and formatting, which were incorporated throughout the document.

Section	Update Description
32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog	Added new devices to the family features (see Table 1 and Table 2). Updated pin diagrams to include new devices (see Pin Diagrams).
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Updated these sections: 2.2 "Decoupling Capacitors", 2.3 "Capacitor on Internal Voltage Regulator (VCAP)", 2.4 "Master Clear (MCLR) Pin", 2.8.1 "Crystal Oscillator Design Consideration"
4.0 "Memory Organization"	Added Memory Map for new devices (see Figure 4-6).
14.0 "Watchdog Timer (WDT)"	New chapter created from content previously located in the Special Features chapter.
30.0 "Electrical Characteristics"	Removed parameter D312 (TSET) from the Comparator Specifications (see Table 30-12).
	Added the Comparator Voltage Reference Specifications (see Table 30-13).
	Updated Table 30-12.

Revision H (July 2015)

This revision includes the following major changes as described in Table A-7, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-7: MAJOR SECTION UPDATES

Section	Update Description				
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Section 2.9 "Sosc Design Recommendation" was removed.				
8.0 "Oscillator Configuration"	The Primary Oscillator (Posc) logic in the Oscillator diagram was updated (see Figure 8-1).				
30.0 "Electrical Characteristics"	The Power-Down Current (IPD) DC Characteristics parameter DC40k was updated (see Table 30-7).				
	Table 30-9: "DC Characteristics: I/O Pin Input Injection current Specifications" was added.				