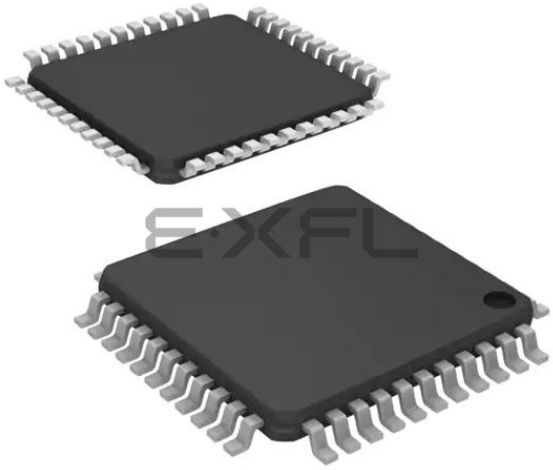

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f128dt-v-pt

TABLE 4: PIN NAMES FOR 28-PIN USB DEVICES

28-PIN SOIC, SPDIP, SSOP (TOP VIEW)(1,2,3)

PIC32MX210F016B
PIC32MX220F032B
PIC32MX230F064B
PIC32MX230F256B
PIC32MX250F128B
PIC32MX270F256B

Pin #	Full Pin Name	Pin #	Full Pin Name
1	$\overline{\text{MCLR}}$	15	V_{BUS}
2	PGED3/V_{REF}+/CV_{REF}+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	PGEC3/V_{REF}-/CV_{REF}-/AN1/RPA1/CTED2/PMD6/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	19	V_{SS}
6	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	20	V_{CAP}
7	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	21	PGED2/RPB10/D+/CTED11/RB10
8	V_{SS}	22	PGEC2/RPB11/D-/RB11
9	OSC1/CLKI/RPA2/RA2	23	V_{USB3V3}
10	OSC2/CLKO/RPA3/PMA0/RA3	24	AN11/RPB13/CTPLS/PMRD/RB13
11	SOSCI/RPB4/RB4	25	CV_{REFOUT}/AN10/C3INB/RPB14/V_{BUSON}/SCK1/CTED5/RB14
12	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	V_{DD}	27	AV_{SS}
14	TMS/RPB5/USBID/RB5	28	AV_{DD}

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
AN0	27	2	33	19	I	Analog	Analog input channels.
AN1	28	3	34	20	I	Analog	
AN2	1	4	35	21	I	Analog	
AN3	2	5	36	22	I	Analog	
AN4	3	6	1	23	I	Analog	
AN5	4	7	2	24	I	Analog	
AN6	—	—	3	25	I	Analog	
AN7	—	—	4	26	I	Analog	
AN8	—	—	—	27	I	Analog	
AN9	23	26	29	15	I	Analog	
AN10	22	25	28	14	I	Analog	
AN11	21	24	27	11	I	Analog	
AN12	20(2)	23(2)	26(2) 11(3)	10(2) 36(3)	I	Analog	
CLKI	6	9	7	30	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	7	10	8	31	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	6	9	7	30	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	7	10	8	31	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	8	11	9	33	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	9	12	10	34	O	—	32.768 kHz low-power oscillator crystal output.
REFCLKI	PPS	PPS	PPS	PPS	I	ST	Reference Input Clock
REFCLKO	PPS	PPS	PPS	PPS	O	—	Reference Output Clock
IC1	PPS	PPS	PPS	PPS	I	ST	Capture Inputs 1-5
IC2	PPS	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
RC0	—	—	3	25	I/O	ST	PORTC is a bidirectional I/O port
RC1	—	—	4	26	I/O	ST	
RC2	—	—	—	27	I/O	ST	
RC3	—	—	11	36	I/O	ST	
RC4	—	—	—	37	I/O	ST	
RC5	—	—	—	38	I/O	ST	
RC6	—	—	—	2	I/O	ST	
RC7	—	—	—	3	I/O	ST	
RC8	—	—	—	4	I/O	ST	
RC9	—	—	20	5	I/O	ST	
T1CK	9	12	10	34	I	ST	Timer1 external clock input
T2CK	PPS	PPS	PPS	PPS	I	ST	Timer2 external clock input
T3CK	PPS	PPS	PPS	PPS	I	ST	Timer3 external clock input
T4CK	PPS	PPS	PPS	PPS	I	ST	Timer4 external clock input
T5CK	PPS	PPS	PPS	PPS	I	ST	Timer5 external clock input
$\overline{U1CTS}$	PPS	PPS	PPS	PPS	I	ST	UART1 clear to send
$\overline{U1RTS}$	PPS	PPS	PPS	PPS	O	—	UART1 ready to send
U1RX	PPS	PPS	PPS	PPS	I	ST	UART1 receive
U1TX	PPS	PPS	PPS	PPS	O	—	UART1 transmit
$\overline{U2CTS}$	PPS	PPS	PPS	PPS	I	ST	UART2 clear to send
$\overline{U2RTS}$	PPS	PPS	PPS	PPS	O	—	UART2 ready to send
U2RX	PPS	PPS	PPS	PPS	I	ST	UART2 receive
U2TX	PPS	PPS	PPS	PPS	O	—	UART2 transmit
SCK1	22	25	28	14	I/O	ST	Synchronous serial clock input/output for SPI1
SDI1	PPS	PPS	PPS	PPS	I	ST	SPI1 data in
SDO1	PPS	PPS	PPS	PPS	O	—	SPI1 data out
$\overline{SS1}$	PPS	PPS	PPS	PPS	I/O	ST	SPI1 slave synchronization or frame pulse I/O
SCK2	23	26	29	15	I/O	ST	Synchronous serial clock input/output for SPI2
SDI2	PPS	PPS	PPS	PPS	I	ST	SPI2 data in
SDO2	PPS	PPS	PPS	PPS	O	—	SPI2 data out
$\overline{SS2}$	PPS	PPS	PPS	PPS	I/O	ST	SPI2 slave synchronization or frame pulse I/O
SCL1	14	17	18	44	I/O	ST	Synchronous serial clock input/output for I2C1

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e® Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt)* operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

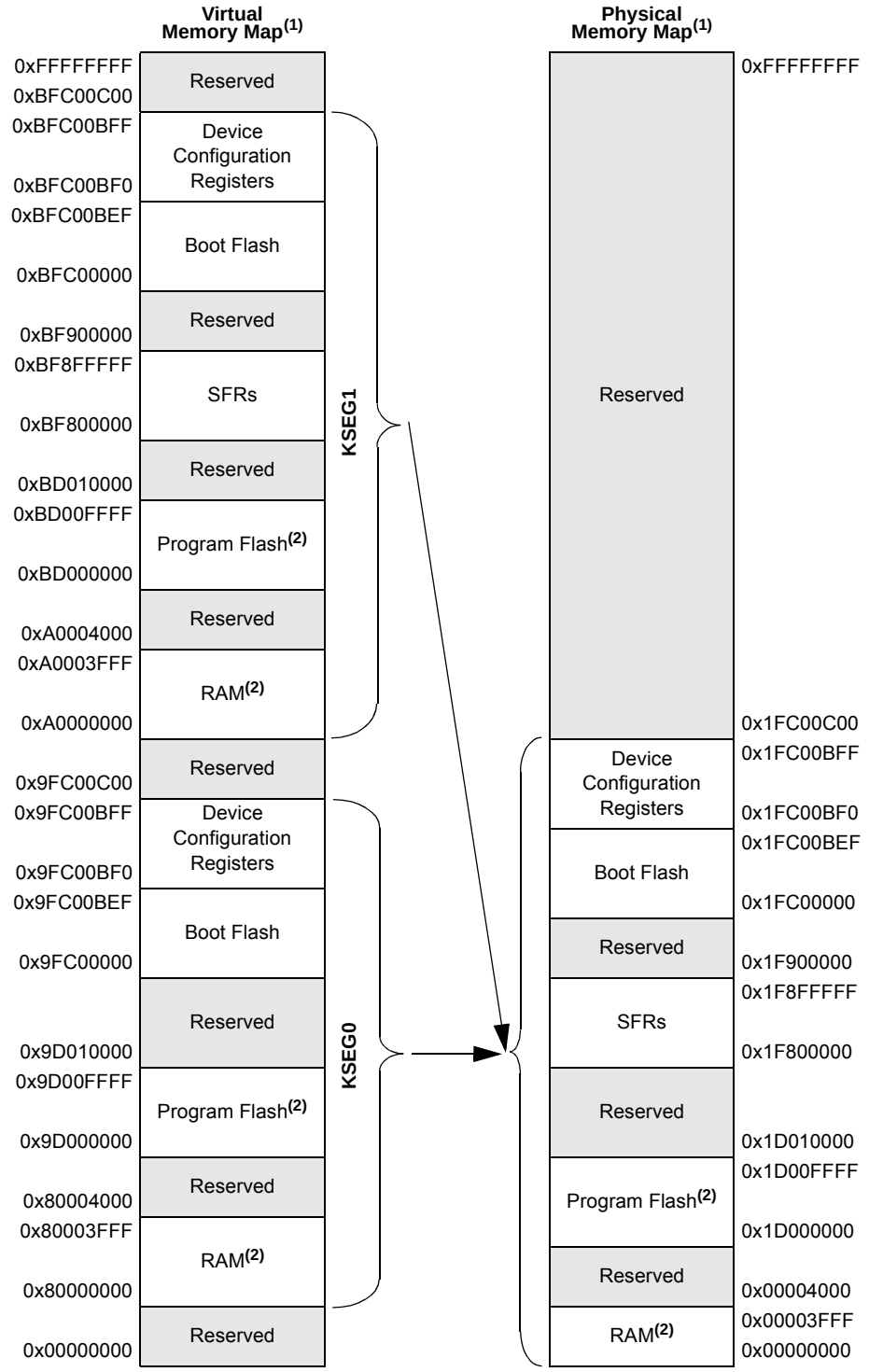
Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent `MDU` instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS32® M4K® PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU, MADD/MADDU, MSUB/MSUBU`	16 bits	1	1
	32 bits	2	2
`MUL`	16 bits	2	1
	32 bits	3	2
`DIV/DIVU`	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 64 KB FLASH)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

9.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32, such as Peripheral Bus devices: SPI, UART, PMP, etc., or memory itself. Figure 9-1 show a block diagram of the DMA Controller module.

The DMA Controller module has the following key features:

- Four identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

FIGURE 9-1: DMA BLOCK DIAGRAM

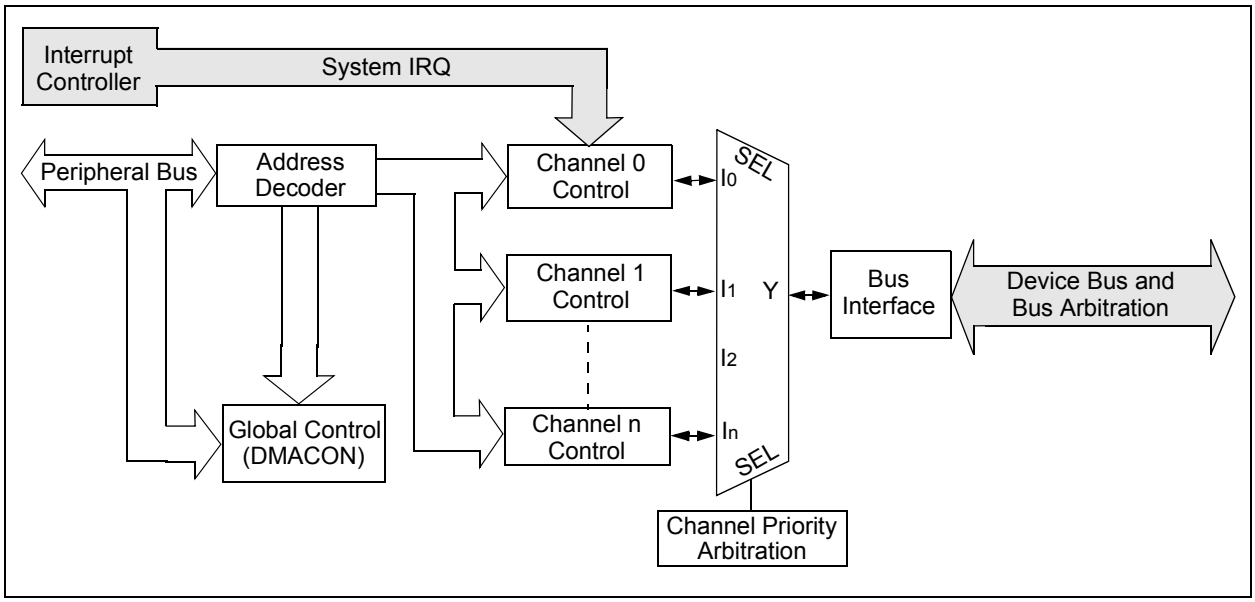


TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3210	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3220	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

REGISTER 10-5: U1PWRC: USB POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	—	—	USLPGRD	USBBUSY(1)	—	USUSPEND	USBPWR

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB bus activity has been detected; however, an interrupt is pending, which has yet to be generated
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode
  (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit
- 1 = USB module is turned on
- 0 = USB module is disabled
  (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

Note 1: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FB4C	RPB8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB8<3:0>				0000
FB50	RPB9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB9<3:0>				0000
FB54	RPB10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB10<3:0>				0000
FB58	RPB11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB11<3:0>				0000
FB60	RPB13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB13<3:0>				0000
FB64	RPB14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB14<3:0>				0000
FB68	RPB15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB15<3:0>				0000
FB6C	RPC0R(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC0<3:0>				0000
FB70	RPC1R(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC1<3:0>				0000
FB74	RPC2R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC2<3:0>				0000
FB78	RPC3R(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC3<3:0>				0000
FB7C	RPC4R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC4<3:0>				0000
FB80	RPC5R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC5<3:0>				0000
FB84	RPC6R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC6<3:0>				0000
FB88	RPC7R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC7<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is only available on 44-pin devices.
2: This register is only available on PIC32MX1XX devices.
3: This register is only available on 36-pin and 44-pin devices.

REGISTER 11-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A, B, C)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit
- 1 = CN is enabled
- 0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Idle mode halts CN operation
- 0 = Idle does not affect CN operation

bit 12-0 **Unimplemented:** Read as '0'

14.1 Watchdog Timer Control Registers

TABLE 14-1: WATCHDOG TIMER CONTROL REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					WDTWINEN	WDTCLR	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

16.0 OUTPUT COMPARE

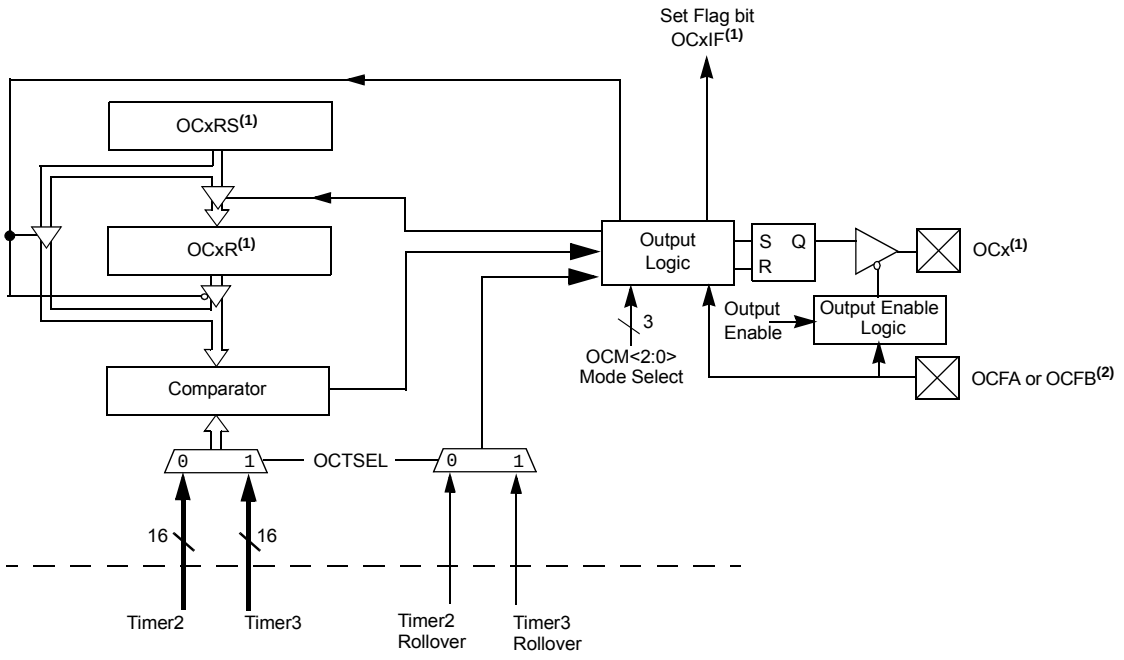
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are some of the key features:

- Multiple Output Compare Modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

FIGURE 16-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 5.

2: The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

NOTES:

20.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

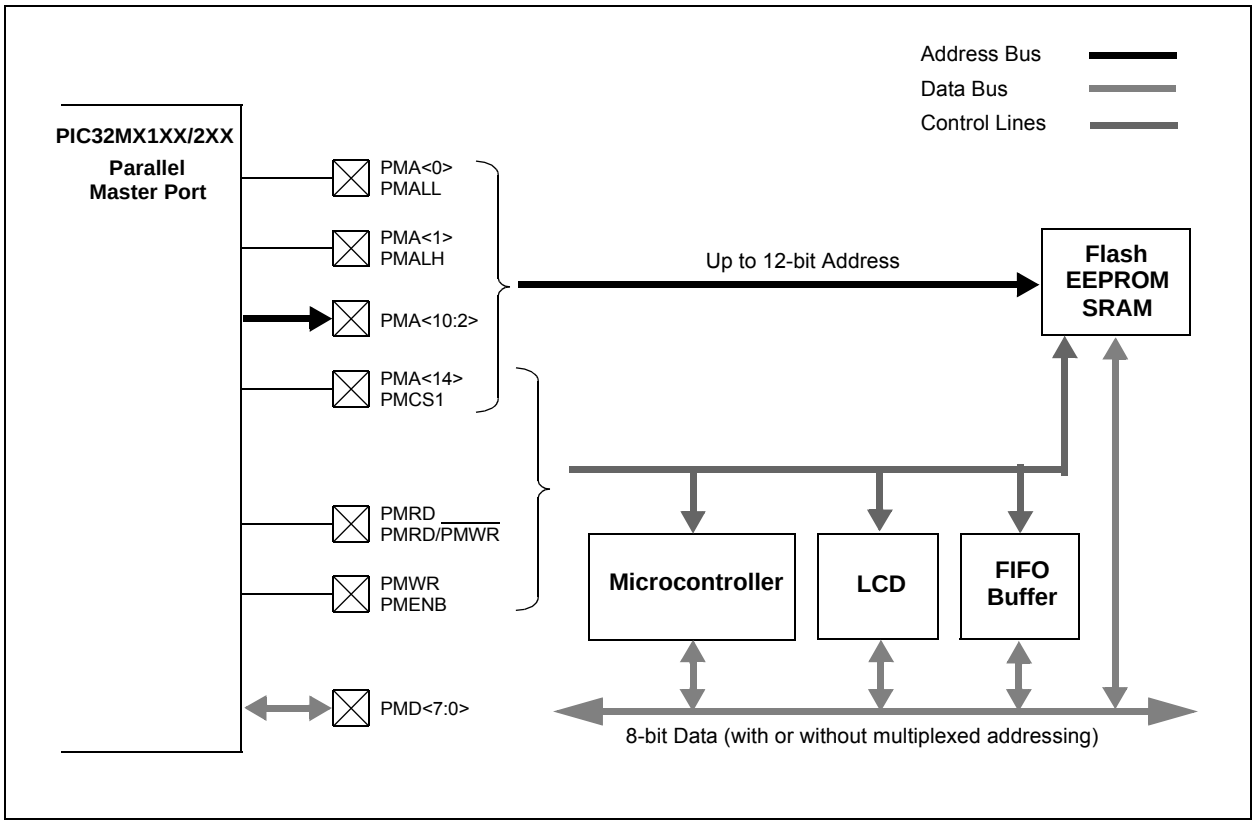
The PMP is a parallel 8-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- Fully multiplexed address/data mode
- Demultiplexed or partially multiplexed address/data mode
  - up to 11 address lines with single Chip Select
  - up to 12 address lines without Chip Select
- One Chip Select line
- Programmable strobe options
  - Individual read and write strobes or;
  - Read/$\overline{\text{write}}$ strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Legacy parallel slave port support
- Enhanced parallel slave support
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Selectable input voltage levels

Figure 20-1 illustrates the PMP module block diagram.

FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(2)		ALP(2)	—	CS1P(2)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit(1)
- 1 = PMP enabled
- 0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
- 11 = Lower 8 bits of address are multiplexed on PMD<7:0> pins; upper 8 bits are not used
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<10:8> and PMA<14>
- 00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
- 1 = PMWR/PMENB port enabled
- 0 = PMWR/PMENB port disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
- 1 = PMRD/PMWR port enabled
- 0 = PMRD/PMWR port disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
- 11 = Reserved
- 10 = PMCS1 functions as Chip Select
- 01 = PMCS1 functions as PMA<14>
- 00 = PMCS1 functions as PMA<14>

bit 5 **ALP:** Address Latch Polarity bit(2)
- 1 = Active-high (PMALL and PMALH)
- 0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

NOTES:

REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 24 **EDG1STAT:** Edge1 Status bit
Indicates the status of Edge1 and can be written to control edge source
1 = Edge1 has occurred
0 = Edge1 has not occurred

bit 23 **EDG2MOD:** Edge2 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 22 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge2 programmed for a positive edge response
0 = Edge2 programmed for a negative edge response

bit 21-18 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = C3OUT pin is selected
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = PBCLK clock is selected
1011 = IC3 Capture Event is selected
1010 = IC2 Capture Event is selected
1001 = IC1 Capture Event is selected
1000 = CTED13 pin is selected
0111 = CTED12 pin is selected
0110 = CTED11 pin is selected
0101 = CTED10 pin is selected
0100 = CTED9 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 17-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ON Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode

bit 12 **TGEN:** Time Generation Enable bit**(1)**
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 30-41) in **Section 30.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

REGISTER 27-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 18-10 **PWP<8:0>:** Program Flash Write-Protect bits(3)

Prevents selected program Flash memory pages from being modified during code execution.
111111111 = Disabled
111111110 = Memory below 0x0400 address is write-protected
111111101 = Memory below 0x0800 address is write-protected
111111100 = Memory below 0x0C00 address is write-protected
111111011 = Memory below 0x1000 (4K) address is write-protected
111111010 = Memory below 0x1400 address is write-protected
111111001 = Memory below 0x1800 address is write-protected
111111000 = Memory below 0x1C00 address is write-protected
111110111 = Memory below 0x2000 (8K) address is write-protected
111110110 = Memory below 0x2400 address is write-protected
111110101 = Memory below 0x2800 address is write-protected
111110100 = Memory below 0x2C00 address is write-protected
111110011 = Memory below 0x3000 address is write-protected
111110010 = Memory below 0x3400 address is write-protected
111110001 = Memory below 0x3800 address is write-protected
111110000 = Memory below 0x3C00 address is write-protected
111101111 = Memory below 0x4000 (16K) address is write-protected
.
.
.
110111111 = Memory below 0x10000 (64K) address is write-protected
.
.
.
101111111 = Memory below 0x20000 (128K) address is write-protected
.
.
.
011111111 = Memory below 0x40000 (256K) address is write-protected
.
.
.
000000000 = All possible memory is write-protected

bit 9-5 **Reserved:** Write '1'

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits(2)

11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = PGEC4/PGED4 pair is used(2)

bit 2 **JTAGEN:** JTAG Enable bit(1)

1 = JTAG is enabled
0 = JTAG is disabled

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)

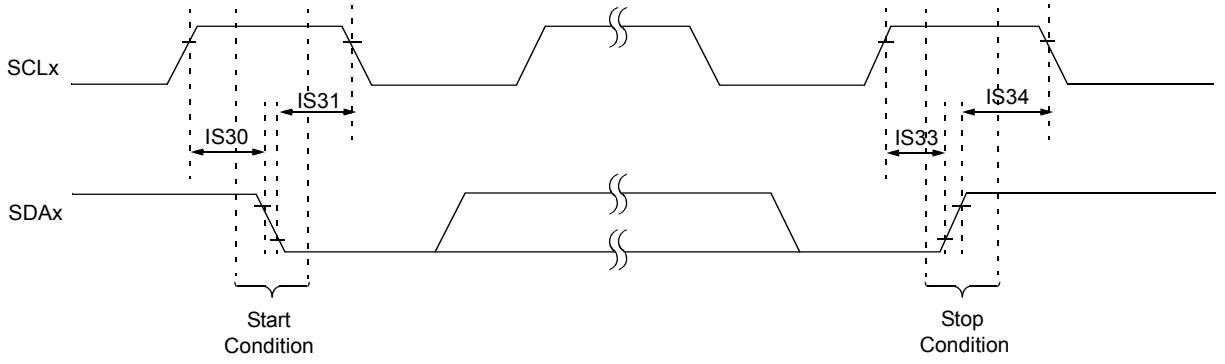
1x = Debugger is disabled
0x = Debugger is enabled

Note 1: This bit sets the value for the JTAGEN bit in the CFGCON register.

2: The PGEC4/PGED4 pin pair is not available on all devices. Refer to the **"Pin Diagrams"** section for availability.

3: The PWP<8:7> bits are only available on devices with 256 KB Flash.

FIGURE 30-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 30-1 for load conditions.

FIGURE 30-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)