Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f256b-50i-so

TABLE 8: PIN NAMES FOR 36-PIN USB DEVICES

36-PIN VTLA (TOP VIEW)[1,2,3,5]

PIC32MX210F016C
PIC32MX220F032C
PIC32MX230F064C
PIC32MX250F128C

36

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	19	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	20	RPC9/CTED7/RC9
3	PGED4[4]/AN6/RPC0/RC0	21	V_{SS}
4	PGEC4[4]/AN7/RPC1/RC1	22	V_{CAP}
5	V_{DD}	23	V_{DD}
6	V_{SS}	24	PGED2/RPB10/D+/CTED11/RB10
7	OSC1/CLKI/RPA2/RA2	25	PGEC2/RPB11/D-/RB11
8	OSC2/CLKO/RPA3/PMA0/RA3	26	V_{USB3V3}
9	SOSCI/RPB4/RB4	27	AN11/RPB13/CTPLS/PMRD/RB13
10	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	28	CVREFOUT/AN10/C3INB/RPB14/V_{BUSON}/SCK1/CTED5/RB14
11	AN12/RPC3/RC3	29	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
12	V_{SS}	30	AV_{SS}
13	V_{DD}	31	AV_{DD}
14	V_{DD}	32	$\overline{MCLR}$
15	TMS/RPB5/USBID/RB5	33	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
16	V_{BUS}	34	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1
17	TDI/RPB7/CTED3/PMD5/INT0/RB7	35	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0
18	TCK/RPB8/SCL1/CTED10/PMD4/RB8	36	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to V_{SS} externally.

4: This pin function is not available on PIC32MX210F016C and PIC32MX120F032C devices.

5: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
MCLR	26	1	32	18	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	25	28	31	17	P	—	Positive supply for analog modules. This pin must be connected at all times.
AVSS	24	27	30	16	P	—	Ground reference for analog modules
VDD	10	13	5, 13, 14, 23	28, 40	P	—	Positive supply for peripheral logic and I/O pins
VCAP	17	20	22	7	P	—	CPU logic filter capacitor connection
VSS	5, 16	8, 19	6, 12, 21	6, 29, 39	P	—	Ground reference for logic and I/O pins. This pin must be connected at all times.
VREF+	27	2	33	19	I	Analog	Analog voltage reference (high) input
VREF-	28	3	34	20	I	Analog	Analog voltage reference (low) input

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   P = Power
ST = Schmitt Trigger input with CMOS levels   O = Output   I = Input
TTL = TTL input buffer   PPS = Peripheral Pin Select   — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

    2: Pin number for PIC32MX1XX devices only.

    3: Pin number for PIC32MX2XX devices only.

4.0 MEMORY ORGANIZATION

Note:	This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.

FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 256 KB FLASH)

Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).
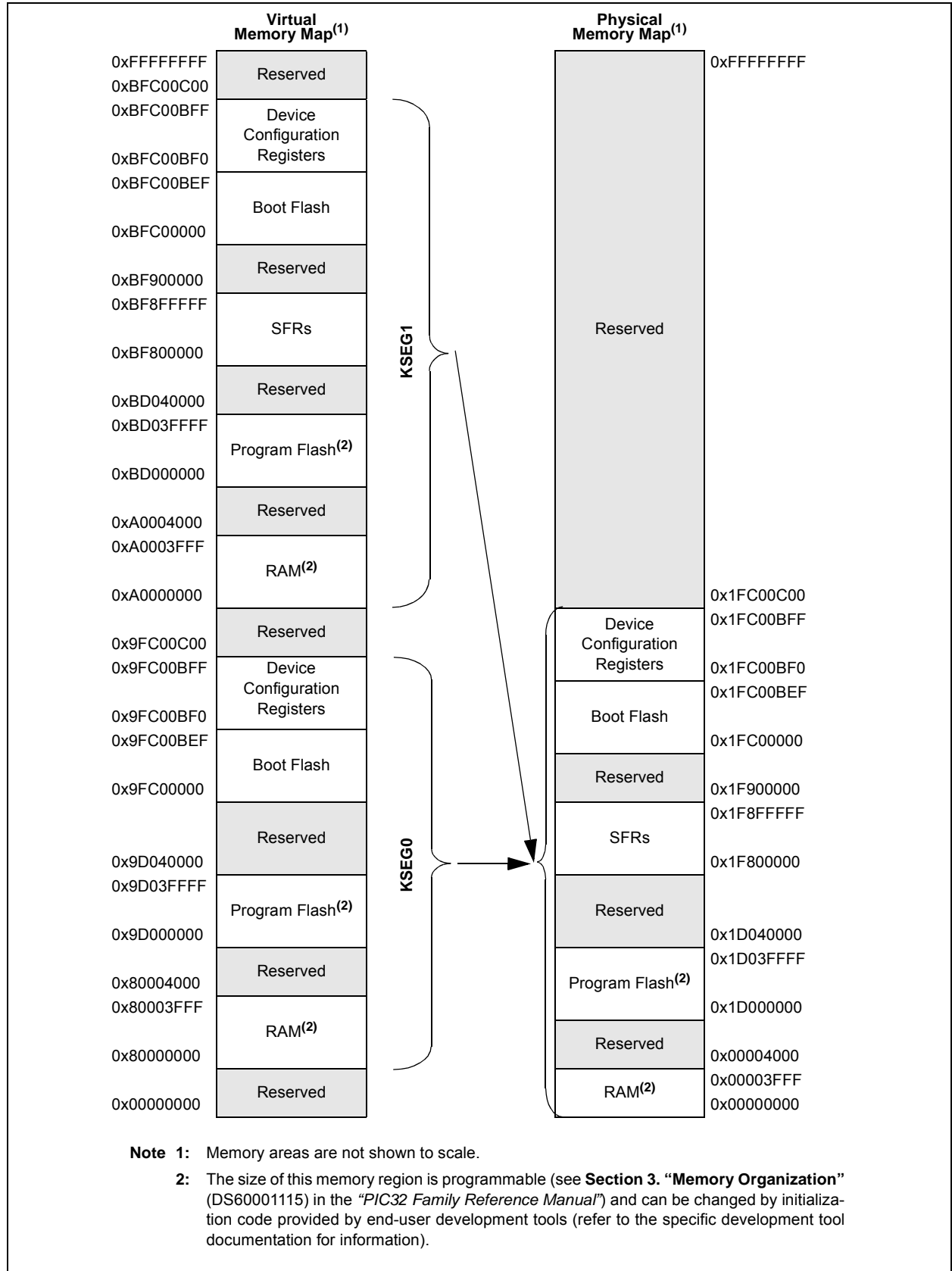
REGISTER 7-6: **IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)**

bit 9-8   **IS01<1:0>:** Interrupt Subpriority bits

     11 = Interrupt subpriority is 3
     10 = Interrupt subpriority is 2
     01 = Interrupt subpriority is 1
     00 = Interrupt subpriority is 0

bit 7-5   **Unimplemented:** Read as '0'

bit 4-2   **IP00<2:0>:** Interrupt Priority bits

     111 = Interrupt priority is 7
     •
     •
     •
     010 = Interrupt priority is 2
     001 = Interrupt priority is 1
     000 = Interrupt is disabled

bit 1-0   **IS00<1:0>:** Interrupt Subpriority bits

     11 = Interrupt subpriority is 3
     10 = Interrupt subpriority is 2
     01 = Interrupt subpriority is 1
     00 = Interrupt subpriority is 0

Note:	This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

FIGURE 8-1: OSCILLATOR DIAGRAM
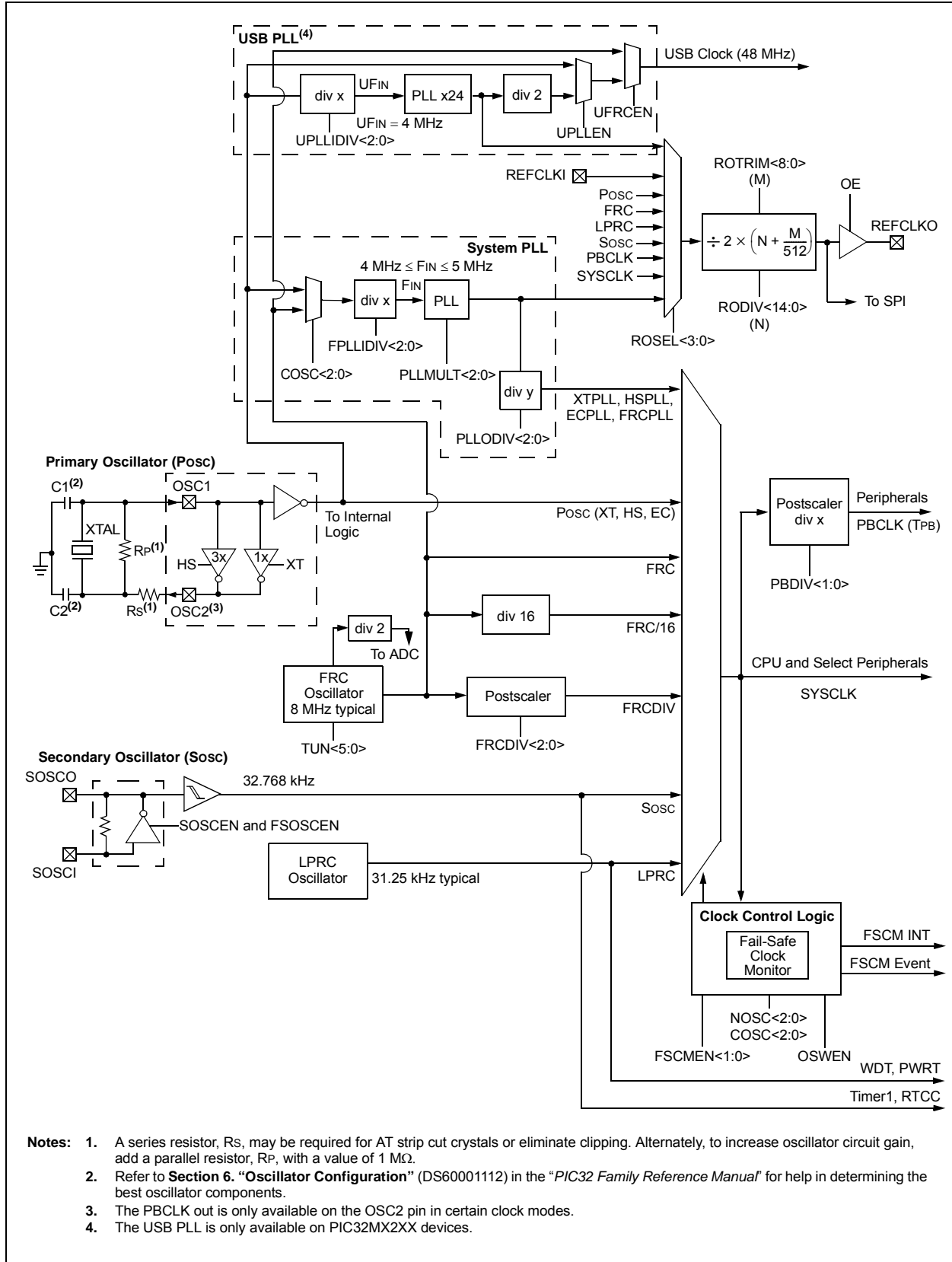
Notes: 1. A series resistor, R_S, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, R_P, with a value of 1 MΩ.
2. Refer to **Section 6. "Oscillator Configuration"** (DS60001112) in the "*PIC32 Family Reference Manual*" for help in determining the best oscillator components.
3. The PBCLK out is only available on the OSC2 pin in certain clock modes.
4. The USB PLL is only available on PIC32MX2XX devices.

9.1 DMA Control Registers

TABLE 9-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF88_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	DMACH<2:0>[2]			0000
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

TABLE 9-2: DMA CRC REGISTER MAP

Virtual Address (BF88_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
3040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
3050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

TABLE 11-6: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FA54	U1CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1CTSR<3:0>				0000
FA58	U2RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2RXR<3:0>				0000
FA5C	U2CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2CTSR<3:0>				0000
FA84	SDI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI1R<3:0>				0000
FA88	SS1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS1R<3:0>				0000
FA90	SDI2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI2R<3:0>				0000
FA94	SS2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS2R<3:0>				0000
FAB8	REFCLKIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKIR<3:0>				0000

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

> **Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontrollers. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), etc. The PIC32 SPI module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master mode and Slave mode support
- Four clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^2S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 17-1: SPI MODULE BLOCK DIAGRAM
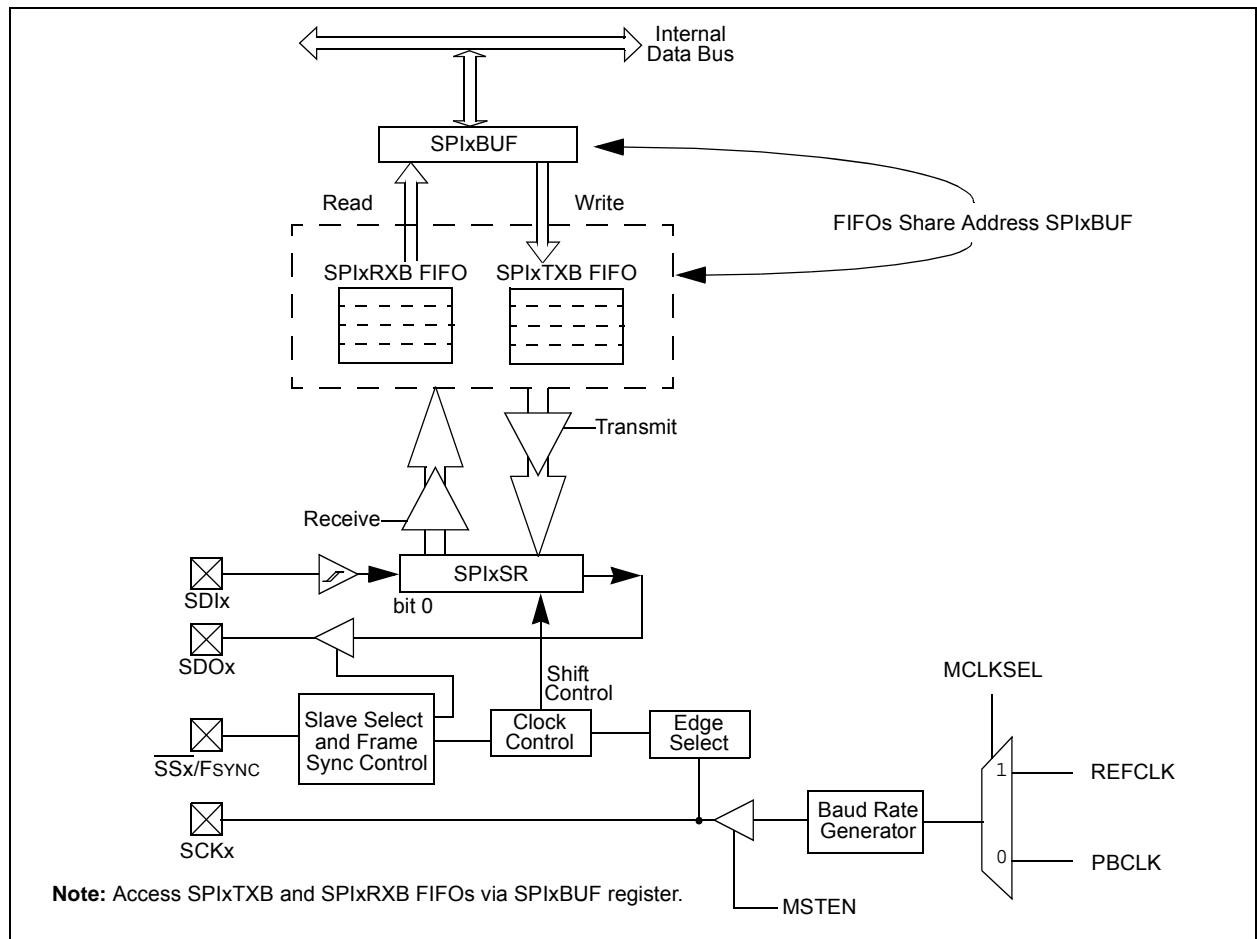
REGISTER 19-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON[1]	—	SIDL	IREN	RTSMD	—	UEN<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit[1]

1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by the UEN<1:0> and UTXEN control bits.
0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal.

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit

1 = IrDA is enabled
0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{UxRTS}$ Pin bit

1 = $\overline{UxRTS}$ pin is in Simplex mode
0 = $\overline{UxRTS}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits

11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{UxCTS}$ pin is controlled by corresponding bits in the PORTx register
10 = UxTX, UxRX, $\overline{UxCTS}$ and $\overline{UxRTS}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{UxRTS}$ pins are enabled and used; $\overline{UxCTS}$ pin is controlled by corresponding bits in the PORTx register
00 = UxTX and UxRX pins are enabled and used; $\overline{UxCTS}$ and $\overline{UxRTS}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
1 = Wake-up enabled
0 = Wake-up disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Loopback mode is enabled
0 = Loopback mode is disabled

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 19-1: **UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 5 **ABAUD:** Auto-Baud Enable bit

1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion

0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit

1 = UxRX Idle state is '0'

0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit

1 = High-Speed mode – 4x baud clock enabled

0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits

11 = 9-bit data, no parity

10 = 8-bit data, odd parity

01 = 8-bit data, even parity

00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit

1 = 2 Stop bits

0 = 1 Stop bit

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON[1]	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>[2]		ALP[2]	—	CS1P[2]	—	WRSP	RDSP

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit[1]

1 = PMP enabled
0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits

11 = Lower 8 bits of address are multiplexed on PMD<7:0> pins; upper 8 bits are not used
10 = All 16 bits of address are multiplexed on PMD<7:0> pins
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<10:8> and PMA<14>
00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit

1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit

1 = PMWR/PMENB port enabled
0 = PMWR/PMENB port disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit

1 = PMRD/PMWR port enabled
0 = PMRD/PMWR port disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits[2]

11 = Reserved
10 = PMCS1 functions as Chip Select
01 = PMCS1 functions as PMA<14>
00 = PMCS1 functions as PMA<14>

bit 5 **ALP:** Address Latch Polarity bit[2]

1 = Active-high (PMALL and PMALH)
0 = Active-low (PMALL and PMALH)

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

21.1 RTCC Control Registers

TABLE 21-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0200	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	—	—	—	RTSECSEL	RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0220	RTCTIME	31:16	—	—	HR10<1:0>		HR01<3:0>				—	MIN10<2:0>			MIN01<3:0>				xxxx
		15:0	—	SEC10<2:0>			SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				—	—	—	MONTH10	MONTH01<3:0>				xxxx
		15:0	—	—	DAY10<1:0>		DAY01<3:0>				—	—	—	—	—	WDAY01<2:0>			xx00
0240	ALRMTIME	31:16	—	—	HR10<1:0>		HR01<3:0>				—	MIN10<2:0>			MIN01<3:0>				xxxx
		15:0	—	SEC10<2:0>			SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MONTH10	MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	—	WDAY01<2:0>			xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

REGISTER 27-5: **CFGCON: CONFIGURATION CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	—	—	IOLOCK[1]	PMDLOCK[1]	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-1	R/W-1
	—	—	—	—	JTAGEN	—	—	TDOEN

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-14   **Unimplemented:** Read as '0'

bit 13   **IOLOCK:** Peripheral Pin Select Lock bit[1]

    1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
    0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.

bit 12   **PMDLOCK:** Peripheral Module Disable bit[1]

    1 = Peripheral module is locked. Writes to PMD registers is not allowed.
    0 = Peripheral module is not locked. Writes to PMD registers is allowed.

bit 11-4   **Unimplemented:** Read as '0'

bit 3   **JTAGEN:** JTAG Port Enable bit

    1 = Enable the JTAG port
    0 = Disable the JTAG port

bit 2-1   **Unimplemented:** Read as '1'

bit 0   **TDOEN:** TDO Enable for 2-Wire JTAG bit

    1 = 2-wire JTAG protocol uses TDO
    0 = 2-wire JTAG protocol does not use TDO

Note 1:   To change this bit, the unlock sequence must be performed. Refer to **Section 6. "Oscillator"**
(DS60001112) in the *"PIC32 Family Reference Manual"* for details.

28.0 INSTRUCTION SET

The PIC32MX1XX/2XX family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

> **Note:** Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

NOTES:

TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp					
Param. No.	Symbol	Characteristics[1]	Min.	Typical	Max.	Units	Conditions	
OS50	F_{PLLI}	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	3.92	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes	
OS51	F_{SYS}	On-Chip VCO System Frequency	60	—	120	MHz	—	
OS52	T_{LOCK}	PLL Start-up Time (Lock Time)	—	—	2	ms	—	
OS53	D_{CLK}	CLKO Stability[2] (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\dfrac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 40 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\dfrac{40}{20}}} = \frac{D_{CLK}}{1.41}$$

TABLE 30-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions	
Internal FRC Accuracy @ 8.00 MHz[1]							
F20b	FRC	-0.9	—	+0.9	%	—	

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

TABLE 30-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions	
LPRC @ 31.25 kHz[1]							
F21	LPRC	-15	—	+15	%	—	

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 32-6: TYPICAL FRC FREQUENCY @ V_{DD} = 3.3V
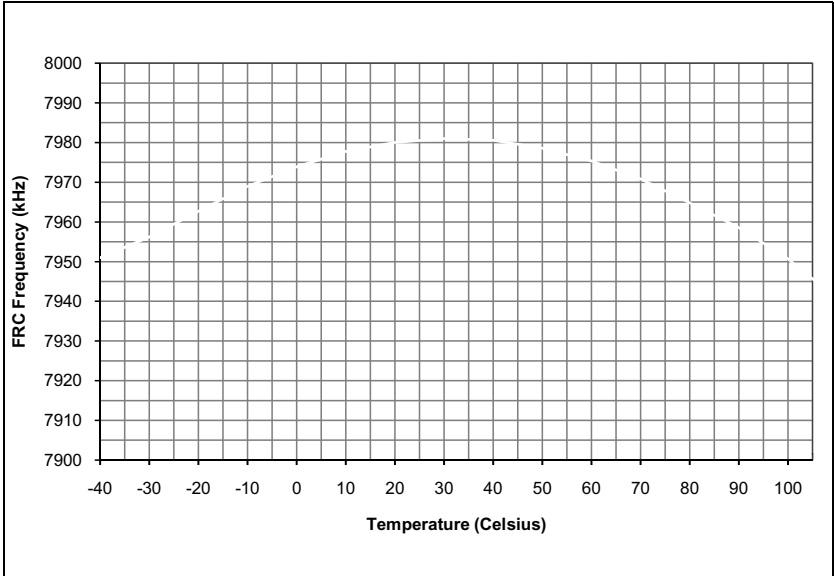

FIGURE 32-7: TYPICAL LPRC FREQUENCY @ V_{DD} = 3.3V
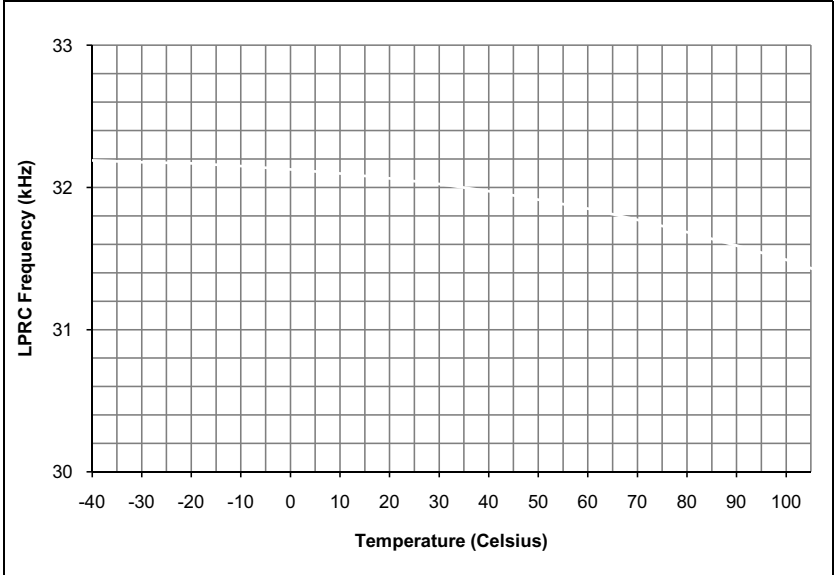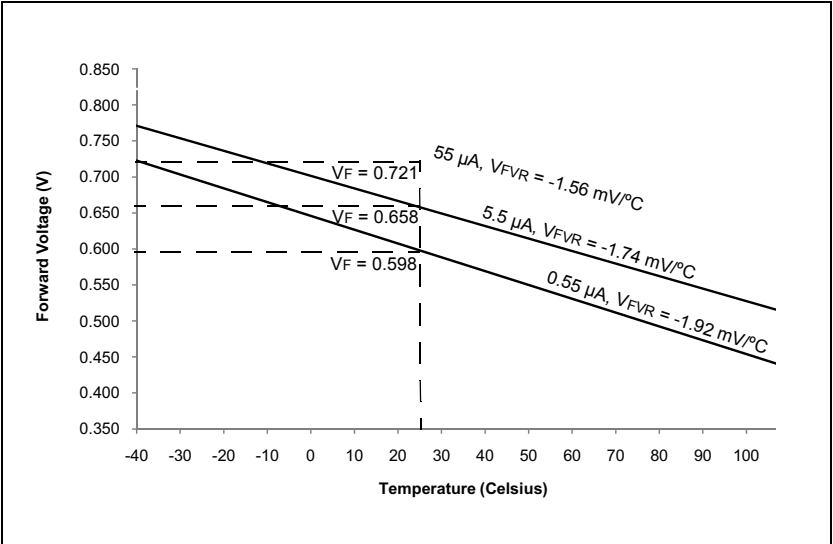

FIGURE 32-8: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE
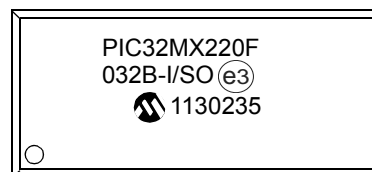

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

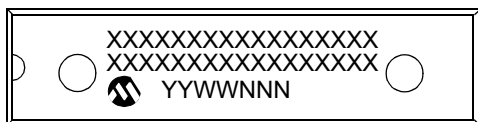## 33.0 PACKAGING INFORMATION

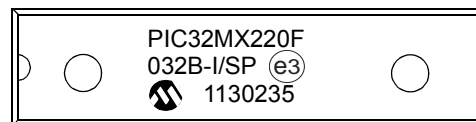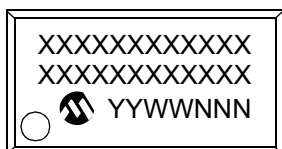### 33.1 Package Marking Information

28-Lead SOIC

```
XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX
   (M) YYWWNNN
○
```
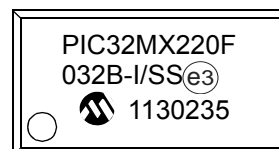
Example

```
PIC32MX220F
032B-I/SO (e3)
   (M) 1130235
○
```

28-Lead SPDIP

```
      XXXXXXXXXXXXXXXXX
      XXXXXXXXXXXXXXXXX
   (M) YYWWNNN
```

Example

```
      PIC32MX220F
      032B-I/SP (e3)
   (M) 1130235
```

28-Lead SSOP

```
XXXXXXXXXXX
XXXXXXXXXXX
   (M) YYWWNNN
○
```

Example

```
PIC32MX220F
032B-I/SS(e3)
   (M) 1130235
○
```

28-Lead QFN

```
•    (M)

XXXXXXXX
XXXXXXXX
YYWWNNN
```

Example

```
•    (M)

32MX220F
032BE/ML(e3)
1130235
```

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

Revision D (February 2012)

All occurrences of VUSB were changed to: VUSB3V3. In addition, text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-3:   MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Corrected a part number error in all pin diagrams. Updated the DMA Channels (Programmable/Dedicated) column in the PIC32MX1XX General Purpose Family Features (see Table 1).
1.0 "Device Overview"	Added the TQFP and VTLA packages to the 44-pin column heading and updated the pin numbers for the SCL1, SCL2, SDA1, and SDA2 pins in the Pinout I/O Descriptions (see Table 1-1).
7.0 "Interrupt Controller"	Updated the Note that follows the features. Updated the Interrupt Controller Block Diagram (see Figure 7-1).
29.0 "Electrical Characteristics"	Updated the Maximum values for parameters DC20-DC24, and the Minimum value for parameter DC21 in the Operating Current (IDD) DC Characteristics (see Table 29-5). Updated all Minimum and Maximum values for the Idle Current (IIDLE) DC Characteristics (see Table 29-6). Updated the Maximum values for parameters DC40k, DC40l, DC40n, and DC40m in the Power-down Current (IPD) DC Characteristics (see Table 29-7). Changed the minimum clock period for SCKx from 40 ns to 50 ns in Note 3 of the SPIx Master and Slave Mode Timing Requirements (see Table 29-26 through Table 29-29).
30.0 "DC and AC Device Characteristics Graphs"	Updated the Typical IIDLE Current @ VDD = 3.3V graph (see Figure 30-5).