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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f256b-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.8.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- COUT = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e.,12 mm length) = 2.5 pF

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION



The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

- Select a crystal with a lower "minimum" power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing "ESR" rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.
- Note: Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, RS, as shown in circuit "C" in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to ~VDD-0.6V. When measuring the oscillator signal you must use a FET scope probe or a probe with ≤ 1.5 pF or the scope probe itself will unduly change the gain and peak-to-peak levels.

2.8.1.1 Additional Microchip References

- AN588 "PICmicro[®] Microcontroller Oscillator Design Guide"
- AN826 "Crystal Oscillator Basics and Crystal Selection for rfPIC[™] and PICmicro[®] Devices"
- AN849 "Basic PICmicro[®] Oscillator Design"



4.2 Bus Matrix Control Registers

TABLE 4-2: BUS MATRIX REGISTER MAP

ess)		ø										Bits							
Virtual Addr (BF88_#	Register Name	Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000		31:16	_		_	_	—	_		_	_	—	_	BMXERRIXI	BMXERRICD	BMXERRDMA	BMXERRDS	BMXERRIS	001F
2000	BINIXCON	15:0		_	_	_	_	-		—	_	BMXWSDRM	_	_	—	BI	MXARB<2:0>		0041
2010		31:16	_		_		_	_		_	_	_	_	_	—	_	_	_	0000
2010	DIVIADAPDA'	15:0									BN	IXDKPBA<15:0>	>						0000
2020		31:16	_					_		—	_	—	—	_	—		_		0000
2020	BINIADODBA	15:0	BMXDUDBA<15:0> 00														0000		
2030		31:16	—	_	_		_	—	_	—	—	—	—	—	—	—	—	-	0000
2000		15:0									BN	IXDUPBA<15:0>	>						0000
2040	BMXDRMS7	31:16									BM	XDRMS7<31.0	>						xxxx
2040	DIVINDI (IVIOZ	15:0																	xxxx
2050		31:16	—	—				—	_	—	—		_	_		BMXPUPBA	<19:16>		0000
2000		15:0	0 BMXPUPBA<15:0> 0000																
2060	BMYDEMS7	31:16									BM								xxxx
2000	DWXTTWOZ	15:0									DIV								xxxx
2070	BMXBOOTS7	31:16	6 0000											0000					
2070	DWIXDOUTSZ	15:0									DIVI	NDOUT32531.0	~						0C00

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

6.1 Reset Control Registers

TABLE 6-1: RESET CONTROL REGISTER MAP

Virtual Address (BF80_#) Register Name ⁽¹⁾							Bits					ú							
	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset	
F600	BCON	31:16	—	—	_	—	—	—	—	—	—	_	_	—	—	_	—	—	0000
	RCON	15:0	—	_	—	—	_	-	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	xxxx(2)
F610	DOMIDET	31:16	—	_	—	—	_	-	_	—	—	—	—	_	—	_	_	—	0000
	NOWRO1	15:0	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	SWRST	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

(1)	IRQ	Vector		Interru	pt Bit Location		Persistent
Interrupt Source ⁽¹⁾	#	#	Flag	Enable	Priority	Sub-priority	Interrupt
		Highes	st Natural O	rder Priority	,		
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1E – SPI1 Fault	36	31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1TX – SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

TABLE 7-2: INTERRUPT REGISTER MAP (CONTINUED)

dress #)		đ								Bits									
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1100		31:16	—	—	—		SPI1IP<2:0>		SPI1IS	<1:0>	—	—	—	US	USBIP<2:0> ⁽²⁾			<1:0> (2)	0000
1100	IPC/	15:0	-	—	_	(CMP3IP<2:0>	>	CMP3IS	6<1:0>	-	_		CN	/IP2IP<2:0>	•	CMP2I	S<1:0>	0000
1110		31:16		—	_	PMPIP<2:0>			PMPIS	<1:0>	_	_		C	NIP<2:0>		CNIS	<1:0>	0000
1110	IFCO	15:0	-	_	-		I2C1IP<2:0>		I2C1IS	<1:0>	_		-	L	J1IP<2:0>		U1IS	<1:0>	0000
1120		31:16	-	—	_	(CTMUIP<2:0	>	CTMUIS	S<1:0>	-	_		12	C2IP<2:0>		12C215	6<1:0>	0000
1120	IFC9	15:0		—	_		U2IP<2:0>		U2IS<	:1:0>	_	_		S	PI2IP<2:0>		SPI2IS	6<1:0>	0000
1120		31:16	—	—	—	[DMA3IP<2:0>	>	DMA3IS	6<1:0>	—	—	_	DN	/IA2IP<2:0>	•	DMA2I	S<1:0>	0000
1130	IPC10	15:0	_	_	_	[DMA1IP<2:0>	>	DMA1IS	S<1:0>	—	_	—	DN	/A0IP<2:0>	•	DMA0I	S<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: These bits are not available on PIC32MX1XX devices.

3: This register does not have associated CLR, SET, INV registers.

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
31:24	—	—	BYTC)<1:0>	WBO ⁽¹⁾	—	—	BITO
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	_
45.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	—	—	—			PLEN<4:0>		
7.0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
7:0	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	_	(CRCCH<2:0>	

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

- bit 29-28 BYTO<1:0>: CRC Byte Order Selection bits
 - 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
 - 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
 - 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
 - 00 = No swapping (i.e., source byte order)
- bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾
 - 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
 - 0 = Source data is written to the destination unaltered
- bit 26-25 Unimplemented: Read as '0'
- bit 24 BITO: CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode):

- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 Unimplemented: Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits

<u>When CRCTYP (DCRCCON<15>) = 1</u> (CRC module is in IP Header mode): These bits are unused.

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode): Denotes the length of the polynomial -1.

- bit 7 CRCEN: CRC Enable bit
 - 1 = CRC module is enabled and channel transfers are routed through the CRC module
 - 0 = CRC module is disabled and channel transfers proceed normally
- Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
31.24	—	—	—	—	—	—	—	—					
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
23:16	—	—	—	—	—	—	—	—					
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
15:8	CHSSIZ<15:8>												
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
7:0				CHSSIZ	<7:0>								

REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSSIZ<15:0>: Channel Source Size bits

1111111111111111 = 65,535 byte source size

REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
31.24	—	—	—	—	—	—	—	—					
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
23:10	—	—	—	—	—	—	—	—					
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
10.0				CHDSIZ	<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
7.0	CHDSIZ<7:0>												

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

IABL		11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)																	
SS										В	its								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FB4C	RPB8R	31:16	—	—	—	-	—	—	—	—	—	—	_	—	_	—	—	—	0000
		15:0		_									_			RPB8	<3:0>		0000
FB50	RPB9R	31:16		_	_	_	_	_			_	_			_			—	0000
		15:0	_	_	—	_	_	_	_	_	_	_	_	_		RPB9	<3:0>		0000
FB54	RPB10R	31:16	—	—	-	-	—	—	_	—	—	—	_	—	—	—	—	—	0000
	-	15:0	_	_	—		_	—	_	_	_	_	_	_		RPB10)<3:0>		0000
FB58	RPB11R	31:16	_	_	—		_	—	_	_	_	_	_	_	_	—	_	_	0000
		15:0		_	_		—	—					_	_		RPB1 ⁻	1<3:0>		0000
FB60	RPB13R	31:16		—	—	—	—	—	—	—	—	—	—	—	—				0000
		15:0		—	—	—	—	—	—	—	—	—	—	—		RPB1	3<3:0>		0000
FB64	RPB14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPB14	4<3:0>		0000
FB68	RPB15R	31:16	—	—	—	—	-		—	—				—	—		—	—	0000
	1. 5101	15:0	—	—	—	—	-		—	—				—		RPB1	5<3:0>		0000
FB6C	RPCOR(3)	31:16	—	—	—	-	—	—	—	—	—	—	—	—	—	—	—	—	0000
. 200		15:0	—	—	—	-	—	—	—	—	—	—	—	—		RPC0	<3:0>		0000
EB70	RPC1R(3)	31:16	_	—	—	—	_	_	_	_	—	—	_	—	_	—	_	—	0000
1 870	NI OIIX	15:0	_	—	—	—	_	_	_	_	—	—	_	—		RPC1	<3:0>		0000
FB74		31:16	_	—	—	—	_	_	_	_	—	—	_	—	_	—	_	—	0000
1014		15:0	_	—	—	—	_	_	_	_	—	—	_	—		RPC2	<3:0>		0000
EB78		31:16		—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	0000
1 870		15:0		—	—	—	—	—	—	—	—	—	—	—		RPC3	<3:0>		0000
FB7C		31:16		—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	0000
1 B/C		15:0	_	—	—	—	—	—	—	—	—	—	—	—		RPC4	<3:0>		0000
EDOO		31:16	-	—	—	—	—	—	—	—	—	—	—	—	-	—	-	-	0000
1 000	NF GOINT	15:0	_	—	—	—	—	—	—	—	—	—	—	—		RPC5	<3:0>		0000
ED94		31:16	—	—	—	—	—	—	_	—	—	—	—	—	—	—	—	—	0000
гро4	NECOK	15:0	—	—	—	—	—	—	_	—	—	—	—	—		RPC6	<3:0>		0000
ED80		31:16	—	—	—	—	—	—	_	—	—	—	—	—	—	—	—	—	0000
F 000	KFU/KU	15:0	_	_	_	_	_	_		_	_	_	_	_		RPC7	<3:0>		0000

OT AUTOUT DEALATED MAD

x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

This register is only available on 44-pin devices. Note 1:

2: 3:

This register is only available on PIC32MX1XX devices. This register is only available on 36-pin and 44-pin devices.

16.0 OUTPUT COMPARE

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 16. "Output Compare" (DS60001111), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation. The following are some of the key features:

- · Multiple Output Compare Modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Can operate from either of two available 16-bit time bases or a single 32-bit time base





17.1 SPI Control Registers

TABLE 17-1: SPI1 AND SPI2 REGISTER MAP

ess		6								Bi	ts								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FI	RMCNT<2:	0>	MCLKSEL	—	_	—	—	—	SPIFE	ENHBUF	0000
3000	SFILCON	15:0	ON	-	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISE	EL<1:0>	SRXISI	EL<1:0>	0000
E010	QDI1QTAT	31:16	_	_	_		RXE	BUFELM<4:	:0>		_	_	_		TX	BUFELM<4	:0>		0000
0100	SFIISTAI	15:0	—	—	—	FRMERR	SPIBUSY	-	_	SPITUR	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	0008
5020	SDI1BUE	31:16									31.05								0000
5620		15:0								DAIA	51.04								0000
5830	SPI1BRG	31:16	—		—	—	—	—	—	—	—	—	—	—	-	—	—	—	0000
3030		15:0	—	—	—						E	3RG<12:0>							0000
		31:16	_	—	—	—	—	_	—	—	—	—	—	—	—	—	-	—	0000
5840	SPI1CON2	15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMO	DC<1:0>	0000
	SDISCON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FI	RMCNT<2:	0>	MCLKSEL	_	_	_	_	_	SPIFE	ENHBUF	0000
5AUU	SFIZCON	15:0	ON	_	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISE	EL<1:0>	SRXISI	EL<1:0>	0000
	CDIPCTAT	31:16		—	—		RXE	BUFELM<4:	:0>		—	_	_		TX	BUFELM<4	:0>		0000
5A10	3F1231AI	15:0		—	—	FRMERR	SPIBUSY	_	—	SPITUR	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	8000
E A 20		31:16									31.05								0000
5AZU	3F12D01	15:0								DAIA	51.0~								0000
EA 20	SDISEDC	31:16	_	—	—	_	_	_	—	—	_	—	—	—	—	—	_	—	0000
5A30		15:0	—		—			-			E	3RG<12:0>		-		-			0000
		31:16	—	-	—	—	-	—	—	-	-	-	—	—	-	—	—	—	0000
5A40	SPI2CON2	15:0	SPI SGNEXT	-	_	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	_	-	_	AUD MONO	_	AUDMO)D<1:0>	0000

Legend: x = unknown value on Reset; -- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

18.1 I2C Control Registers

TABLE 18-1: I2C1 AND I2C2 REGISTER MAP

ess	Register Name ⁽¹⁾		Bits																
Virtual Addr (BF80_#)		Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5000	1201000	31:16	_	_		_	_	-	_	_	_	_	_	_		_	_	_	0000
5000	12CTCON	15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5010	010 I2C1STAT	31:16	_	_		—	_		—	_	_	_	_	_	-	_	_	_	0000
		15:0	ACKSTAT	TRSTAT		—	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
5020		31:16	—	—	_		—			—	_				—		—	_	0000
0020	12017188	15:0	—	—	—	—	—	—					Address	Register					0000
5030	I2C1MSK	31:16	—	_	_	—	—			—	_	—	—	—	—	_	—	_	0000
		15:0	_	_			_						Address Ma	ask Register					0000
5040	I2C1BRG	31:16	_	—	_	-	—	_	—	—		—	—	—	—	—	—	—	0000
		15:0	—	_	_	—					Bau	id Rate Ger	erator Reg	ister					0000
5050	I2C1TRN	31:16	_	_	—	—	—	—	—	_	_	—	—	_		—	—	_	0000
		15:0	_	—	_		—			_				Transmit	Register				0000
5060	I2C1RCV	31:16		_			_			_		_	_			_	—		0000
		15:0	_	_			_			_				Receive	Register				0000
5100	I2C2CON	31:16	_	_	-	-	-	—	—	-	-	-	-	-	-	-	-		0000
		15:0	ON	_	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5110	I2C2STAT	31.10					_								-				0000
		15.0	ACKSTAT	IRSIAI				BUL	GCSTAT	ADD IU	IWCOL	12000	A	P	3	<u></u> vv	KDF	IBF	0000
5120	I2C2ADD	15.0							_	—	_	_		— Pogistor	_	_	_	_	0000
		31.16					_						Address	Keyistei	_		_		0000
5130	I2C2MSK	15.0		_		<u> </u>	_		1				Address Ma	l Isk Register					0000
		31:16	_	_		_			_	_	_		_		_		_	_	0000
5140	I2C2BRG	15:0	_	_	_	_					Bau	id Rate Ger	erator Reg	ister					0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
5150	I2C2TRN	15:0	_	_	_	_	_	_	_	_				Transmit	Register				0000
- 10-		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
5160	I2C2RCV	15:0	_	_	_	_	_	_	_	_				Receive	Register				0000
Legen	wend: x = unknown value on Reset: — = unimplemented. read as '0'. Reset values are shown in hexadecimal.																		

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information. Note 1:

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED) bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bit 11 = Reserved; do not use 10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters) 01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters) 00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character) bit 5 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect. 0 = Address Detect mode is disabled bit 4 **RIDLE:** Receiver Idle bit (read-only) 1 =Receiver is Idle 0 = Data is being received PERR: Parity Error Status bit (read-only) bit 3 1 = Parity error has been detected for the current character 0 = Parity error has not been detected bit 2 FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character 0 = Framing error has not been detected **OERR:** Receive Buffer Overrun Error Status bit. bit 1 This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state. 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)

- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

- bit 1-0 WAITE<1:0>: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾
 - 11 = Wait of 4 Трв
 - 10 = Wait of 3 Трв
 - 01 = Wait of 2 TPB
 - 00 = Wait of 1 TPB (default)

For Read operations:

- 11 = Wait of 3 TPB
- 10 = Wait of 2 TPB
- 01 = Wait of 1 ТРВ
- 00 = Wait of 0 TPB (default)
- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	_	_	—	_			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	—	—	—	—	_	_	—	_			
45.0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
15:8	—	PTEN14	—	—	_		PTEN<10:8>				
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0	PTEN<7:0>										

REGISTER 20-4: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 Unimplemented: Read as '0'

- bit 15-14 **PTEN14:** PMCS1 Address Port Enable bits
 - 1 = PMA14 functions as either PMA14 or PMCS1⁽¹⁾
 - 0 = PMA14 functions as port I/O
- bit 13-11 Unimplemented: Read as '0'
- bit 10-2 PTEN<10:2>: PMP Address Port Enable bits
 - 1 = PMA<10:2> function as PMP address lines
 - 0 = PMA<10:2> function as port I/O

bit 1-0 PTEN<1:0>: PMALH/PMALL Address Port Enable bits

- 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL⁽²⁾
- 0 = PMA1 and PMA0 pads functions as port I/O
- Note 1: The use of this pin as PMA14 or CS1 is selected by the CSF<1:0> bits in the PMCON register.
 - 2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by bits ADRMUX<1:0> in the PMCON register.

REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 ARPT<7:0>: Alarm Repeat Counter Value bits⁽²⁾ 11111111 = Alarm will trigger 256 times

0000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31.24	—	—	HR10<1:0>		HR01<3:0>				
00.40	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23:10	—		MIN10<2:0>		MIN01<3:0>				
45.0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15:8	—		SEC10<2:0>		SEC01<3:0>				
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
7:0	—	—	—	—	—		—	—	
Legend:									

REGISTER 21-3: RTCTIME: RTC TIME VALUE REGISTER

R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is

bit 31-30 Unimplemented: Read as '0'

bit 29-28 HR10<1:0>: Binary-Coded Decimal Value of Hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary-Coded Decimal Value of Hours bits, 1s place digit; contains a value from 0 to 9 bit 23 **Unimplemented:** Read as '0'

bit 22-20 MIN10<2:0>: Binary-Coded Decimal Value of Minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary-Coded Decimal Value of Minutes bits, 1s place digit; contains a value from 0 to 9 bit 15 **Unimplemented:** Read as '0'

bit 14-12 SEC10<2:0>: Binary-Coded Decimal Value of Seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary-Coded Decimal Value of Seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 Unimplemented: Read as '0'

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

x = Bit is unknown

NOTES:

TABLE 31-8:SPIX MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHA	ARACTERIS	STICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp					
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Conditions	
MSP70	TscL	SCKx Input Low Time (Note 1,2)	Tsck/2		I	ns	—	
MSP71	TscH	SCKx Input High Time (Note 1,2)	Tsck/2			ns	—	
MSP51	TssH2doZ	5		25	ns	_		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns.

TABLE 31-9: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHA	RACTERIS	TICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions		
SP70	TscL	SCKx Input Low Time (Note 1,2)	Tsck/2	_	—	ns	_		
SP71	TscH	SCKx Input High Time (Note 1,2)	Tsck/2		—	ns	—		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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