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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f256b-v-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7  $\mu F$  to 47  $\mu F$ . This capacitor should be located as close to the device as possible.

### 2.3 Capacitor on Internal Voltage Regulator (VCAP)

#### 2.3.1 INTERNAL REGULATOR MODE

A low-ESR (3 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **30.0 "Electrical Characteristics"** for additional information on CEFC specifications.

# 2.4 Master Clear (MCLR) Pin

The  $\overline{\text{MCLR}}$  pin provides two specific device functions:

- Device Reset
- Device programming and debugging

Pulling The  $\overline{\text{MCLR}}$  pin low generates a device Reset. Figure 2-2 illustrates a typical  $\overline{\text{MCLR}}$  circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the  $\overline{\text{MCLR}}$  pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.



# EXAMPLE OF MCLR PIN CONNECTIONS



**3:** No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

# 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.



#### FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX110/210 DEVICES (4 KB RAM, 16 KB FLASH)

Interrupt Source(1)	IRQ	Vector		Interrupt Bit Location						
interrupt Source <sup>v</sup>	#	#	Flag	Enable	Priority	Sub-priority	Interrupt			
U1E – UART1 Fault	39	32	IFS1<7>	IEC1<7>	IPC8<4:2>	IPC8<1:0>	Yes			
U1RX – UART1 Receive Done	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>	Yes			
U1TX – UART1 Transfer Done	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>	Yes			
I2C1B – I2C1 Bus Collision Event	42	33	IFS1<10>	IEC1<10>	IPC8<12:10>	IPC8<9:8>	Yes			
I2C1S – I2C1 Slave Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>	Yes			
I2C1M – I2C1 Master Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>	Yes			
CNA – PORTA Input Change Interrupt	45	34	IFS1<13>	IEC1<13>	IPC8<20:18>	IPC8<17:16>	Yes			
CNB – PORTB Input Change Interrupt	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>	Yes			
CNC – PORTC Input Change Interrupt	47	34	IFS1<15>	IEC1<15>	IPC8<20:18>	IPC8<17:16>	Yes			
PMP – Parallel Master Port	48	35	IFS1<16>	IEC1<16>	IPC8<28:26>	IPC8<25:24>	Yes			
PMPE – Parallel Master Port Error	49	35	IFS1<17>	IEC1<17>	IPC8<28:26>	IPC8<25:24>	Yes			
SPI2E – SPI2 Fault	50	36	IFS1<18>	IEC1<18>	IPC9<4:2>	IPC9<1:0>	Yes			
SPI2RX – SPI2 Receive Done	51	36	IFS1<19>	IEC1<19>	IPC9<4:2>	IPC9<1:0>	Yes			
SPI2TX – SPI2 Transfer Done	52	36	IFS1<20>	IEC1<20>	IPC9<4:2>	IPC9<1:0>	Yes			
U2E – UART2 Error	53	37	IFS1<21>	IEC1<21>	IPC9<12:10>	IPC9<9:8>	Yes			
U2RX – UART2 Receiver	54	37	IFS1<22>	IEC1<22>	IPC9<12:10>	IPC9<9:8>	Yes			
U2TX – UART2 Transmitter	55	37	IFS1<23>	IEC1<23>	IPC9<12:10>	IPC9<9:8>	Yes			
I2C2B – I2C2 Bus Collision Event	56	38	IFS1<24>	IEC1<24>	IPC9<20:18>	IPC9<17:16>	Yes			
I2C2S – I2C2 Slave Event	57	38	IFS1<25>	IEC1<25>	IPC9<20:18>	IPC9<17:16>	Yes			
I2C2M – I2C2 Master Event	58	38	IFS1<26>	IEC1<26>	IPC9<20:18>	IPC9<17:16>	Yes			
CTMU – CTMU Event	59	39	IFS1<27>	IEC1<27>	IPC9<28:26>	IPC9<25:24>	Yes			
DMA0 – DMA Channel 0	60	40	IFS1<28>	IEC1<28>	IPC10<4:2>	IPC10<1:0>	No			
DMA1 – DMA Channel 1	61	41	IFS1<29>	IEC1<29>	IPC10<12:10>	IPC10<9:8>	No			
DMA2 – DMA Channel 2	62	42	IFS1<30>	IEC1<30>	IPC10<20:18>	IPC10<17:16>	No			
DMA3 – DMA Channel 3	63	43	IFS1<31>	IEC1<31>	IPC10<28:26>	IPC10<25:24>	No			
		Lowes	st Natural O	rder Priority						

#### TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

#### REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

bit 3	CF: Clock Fail Detect bit
	1 = FSCM has detected a clock failure
	0 = No clock failure has been detected
bit 2	UFRCEN: USB FRC Clock Enable bit <sup>(1)</sup>
	<ul> <li>1 = Enable the FRC as the clock source for the USB clock source</li> <li>0 = Use the Primary Oscillator or USB PLL as the USB clock source</li> </ul>
bit 1	SOSCEN: Secondary Oscillator (Sosc) Enable bit
	1 = Enable the Secondary Oscillator
	0 = Disable the Secondary Oscillator
bit 0	OSWEN: Oscillator Switch Enable bit
	<ul> <li>1 = Initiate an oscillator switch to selection specified by NOSC&lt;2:0&gt; bits</li> <li>0 = Oscillator switch is complete</li> </ul>
Note 1:	This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit         Bit         Bit           5         29/21/13/5         28/20/12/4         27/19/11/3		Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0						
	U-0	R/W-0	R/W-0	R/W-0	R/W-0									
31:24	—	RODIV<14:8> <sup>(1,3)</sup>												
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
23:16	RODIV<7:0> <sup>(1,3)</sup>													
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC						
15:8	ON	_	SIDL	OE	RSLP <sup>(2)</sup>	-	DIVSWEN	ACTIVE						
	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0						
7:0		_	_	_	ROSEL<3:0> <sup>(1)</sup>									

#### **REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

Legend:	HC = Hardware Clearable	HS = Hardware Settable				
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31 Unimplemented: Read as '0'

bit 30-16	RODIV<14:0> Reference Clock Divider bits <sup>(1,3)</sup>
	The value selects the reference clock divider bits. See Figure 8-1 for information.
bit 15	ON: Output Enable bit
	1 = Reference Oscillator module is enabled
	0 = Reference Oscillator module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Peripheral Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
  - 0 =Continue module operation when the device enters lide mode
- bit 12 **OE:** Reference Clock Output Enable bit
  - 1 = Reference clock is driven out on REFCLKO pin
  - 0 = Reference clock is not driven out on REFCLKO pin
- bit 11 RSLP: Reference Oscillator Module Run in Sleep bit<sup>(2)</sup>
  - 1 = Reference Oscillator module output continues to run in Sleep
  - 0 = Reference Oscillator module output is disabled in Sleep
- bit 10 Unimplemented: Read as '0'
- bit 9 DIVSWEN: Divider Switch Enable bit
  - 1 = Divider switch is in progress
    - 0 = Divider switch is complete
- bit 8 ACTIVE: Reference Clock Request Status bit
  - 1 = Reference clock request is active
  - 0 = Reference clock request is not active
- bit 7-4 Unimplemented: Read as '0'
- **Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
  - **2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
  - 3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
	ROTRIM<8:1>												
22:16	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0					
23:10	ROTRIM<0>	—	—	—	—	—	—	—					
45.0	U-0	R-0	U-0	U-0 U-0		U-0	U-0	U-0					
15:8	—	_	_	_	_	_	—	—					
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
7:0	_	_	_	_	_	_	_	_					

#### REGISTER 8-4: REFOTRIM: REFERENCE OSCILLATOR TRIM REGISTER

#### Legend:

Logonal							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-23 ROTRIM<8:0>: Reference Oscillator Trim bits

**Note:** While the ON (REFOCON<15>) bit is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

### 10.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 27. "USB On-The-Go (OTG)" (DS60001126), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 Full-Speed and Low-Speed embedded host, Full-Speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 10-1.

The clock generator provides the 48 MHz clock required for USB Full-Speed and Low-Speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module. The PIC32 USB module includes the following features:

- · USB Full-Speed support for Host and Device
- Low-Speed Host support
- USB OTG support
- · Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- · Transaction handshaking performed by hardware
- · Endpoint buffering anywhere in system RAM
- · Integrated DMA to access system RAM and Flash
- Note: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc., also referred to as USB-IF (www.usb.org). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

#### REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)

- bit 1 CRC5EF: CRC5 Host Error Flag bit<sup>(4)</sup>
  - 1 = Token packet rejected due to CRC5 error
  - 0 = Token packet accepted
  - EOFEF: EOF Error Flag bit<sup>(3,5)</sup>
  - 1 = An EOF error condition was detected
  - 0 = No EOF error condition was detected
- bit 0 PIDEF: PID Check Failure Flag bit
  - 1 = PID check failed
  - 0 = PID check passed
- **Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
  - **2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
  - **3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
  - 4: Device mode.
  - 5: Host mode.

#### **INPUT CAPTURE** 15.0

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 15. "Input Capture" (DS60001122), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- · Simple capture event modes:
  - Capture timer value on every rising and falling edge of input at ICx pin
  - Capture timer value on every edge (rising and falling)
  - Capture timer value on every edge (rising and falling), specified edge first.

- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- · Device wake-up from capture pin during Sleep and Idle modes
- · Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- · Input capture can also be used to provide additional sources of external interrupts

Figure 15-1 illustrates a general block diagram of the Input Capture module.



### FIGURE 18-1: I<sup>2</sup>C BLOCK DIAGRAM



Bit Range	Bit Bit 31/23/15/7 30/22/14/6		Bit Bit 29/21/13/5 28/20/12/4		Bit 27/19/11/3	Bit Bit 7/19/11/3 26/18/10/2		Bit 24/16/8/0					
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
31:24		YEAR1	0<3:0>		YEAR01<3:0>								
00.40	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
23:16	—	—	—	MONTH10	MONTH01<3:0>								
15.9	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
15:8	_	—	DAY1	)<1:0>	DAY01<3:0>								
7.0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x					
7:0	—	_	—	—	— WDAY01<2:0>								
	•												
Legend:													
R = Read	lable bit		W = Writable	e bit	U = Unimplemented bit, read as '0'								
-n = Value	e at POR		'1' = Bit is se	et	'0' = Bit is cleared x = Bit is unknown								

### REGISTER 21-4: RTCDATE: RTC DATE VALUE REGISTER

bit 31-28 YEAR10<3:0>: Binary-Coded Decimal Value of Years bits, 10s place digit; contains a value from 0 to 9

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1s place digit; contains a value from 0 to 9 bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MONTH10:** Binary-Coded Decimal Value of Months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9 bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 DAY10<1:0>: Binary-Coded Decimal Value of Days bits, 10s place digit; contains a value of 0 to 3

bit 11-8 DAY01<3:0>: Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 WDAY01<2:0>: Binary-Coded Decimal Value of Weekdays bits; contains a value from 0 to 6

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).

Bit Range	Bit Bit Bit Range 31/23/15/7 30/22/14/6		Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	—	—	_	—	_	—	—	—	
45.0	R/W-0	U-0 U-0		U-0	U-0	U-0	U-0	U-0	
15:8	ON <sup>(1)</sup>	—	—	—	—	—	—	—	
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0 R/W-0		R/W-0	R/W-0	
7:0	_	CVROE	CVRR	CVRSS		CVR	<3:0>		

#### **REGISTER 24-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Comparator Voltage Reference On bit<sup>(1)</sup>
  - 1 = Module is enabled
    - Setting this bit does not affect other bits in the register.
  - 0 = Module is disabled and does not consume current.
    - Clearing this bit does not affect the other bits in the register.
- bit 14-7 Unimplemented: Read as '0'
- bit 6 **CVROE:** CVREFOUT Enable bit
  - 1 = Voltage level is output on CVREFOUT pin
  - 0 = Voltage level is disconnected from CVREFOUT pin
- bit 5 CVRR: CVREF Range Selection bit
  - 1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size
  - 0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size
- bit 4 **CVRSS:** CVREF Source Selection bit
  - 1 = Comparator voltage reference source, CVRSRC = (VREF+) (VREF-)
  - 0 = Comparator voltage reference source, CVRSRC = AVDD AVSS
- bit 3-0 **CVR<3:0>:** CVREF Value Selection  $0 \le CVR<3:0> \le 15$  bits

<u>When CVRR = 1:</u> CVREF = (CVR<3:0>/24) • (CVRSRC) <u>When CVRR = 0:</u> CVREF = 1/4 • (CVRSRC) + (CVR<3:0>/32) • (CVRSRC)

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

### 27.2 Configuration Registers

### TABLE 27-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

ess				Bits													í		
Virtual Addr (BFC0_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
	ADE 0 DE VOE 00 31:1	31:16	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	_	-	—	—	—	—	—	_	—	_	-	_	xxxx
0BF0 D	DEVCEGS	15:0		USERID<15:0> xxx											xxxx				
		31:16	—	—	_	—	—	-	-	—	—	—	—	_	—	FP	LLODIV<2:(	)>	xxxx
UDF4	DEVCFG2	15:0	UPLLEN <sup>(1)</sup>	—	_	—	—	UPL	LIDIV<2:0>	<b>_</b> (1)	—	FF	PLLMUL<2:	)>	—	FF	PLLIDIV<2:0	>	xxxx
		31:16	—	—	_	—	—	-	FWDTWI	NSZ<1:0>	FWDTEN	WINDIS	—		١	NDTPS<4:0	>		XXXX
UDFO	DEVCEGI	15:0	FCKSM	<1:0>	FPBD	IV<1:0>	—	OSCIOFNC	POSCM	OD<1:0>	IESO	—	FSOSCEN	CEN — FNOSC		NOSC<2:0>	•	XXXX	
0BFC DEVC		31:16	—	—	_	CP	—	-	-	BWP	—	—	—	_	—	F	WP<8:6>(2)		XXXX
	DEVCEGO	15:0			PWP<	:5:0>			_	_	_	_	_	ICESE	L<1:0>	JTAGEN	DEBUG	6<1:0>	XXXX

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on PIC32MX2XX devices.

2: PWP<8:7> are only available on devices with 256 KB of Flash.

### TABLE 27-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

ess										В	its								(E
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets <sup>(</sup>
F000		31:16		VER	<3:0>							DEVID	<27:16>						xxxx <sup>(1</sup>
F220	DEVID	15:0								DEVID	<15:0>								xxxx <sup>(1</sup>
F000		31:16	_	_	_	—	_	_	_	_	_	_	_	_	_	_	_	_	0000
F200	CFGCON	15:0	_	—	IOLOCK	PMDLOCK	_	_	_	_	_	_	_	_	JTAGEN	_	_	TDOEN	000B
F020	OVOKEV(3)	31:16								SAGKE.	V<31.05								0000
F230	STORET	15:0								STORE	1~51.02								0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	—	_	—	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	_	—	—	—	—	—	_	—
45.0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
15:8	—	—	IOLOCK <sup>(1)</sup>	PMDLOCK <sup>(1)</sup>	—	—		_
7.0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-1	R/W-1
7:0	—	_	_	_	JTAGEN	_		TDOEN

#### **REGISTER 27-5: CFGCON: CONFIGURATION CONTROL REGISTER**

#### Legend:

Logonan			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-14 Unimplemented: Read as '0'

- bit 13 IOLOCK: Peripheral Pin Select Lock bit<sup>(1)</sup>
  - 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
  - 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.
- bit 12 PMDLOCK: Peripheral Module Disable bit<sup>(1)</sup>
  - 1 = Peripheral module is locked. Writes to PMD registers is not allowed.
  - 0 = Peripheral module is not locked. Writes to PMD registers is allowed.

#### bit 11-4 Unimplemented: Read as '0'

- bit 3 JTAGEN: JTAG Port Enable bit
  - 1 = Enable the JTAG port
    - 0 = Disable the JTAG port
- bit 2-1 Unimplemented: Read as '1'
- bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG bit
  - 1 = 2-wire JTAG protocol uses TDO
  - 0 = 2-wire JTAG protocol does not use TDO
- Note 1: To change this bit, the unlock sequence must be performed. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.





#### TABLE 30-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				<b>Standar</b> (unless Operatir	d Operating Condition otherwise stated) ng temperature -40°C -40°C	I <b>IS: 2.3V</b> C ≤ TA ≤ C ≤ TA ≤	<b>/ to 3.6</b> ( +85°C ( +105°	<b>V</b> 5 for Industrial C for V-temp	
Param. No.	Symbol	Characteristics <sup>(1)</sup>		Min.	Max.	Units	Condi	tions	
TB10	ТтхН	TxCK High Time	Synchron prescaler	ous, with	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8,
TB11	ΤτχL	TxCK Low Time	Synchron prescaler	ous, with	[(12.5 ns or 1 ТРВ)/N] + 25 ns	_	ns	Must also meet parameter TB15	16, 32, 64, 256)
TB15	T⊤xP	TxCK Input	Synchron prescaler	ous, with	[(Greater of [(25 ns or 2 Трв)/N] + 30 ns	_	ns	VDD > 2.7V	
		Period			[(Greater of [(25 ns or 2 Трв)/N] + 50 ns	_	ns	VDD < 2.7V	
TB20	TCKEXTMRL	Delay from Clock Edge	External T e to Timer I	xCK ncrement	—	1	Трв	_	-

Note 1: These parameters are characterized, but not tested in manufacturing.

#### FIGURE 30-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



#### TABLE 30-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHA	RACTERI	STICS	Standard O (unless oth Operating te	$\begin{array}{ll} \mbox{perating Conditions: 2.3V} \\ \mbox{erwise stated}) \\ \mbox{ermperature} & -40^{\circ}C \leq TA \leq + \\ -40^{\circ}C \leq TA \leq + \end{array}$	<b>to 3.6V</b> 85°C foi 105°C fo	<sup>-</sup> Industri or V-tem	al p	
Param. No.	Symbol	Charac	cteristics <sup>(1)</sup>	Min.	Max.	Units	Con	ditions
IC10	TccL	ICx Input	t Low Time	[(12.5 ns or 1 ТРВ)/N] + 25 ns	_	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	ТссН	ICx Input	t High Time	[(12.5 ns or 1 ТРВ)/N] + 25 ns	_	ns	Must also meet parameter IC15.	
IC15	TCCP	ICx Input	t Period	[(25 ns or 2 Трв)/N] + 50 ns	_	ns	_	

Note '	1:	These	parameters a	are charac	terized, bu	it not f	tested in	manufacturing	
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#### TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section	Update Description
4.0 "Memory Organization"	Added Memory Maps for the new devices (see Figure 4-3 and Figure 4-4).
	Removed the BMXCHEDMA bit from the Bus Matrix Register map (see Table 4-1).
	Added the REFOTRIM register, added the DIVSWEN bit to the REFOCON registers, added Note 4 to the ULOCK and SOSCEN bits and added the PBDIVRDY bit in the OSCCON register in the in the System Control Register map (see Table 4-16).
	Removed the ALTI2C1 and ALTI2C2 bits from the DEVCFG3 register and added Note 1 to the UPLLEN and UPLLIDIV<2:0> bits of the DEVCFG2 register in the Device Configuration Word Summary (see Table 4-17).
	Updated Note 1 in the Device and Revision ID Summary (see Table 4-18).
	Added Note 2 to the PORTA Register map (see Table 4-19).
	Added the ANSB6 and ANSB12 bits to the ANSELB register in the PORTB Register map (see Table 4-20).
	Added Notes 2 and 3 to the PORTC Register map (see Table 4-21).
	Updated all register names in the Peripheral Pin Select Register map (see Table 4-23).
	Added values in support of new devices (16 KB RAM and 32 KB RAM) in the Data RAM Size register (see Register 4-5).
	Added values in support of new devices (64 KB Flash and 128 KB Flash) in the Data RAM Size register (see Register 4-5).
8.0 "Oscillator Configuration"	Added Note 5 to the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1).
	Added the PBDIVRDY bit and Note 2 to the Oscillator Control register (see Register 8-1).
	Added the DIVSWEN bit and Note 3 to the Reference Oscillator Control register (see Register 8-3).
	Added the REFOTRIM register (see Register 8-4).
21.0 "10-bit Analog-to-Digital	Updated the ADC1 Module Block Diagram (see Figure 21-1).
Converter (ADC)"	Updated the Notes in the ADC Input Select register (see Register 21-4).
24.0 "Charge Time Measurement	Updated the CTMU Block Diagram (see Figure 24-1).
	Added Note 3 to the CTMU Control register (see Register 24-1)
26.0 "Special Features"	Added Note 1 and the PGEC4/PGED4 pin pair to the ICESEL<1:0> bits in DEVCFG0: Device Configuration Word 0 (see Register 26-1).
	Removed the ALTI2C1 and ALTI2C2 bits from the Device Configuration Word 3 register (see Register 26-4).
	Removed 26.3.3 "Power-up Requirements".
	Added Note 3 to the Connections for the On-Chip Regulator diagram (see Figure 26-2).
	Updated the Block Diagram of Programming, Debugging and Trace Ports diagram (see Figure 26-3).

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Start Address)	97
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DCHxSPTR (DMA Channel 'x' Source Pointer)	9
DCHxSSA (DMA Channel 'x' Source Start Address) 9	7
DCHxSSIZ (DMA Channel 'x' Source Size) 9	8
DCRCCON (DMA CRC Control)9	0
DCRCDATA (DMA CRC Data)9	2
DCRCXOR (DMA CRCXOR Enable)	2
DEVCFG0 (Device Configuration Word 0) 24	1
DEVCFG1 (Device Configuration Word 1) 24	3
DEVCFG2 (Device Configuration Word 2)	5
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DMACON (DMA Controller Control) 8	8
DMASTAT (DMA Status)	a
12CxCON (12C Control)	6
12CxSTAT (12C Status) 17	'a
ICVCON (Input Conture 'v' Control)	0
ICXCON (Input Captule X Control)	9
IECX (Interrupt Enable Control)	0
IFSX (Interrupt Flag Status)	0
INTCON (Interrupt Control)	8
INTSTAT (Interrupt Status)	9
IPCx (Interrupt Priority Control)7	1
IPTMR (Interrupt Proximity Timer)6	9
NVMADDR (Flash Address) 5	6
NVMCON (Programming Control) 5	5
NVMDATA (Flash Program Data) 5	7
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NVMSRCADDR (Source Data Address) 5	7
OCxCON (Output Compare 'x' Control) 16	3
OSCCON (Oscillator Control)7	6
OSCTUN (FRC Tuning)7	9
PMADDR (Parallel Port Address) 19	5
, ,	
PMAEN (Parallel Port Pin Enable) 19	6
PMAEN (Parallel Port Pin Enable)	6 1
PMAEN (Parallel Port Pin Enable)	6 1 3
PMAEN (Parallel Port Pin Enable)	6 1 3 7
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         REFOCON (Reference Oscillator Control)       8	6 1 3 7
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8	6 1 3 7 0 2
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14	6137021
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         PREFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6	61370212
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         PREFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCAL RM (RTC Alarm Control)       20	613702123
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         PREFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20	
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCCOATE (RTC Date Value)       20	61370212316
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         PMSTAT (Parallel Port Status (Slave Modes Only)       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCDATE (RTC Date Value)       20         RTCTIME (RTC Time Value)       20	613702123165
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCDATE (RTC Date Value)       20         RTCTIME (RTC Time Value)       20         RTCTIME (RTC Time Value)       20	6137021231657
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PREFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCON (RTC Control)       20         RTCDATE (RTC Date Value)       20         RTCTIME (RTC Time Value)       20         SPIXCON (SPI Control)       16         SPIXCON2 (SPI Control)       17	61370212316570
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCON (RTC Control)       20         RTCDATE (RTC Date Value)       20         RTCTIME (RTC Time Value)       20         SPIXCON (SPI Control)       16         SPIXCON2 (SPI Control 2)       17	613702123165701
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PREFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCON (RTC Control)       20         RTCDATE (RTC Date Value)       20         RTCIME (RTC Time Value)       20         SPIXCON (SPI Control)       16         SPIXCON2 (SPI Control 2)       17         SPIXSTAT (SPI Status)       17         SPIXSTAT (SPI Status)       17	6137021231657015
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCTIME (RTC Time Value)       20         RTCTIME (RTC Time Value)       20         SPIxCON (SPI Control)       16         SPIxCON2 (SPI Control)       17         SPIXSTAT (SPI Status)       17         T1CON (Type A Timer Control)       14	61370212316570150
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PREFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCTIME (RTC Time Value)       20         RTCTIME (RTC Time Value)       20         SPIxCON (SPI Control)       16         SPIxCON2 (SPI Control 2)       17         SPIxSTAT (SPI Status)       17         T1CON (Type A Timer Control)       14         TXCON (Type B Timer Control)       15	613702123165701501
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PREFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCTIME (RTC Date Value)       20         RTCIME (RTC Time Value)       20         SPIXCON (SPI Control)       16         SPIXCON2 (SPI Control)       17         SPIXSTAT (SPI Status)       17         T1CON (Type A Timer Control)       14         TXCON (USB Address)       12         U1ADDR (USB Address)       12	613702123165701501
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCTIME (RTC Time Value)       20         RTCIME (RTC Time Value)       20         SPIxCON (SPI Control)       16         SPIxCON (SPI Control)       17         SPIxSTAT (SPI Status)       17         T1CON (Type A Timer Control)       14         TXCON (Type B Timer Control)       14         TADDR (USB Address)       12         U1BDTP1 (USB BDT Page 1)       12	6137021231657015013
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCCATE (RTC Date Value)       20         RTCIME (RTC Time Value)       20         SPIxCON (SPI Control)       16         SPIxCON (SPI Control 2)       17         SPIxSTAT (SPI Status)       17         T1CON (Type A Timer Control)       14         TXCON (Type B Timer Control)       15         U1ADDR (USB Address)       12         U1BDTP1 (USB BDT Page 1)       12         U1BDTP2 (USB BDT Page 2)       12	61370212316570150134
PMAEN (Parallel Port Pin Enable)       19         PMCON (Parallel Port Control)       19         PMMODE (Parallel Port Mode)       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         PMSTAT (Parallel Port Status (Slave Modes Only).       19         REFOCON (Reference Oscillator Control)       8         REFOTRIM (Reference Oscillator Trim)       8         RPnR (Peripheral Pin Select Output)       14         RSWRST (Software Reset)       6         RTCALRM (RTC Alarm Control)       20         RTCCON (RTC Control)       20         RTCCATE (RTC Date Value)       20         RTCTIME (RTC Time Value)       20         SPIxCON (SPI Control)       16         SPIxCON (SPI Control)       17         SPIxCON (SPI Control 2)       17         SPIxSTAT (SPI Status)       17         T1CON (Type A Timer Control)       14         TXCON (Type B Timer Control)       14         TXCON (Type B Timer Control)       15         U1ADDR (USB Address)       12         U1BDTP1 (USB BDT Page 1)       12         U1BDTP3 (USB BDT Page 2)       12         U1BDT21 (UBB BDT Page 3)       12	613702123165701501344
PMAEN (Parallel Port Pin Enable)19PMCON (Parallel Port Control)19PMMODE (Parallel Port Mode)19PMSTAT (Parallel Port Status (Slave Modes Only)19REFOCON (Reference Oscillator Control)8REFOTRIM (Reference Oscillator Control)8REFOTRIM (Reference Oscillator Trim)8RPnR (Peripheral Pin Select Output)14RSWRST (Software Reset)6RTCALRM (RTC Alarm Control)20RTCCON (RTC Control)20RTCCATE (RTC Date Value)20RTCTIME (RTC Time Value)20SPIxCON (SPI Control)16SPIxCON (SPI Control)16SPIxCON (SPI Control)17SPIxSTAT (SPI Status)17T1CON (Type A Timer Control)14TxCON (Type B Timer Control)15U1ADDR (USB Address)12U1BDTP1 (USB BDT Page 1)12U1BDTP3 (USB BDT Page 3)12U1CNFG1 (USB Configuration 1)12	6137021231657015013445
PMAEN (Parallel Port Pin Enable)19PMCON (Parallel Port Control)19PMMODE (Parallel Port Mode)19PMSTAT (Parallel Port Status (Slave Modes Only)19REFOCON (Reference Oscillator Control)8REFOTRIM (Reference Oscillator Control)8RPnR (Peripheral Pin Select Output)14RSWRST (Software Reset)6RTCALRM (RTC Alarm Control)20RTCCON (RTC Control)20RTCCDATE (RTC Date Value)20RTCTIME (RTC Time Value)20SPIxCON (SPI Control)16SPIxCON2 (SPI Control)16SPIxCON2 (SPI Control 2)17SPIxSTAT (SPI Status)17T1CON (Type A Timer Control)14TxCON (Type B Timer Control)14TxCON (USB Address)12U1BDTP1 (USB BDT Page 1)12U1BDTP3 (USB BDT Page 3)12U1CNFG1 (USB Configuration 1)12U1CON (USB Control)11	61370212316570150134459
PMAEN (Parallel Port Pin Enable)19PMCON (Parallel Port Control)19PMMODE (Parallel Port Mode)19PMSTAT (Parallel Port Status (Slave Modes Only)19REFOCON (Reference Oscillator Control)8REFOTRIM (Reference Oscillator Control)8RPnR (Peripheral Pin Select Output)14RSWRST (Software Reset)6RTCALRM (RTC Alarm Control)20RTCCON (RTC Control)20RTCCDATE (RTC Date Value)20RTCTIME (RTC Time Value)20SPIxCON (SPI Control)16SPIxCON2 (SPI Control 2)17SPIxSTAT (SPI Status)17T1CON (Type A Timer Control)14TxCON (Type B Timer Control)15U1ADDR (USB Address)12U1BDTP1 (USB BDT Page 1)12U1BDTP3 (USB BDT Page 3)12U1CNFG1 (USB Configuration 1)11U1CN (USB Control)11	613702123165701501344597
PMAEN (Parallel Port Pin Enable)19PMCON (Parallel Port Control)19PMMODE (Parallel Port Mode)19PMSTAT (Parallel Port Status (Slave Modes Only)19REFOCON (Reference Oscillator Control)8REFOTRIM (Reference Oscillator Control)8RPnR (Peripheral Pin Select Output)14RSWRST (Software Reset)6RTCALRM (RTC Alarm Control)20RTCCON (RTC Control)20RTCCON (RTC Control)20RTCTIME (RTC Time Value)20SPIxCON (SPI Control)16SPIxCON2 (SPI Control 2)17SPIxSTAT (SPI Status)17T1CON (Type A Timer Control)14TxCON (Type B Timer Control)14TxCON (USB Address)12U1BDTP1 (USB BDT Page 1)12U1BDTP3 (USB BDT Page 3)12U1CNFG1 (USB Configuration 1)11U1EIR (USB Error Interrupt Enable)11U1EIR (USB Error Interrupt Status)11	6137021231657015013445975
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# **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PIC32 MX 1XX F 032 D B T - 501/PT - XXX       Example:         Microchip Brand	
	Flash Memory Family
Architecture	$MX = M4K^{\odot} MCU \text{ core}$
Product Groups	1XX = General purpose microcontroller family 2XX = General purpose microcontroller family
Flash Memory Family	F = Flash program memory
Program Memory Size	016 = 16K 032 = 32K 064 = 64K 128 = 128K 256 = 256K
Pin Count	B = 28-pin C = 36-pin D = 44-pin
Software Targeting	B = Targeted for Bluetooth <sup>®</sup> Audio Break-in devices
Speed	<ul> <li>= 40 MHz - () indicates a blank field; package markings for 40 MHz devices do not include the Speed</li> <li>= 50 MHz</li> </ul>
Temperature Range	I = $-40^{\circ}$ C to $+85^{\circ}$ C (Industrial) V = $-40^{\circ}$ C to $+105^{\circ}$ C (V-temp)
Package	ML= 28-Lead (6x6 mm) QFN (Plastic Quad Flatpack)ML= 44-Lead (8x8 mm) QFN (Plastic Quad Flatpack)PT= 44-Lead (10x10x1 mm) TQFP (Plastic Thin Quad Flatpack)SO= 28-Lead (7.50 mm) SOIC (Plastic Small Outline)SP= 28-Lead (300 mil) SPDIP (Skinny Plastic Dual In-line)SS= 28-Lead (5.30 mm) SSOP (Plastic Shrink Small Outline)TL= 36-Lead (5x5 mm) VTLA (Very Thin Leadless Array)TL= 44-Lead (6x6 mm) VTLA (Very Thin Leadless Array)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample

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