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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f256b-v-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

		Pin Nu	mber ⁽¹⁾						
Pin Name	28-pin QFN	28-pin 44-pin 28-pin SSOP/ 36-pin QFN/ QFN SPDIP/ VTLA TQFP/ SOIC VTLA		Pin Type	Buffer Type	Description			
MCLR	26	1	32	18	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.		
AVDD	25	28	31	17	Р	_	Positive supply for analog modules. Th pin must be connected at all times.		
AVss	24	27	30	16	Р	—	Ground reference for analog modules		
Vdd	10	13	5, 13, 14, 23	28, 40	Р	—	Positive supply for peripheral logic and I/O pins		
VCAP	17	20	22	7	Р	—	CPU logic filter capacitor connection		
Vss	5, 16	8, 19	6, 12, 21	6, 29, 39	Р	—	Ground reference for logic and I/O pins. This pin must be connected at all times.		
VREF+	27	2	33	19	I	Analog	Analog voltage reference (high) input		
VREF-	28	3	34	20	I	Analog	Analog voltage reference (low) input		
Legend:	CMOS = CMOS compatible input or output ST = Schmitt Trigger input with CMOS levels				Analog = O = Outp	Analog input P = Power ut I = Input			

TADI E 4 4. DINOUT I/O DESCRIPTIONS (CONTINUED)

ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer

Analog = Analog input	P = Powe
O = Output	l = Input
PPS = Peripheral Pin Select	— = N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

Exception	Description
Reset	Assertion MCLR or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Вр	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

TABLE 3-3: MIPS32[®] M4K[®] PROCESSOR CORE EXCEPTION TYPES

3.3 Power Management

The MIPS M4K processor core offers many power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see Section 26.0 "Power-Saving Features".

3.4 EJTAG Debug Support

The MIPS M4K processor core provides an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
31.24	NVMKEY<31:24>										
00.10	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
23:10	NVMKEY<23:16>										
45.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
15:8	NVMKEY<15:8>										
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
7:0		NVMKEY<7:0>									

REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMKEY<31:0>: Unlock Register bits

These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31:24	NVMADDR<31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:10	NVMADDR<23:16>								
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
10.0	NVMADDR<15:8>								
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0				NVMA	DR<7:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMADDR<31:0>: Flash Address bits

Bulk/Chip/PFM Erase: Address is ignored. Page Erase: Address identifies the page to erase. Row Program: Address identifies the row to program. Word Program: Address identifies the word to program.

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

(1)	IRQ	Vector #		Persistent			
Interrupt Source ⁽¹⁾	#		Flag	Enable	Priority	Sub-priority	Interrupt
		Highes	st Natural O	rder Priority	,		
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1E – SPI1 Fault	36	31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1TX – SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTE	CEGISTER 9-8. DCHXECON: DMA CHANNEL X EVENT CONTROL REGISTER									
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31.24	—	—	—	_	—	—	—	—		
22:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1		
23.10	CHAIRQ<7:0> ⁽¹⁾									
15.0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1		
10.0	CHSIRQ<7:0> ⁽¹⁾									
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0		
7:0	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN					

CISTER 0-8. CIETED

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 Unimplemented: Read as '0'

bit

bit

bit

bit

bit

bit

31-24	Unimplemented. Read as 0
23-16	CHAIRQ<7:0>: Channel Transfer Abort IRQ bits ⁽¹⁾
	11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
	•
	•
	00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag 00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag
15-8	CHSIRQ<7:0>: Channel Transfer Start IRQ bits ⁽¹⁾
	11111111 = Interrupt 255 will initiate a DMA transfer
	•
	•
	•
	00000001 = Interrupt 0 will initiate a DMA transfer
7	CEORCE: DMA Forced Transfer bit
1	
	 1 = A DMA transfer is forced to begin when this bit is written to a '1' 0 = This bit always reads '0'
6	CABORT: DMA Abort Transfer bit
	1 = A DMA transfer is aborted when this bit is written to a '1'
	0 = This bit always reads '0'
5	PATEN: Channel Pattern Match Abort Enable bit
	1 = Abort transfer and clear CHEN on pattern match
	0 = Pattern match is disabled
4	SIRQEN: Channel Start IRQ Enable bit
	1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

- - 0 = Interrupt number CHSIRQ is ignored and does not start a transfer
- bit 3 AIRQEN: Channel Abort IRQ Enable bit
 - 1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
 - 0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer
- bit 2-0 Unimplemented: Read as '0'
- Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

TABLE 10-1: USB REGISTER MAP (CONTINUED)

ess											Bit	s							
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5390	LI1EP9	31:16	—	—	—	—	—	—	-		_	_	—	—	—	-	—	—	0000
0000	UTER 9	15:0	_	—	—	—		—	_	—	_		—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5340		31:16	_	—	—	—	—	—	_	—	_	_	—		_	_	—		0000
5570	UTEL TO	15:0	-	—	_	—	_	_	-	_	_	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0		31:16		_	_	_	_	_		_			_	—			_	—	0000
5560	UILFII	15:0		—	_	_	_	_		_	-	-	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5300		31:16		_	_	_	_	_		_			_	—			_	—	0000
5500	UILF 12	15:0		—	_	_	_	_		_	-	-	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5200		31:16		—	_	_	_	_		_	-	-	_	—		-		—	0000
5500	UILF 13	15:0		—	_	_	_	_		_	-	-	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_	_	_	_	_	_	_	_	_	_	—	_	_	_	—	0000
53E0	UTEP14	15:0	_	_		_			_		_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_		_			_		_	_	_	_	_	_	_	—	0000
53FU	UTEP15	15:0	_						_			-		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

sss										В	its								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5000	DD00D(1)	31:16	_	—	—	_	—	—	—	—	_	_	—	_	—	—	—	—	0000
FB8C	RPCOR	15:0	—	—	—	_	—	—	—	—	_	_	_	_		RPC8	<3:0>		0000
5000	DD00D(3)	31:16	—	_	_	_	_	_	—	_	_	—	_	—	_	_	—	_	0000
FB90	KPC9R ^{ey}	15:0	—	_	_	_	_	_	—	_	_	_	_	_		RPC9	<3:0>		0000

x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

Note 1:

2:

This register is only available on 44-pin devices. This register is only available on PIC32MX1XX devices. This register is only available on 36-pin and 44-pin devices. 3:

15.1 **Input Capture Control Registers**

AB	LE 15-1:	IN	PUT CA	PTURE	E 1-INPU		URE 5	REGIST	ER MA	2							
ess		â								Bi	ts						
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1
2000		31:16				—	—	_	—						—	—	—
2000	IC ICON.	15:0	ON		SIDL	_	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2010	IC1BUF	31:16 15:0								IC1BUF	<31:0>						
2200		31:16	_	_	_	—	—	_	—	—	_	_	-	_	—	—	_
2200	1020011	15:0	ON		SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2210	IC2BUF	31:16 15:0								IC2BUF	<31:0>						
2400		31:16	—	—	_	_	_	_	_	—	_	—	_	—	_	—	_
2400	IC3CON /	15:0	ON	_	SIDL	—	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2410	IC3BUF	31:16 15:0								IC3BUF	<31:0>						
2600		31:16	_		_	-	-		—	—	_				—	—	_
2000	1040011	15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2610	IC4BUF	31:16 15:0								IC4BUF	<31:0>						
2800		31:16	_		_	-	-		—	—	_				—	—	—
2000	1000010	15:0	ON	_	SIDL	—	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2810	IC5BUF	31:16 15:0								IC5BUF	<31:0>						

T

Legend:

This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information. Note 1:

All Resets

0000

0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx

16/0

—

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	IREN	RTSMD	—	UEN	<1:0>
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL	<1:0>	STSEL

REGISTER 19-1: UXMODE: UARTX MODE REGISTER

Legend:

Logonal			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ON: UARTx Enable bit⁽¹⁾
 - 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by the UEN<1:0> and UTXEN control bits.
 - 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal.
- bit 14 Unimplemented: Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode
- bit 12 IREN: IrDA Encoder and Decoder Enable bit
 - 1 = IrDA is enabled
 - 0 = IrDA is disabled
- bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit
 - 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
 - $0 = \overline{\text{UxRTS}}$ pin is in Flow Control mode
- bit 10 Unimplemented: Read as '0'
- bit 9-8 UEN<1:0>: UARTx Enable bits
 - 11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
 - 10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used
 - 01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
 - 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register
- bit 7 WAKE: Enable Wake-up on Start bit Detect During Sleep Mode bit
 - 1 = Wake-up enabled
 - 0 = Wake-up disabled
- bit 6 LPBACK: UARTx Loopback Mode Select bit
 - 1 = Loopback mode is enabled
 - 0 = Loopback mode is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	_	_	_	_	_	—	_	—	
45.0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	
15:8	BUSY	IRQM	<1:0>	INCM	<1:0>	—	MODE	=<1:0>	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	WAITB	<1:0>(1)		WAITM	<3:0>(1)		WAITE<1:0>(1)		

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **BUSY:** Busy bit (Master mode only)
 - 1 = Port is busy
 - 0 = Port is not busy

bit 14-13 IRQM<1:0>: Interrupt Request Mode bits

- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

bit 12-11 INCM<1:0>: Increment Mode bits

- 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾
- 01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾
- 00 = No increment or decrement of address
- bit 10 Unimplemented: Read as '0'
- bit 9-8 MODE<1:0>: Parallel Port Mode Select bits
 - 11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)
 - 10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)
 - 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
 - 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)
- bit 7-6 WAITB<1:0>: Data Setup to Read/Write Strobe Wait States bits⁽¹⁾
 - 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
 - 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
 - 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
 - 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

bit 5-2 WAITM<3:0>: Data Read/Write Strobe Wait States bits⁽¹⁾

- 1111 = Wait of 16 Трв •
- . 0001 = Wait of 2 Трв 0000 = Wait of 1 Трв (default)
- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
31:24		YEAR1	0<3:0>	1<3:0>								
00.40	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
23:16	—	—	—	MONTH10								
45.0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
15:8	_	—	DAY1)<1:0>		DAY01	<3:0>					
7.0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x				
7:0	—	—	—	—	—	— WDAY01<2:0>						
	•											
Legend:	Legend:											
R = Read	lable bit		W = Writable	e bit	U = Unimple	emented bit, re	ead as '0'					
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown					known							

REGISTER 21-4: RTCDATE: RTC DATE VALUE REGISTER

bit 31-28 YEAR10<3:0>: Binary-Coded Decimal Value of Years bits, 10s place digit; contains a value from 0 to 9

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1s place digit; contains a value from 0 to 9 bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MONTH10:** Binary-Coded Decimal Value of Months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9 bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 DAY10<1:0>: Binary-Coded Decimal Value of Days bits, 10s place digit; contains a value of 0 to 3

bit 11-8 DAY01<3:0>: Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 WDAY01<2:0>: Binary-Coded Decimal Value of Weekdays bits; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
15:8		VCFG<2:0>		OFFCAL	—	CSCNA	—	—
7.0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	BUFS			SMP	1<3:0>		BUFM	ALTS

REGISTER 22-2: AD1CON2: ADC CONTROL REGISTER 2

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-13 VCFG<2:0>: Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	AVss
001	External VREF+ pin	AVss
010	AVdd	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVss

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the sample and hold amplifier are connected to VREFL

0 = Disable Offset Calibration mode

The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 Unimplemented: Read as '0'

- bit 10 **CSCNA:** Input Scan Select bit
 - 1 = Scan inputs
 - 0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1.

1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7

0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 Unimplemented: Read as '0'

bit 5-2 SMPI<3:0>: Sample/Convert Sequences Per Interrupt Selection bits

```
1111 = Interrupts at the completion of conversion for each 16<sup>th</sup> sample/convert sequence
```

```
1110 = Interrupts at the completion of conversion for each 15<sup>th</sup> sample/convert sequence
```

- .
- •

0001 = Interrupts at the completion of conversion for each 2^{nd} sample/convert sequence 0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 BUFM: ADC Result Buffer Mode Select bit

- 1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
 - 0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 ALTS: Alternate Input Sample Mode Select bit

- 1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
- 0 = Always use Sample A input multiplexer settings

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
31:24	—	—	—	—	—	—	—	—				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
23:16	—	—	—	—	—	—	—	—				
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
15:8	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
7.0	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0				

REGISTER 22-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CSSL<15:0>: ADC Input Pin Scan Selection bits^(1,2)

1 = Select ANx for input scan

0 = Skip ANx for input scan

- **Note 1:** CSSL = ANx, where 'x' = 0-12; CSSL13 selects CTMU input for scan; CSSL14 selects IVREF for scan; CSSL15 selects Vss for scan.
 - 2: On devices with less than 13 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	_	—	—	—	—	—
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ⁽¹⁾	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	CVROE	CVRR	CVRSS		CVR	<3:0>	

REGISTER 24-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Comparator Voltage Reference On bit⁽¹⁾
 - 1 = Module is enabled
 - Setting this bit does not affect other bits in the register.
 - 0 = Module is disabled and does not consume current.
 - Clearing this bit does not affect the other bits in the register.
- bit 14-7 Unimplemented: Read as '0'
- bit 6 **CVROE:** CVREFOUT Enable bit
 - 1 = Voltage level is output on CVREFOUT pin
 - 0 = Voltage level is disconnected from CVREFOUT pin
- bit 5 CVRR: CVREF Range Selection bit
 - 1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size
 - 0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size
- bit 4 **CVRSS:** CVREF Source Selection bit
 - 1 = Comparator voltage reference source, CVRSRC = (VREF+) (VREF-)
 - 0 = Comparator voltage reference source, CVRSRC = AVDD AVSS
- bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \le CVR<3:0> \le 15$ bits

<u>When CVRR = 1:</u> CVREF = (CVR<3:0>/24) • (CVRSRC) <u>When CVRR = 0:</u> CVREF = 1/4 • (CVRSRC) + (CVR<3:0>/32) • (CVRSRC)

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

30.1 DC Characteristics

TABLE 30-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range	Temp. Range	Max. Frequency		
Characteristic	(in Volts) ⁽¹⁾	(in °C)	PIC32MX1XX/2XX 28/36/44-pin Famil		
DC5	2.3-3.6V	-40°C to +85°C	40 MHz		
DC5b	2.3-3.6V	-40°C to +105°C	40 MHz		

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
V-temp Temperature Devices					
Operating Junction Temperature Range	TJ	-40	_	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+105	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH)	PD	PINT + PI/O			W
I/O Pin Power Dissipation: I/O = S (({VDD – VOH} x IOH) + S (VOL x IOL))					
Maximum Allowed Power Dissipation	PDMAX	(TJ — TA)/θJ	A	W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 28-pin SSOP	θJA	71		°C/W	1
Package Thermal Resistance, 28-pin SOIC	θJA	50	_	°C/W	1
Package Thermal Resistance, 28-pin SPDIP	θJA	42		°C/W	1
Package Thermal Resistance, 28-pin QFN	θJA	35		°C/W	1
Package Thermal Resistance, 36-pin VTLA	θJA	31	—	°C/W	1
Package Thermal Resistance, 44-pin QFN	θJA	32		°C/W	1
Package Thermal Resistance, 44-pin TQFP	θJA	45		°C/W	1
Package Thermal Resistance, 44-pin VTLA	θJA	30	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

DC CHA	RACTERIS	TICS	$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Typical ⁽²⁾	Max.	Units	Conditions				
Power-D	Power-Down Current (IPD) (Notes 1, 5)							
DC40k	44	70	μA	-40°C				
DC40I	44	70	μA	+25°C	Pasa Power Down Current			
DC40n	168	259	μA	+85°C	Base Fower-Down Guiteni			
DC40m	335	536	μA	+105°C				
Module	Differential	Current						
DC41e	5	20	μA	3.6V	Watchdog Timer Current: AIWDT (Note 3)			
DC42e	23	50	μA	3.6V RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC (Note 3				
DC43d	1000	1100	μA	3.6V	ADC: △IADC (Notes 3,4)			

TABLE 30-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

Note 1: The test conditions for IPD current measurements are as follows:

Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)

OSC2/CLKO is configured as an I/O input pin

• USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8

• CPU is in Sleep mode, and SRAM data memory Wait states = 1

• No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set

• WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled

• All I/O pins are configured as inputs and pulled to Vss

• MCLR = VDD

• RTCC and JTAG are disabled

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- **3:** The △ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5: IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

FIGURE 30-23: EJTAG TIMING CHARACTERISTICS



TABLE 30-42: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS			Standa (unles Operat	ard Oper s otherw ing temp	ating Co vise state erature	pnditions: 2.3V to 3.6V ed) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp	
Param. No.	Symbol	Description ⁽¹⁾	Min.	Min. Max. Units		Conditions	
EJ1	Ттсксус	TCK Cycle Time	25	—	ns	—	
EJ2	Ттскнідн	TCK High Time	10	—	ns	—	
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—	
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	_	
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	-	ns	_	
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	-	5	ns	_	
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns		
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—	
EJ9	Trf	TAP Signals Rise/Fall Time, All Input and Output	_	_	ns	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES		
Dimensior	Dimension Limits		NOM	MAX
Number of Pins	Ν		28	
Pitch	е		.100 BSC	
Top to Seating Plane	Α	-	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	с	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eВ	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Dimension Limits			MAX
Number of Pins	Ν		28	
Pitch	е		0.65 BSC	
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65 3.70 4.2		
Contact Width	b	0.23 0.30 0.3		
Contact Length	L	0.50 0.55 0.70		
Contact-to-Exposed Pad	К	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units	N	IILLIMETER	S		
Dimension	Limits	MIN	NOM	MAX		
Number of Pins	N		44	-		
Number of Pins per Side	ND		12			
Number of Pins per Side	NE		10			
Pitch	е	0.50 BSC				
Overall Height	A	0.80 0.90 1.0				
Standoff	A1	0.025	-	0.075		
Overall Width	E		6.00 BSC			
Exposed Pad Width	E2	4.40	4.55	4.70		
Overall Length	D		6.00 BSC	-		
Exposed Pad Length	D2	4.40 4.55 4.70				
Contact Width	b	0.20 0.25 0.30				
Contact Length	L	0.20 0.25 0.30				
Contact-to-Exposed Pad	K	0.20	_	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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