



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f256bt-v-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 8: **PIN NAMES FOR 36-PIN USB DEVICES**

36-PIN VTLA (TOP VIEW)^(1,2,3,5)

PIC32MX210F016C

	PIC32MX220F032C PIC32MX230F064C PIC32MX250F128C		
			36
			1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	19	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	20	RPC9/CTED7/RC9
3	PGED4 ⁽⁴⁾ /AN6/RPC0/RC0	21	Vss
4	PGEC4 ⁽⁴⁾ /AN7/RPC1/RC1	22	VCAP
5	VDD	23	Vdd
6	Vss	24	PGED2/RPB10/D+/CTED11/RB10
7	OSC1/CLKI/RPA2/RA2	25	PGEC2/RPB11/D-/RB11
8	OSC2/CLKO/RPA3/PMA0/RA3	26	VUSB3V3
9	SOSCI/RPB4/RB4	27	AN11/RPB13/CTPLS/PMRD/RB13
10	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	28	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14
11	AN12/RPC3/RC3	29	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
12	Vss	30	AVss
13	DD	31	AVdd
14	DD	32	MCLR
15	TMS/RPB5/USBID/RB5	33	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
16	VBUS	34	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1
17	TDI/RPB7/CTED3/PMD5/INT0/RB7	35	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0
18	TCK/RPB8/SCL1/CTED10/PMD4/RB8	36	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1
		L	

Note The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin 1: Select" for restrictions.

Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information. 2:

The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally. 3:

4: This pin function is not available on PIC32MX210F016C and PIC32MX120F032C devices.

5: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

2.8.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- COUT = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e.,12 mm length) = 2.5 pF

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION



The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

- Select a crystal with a lower "minimum" power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing "ESR" rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.
- Note: Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, RS, as shown in circuit "C" in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to ~VDD-0.6V. When measuring the oscillator signal you must use a FET scope probe or a probe with ≤ 1.5 pF or the scope probe itself will unduly change the gain and peak-to-peak levels.

2.8.1.1 Additional Microchip References

- AN588 "PICmicro[®] Microcontroller Oscillator Design Guide"
- AN826 "Crystal Oscillator Basics and Crystal Selection for rfPIC[™] and PICmicro[®] Devices"
- AN849 "Basic PICmicro[®] Oscillator Design"





FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 64 KB FLASH)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R	R	R	R	R	R	R	R		
31:24	BMXPFMSZ<31:24>									
22:46	R	R	R	R	R	R	R	R		
23.10	BMXPFMSZ<23:16>									
45.0	R	R	R	R	R	R	R	R		
15:8	BMXPFMSZ<15:8>									
7:0	R	R	R	R	R	R	R	R		
				BMXPF	MSZ<7:0>					

REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BMXPFMSZ<31:0>: Program Flash Memory (PFM) Size bits

Static value that indicates the size of the PFM in bytes: 0x00004000 = Device has 16 KB Flash 0x00008000 = Device has 32 KB Flash 0x00010000 = Device has 64 KB Flash 0x00020000 = Device has 128 KB Flash 0x00040000 = Device has 256 KB Flash

REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	R	R	R	R	R	R	R	R		
31:24				BMXBOO	TSZ<31:24>					
22.16	R	R	R	R	R	R	R	R		
23.10	BMXBOOTSZ<23:16>									
45.0	R	R	R	R	R	R	R	R		
15:8	BMXBOOTSZ<15:8>									
7:0	R	R	R	R	R	R	R	R		
				BMXBO	OTSZ<7:0>					

Legend:					
R = Readable bit	e bit W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits Static value that indicates the size of the Boot PFM in bytes: 0x00000C00 = Device has 3 KB boot Flash

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31.24		NVMDATA<31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23:10	NVMDATA<23:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	NVMDATA<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				NVMD	ATA<7:0>					

REGISTER 5-4: NVMDATA: FLASH PROGRAM DATA REGISTER

Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMDATA<31:0>: Flash Programming Data bits

Note: The bits in this register are only reset by a Power-on Reset (POR).

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	NVMSRCADDR<31:24>									
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23:10	NVMSRCADDR<23:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	NVMSRCADDR<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				NVMSRC	ADDR<7:0>					

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 NVMSRCADDR<31:0>: Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	_	—	_	—	—	_	_	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	—	—	—	_	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	_	_	_	_	_	_	_	SWRST ⁽¹⁾

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Legend:	HC = Cleared by hardwar	re			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-1 Unimplemented: Read as '0'

- bit 0 SWRST: Software Reset Trigger bit⁽¹⁾ 1 = Enable Software Reset event
 - 0 = No effect
- Note 1: The system unlock sequence must be performed before the SWRST bit is written. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

		Vector		Persistent			
Interrupt Source ⁽¹⁾	#	#	Flag	Enable	Priority	Sub-priority	Interrupt
		Highes	st Natural O	rder Priority	,		
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1E – SPI1 Fault	36	31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1TX – SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

REGIST	ER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)
bit 9-8	IS01<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0
bit 7-5	Unimplemented: Read as '0'
bit 4-2	IP00<2:0>: Interrupt Priority bits
	<pre>111 = Interrupt priority is 7</pre>
	010 = Interrupt priority is 2 001 = Interrupt priority is 1 000 = Interrupt is disabled
bit 1-0	IS00<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0
Note:	This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bir definitions.

8.1 Oscillator Control Regiters

ТАВ	LE 8-1:	1: OSCILLATOR CONTROL REGISTER MAP																	
ess		ė	Bits													s			
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F000	OSCCON	AN 31:16 PLLODIV<2:0> FRCDIV<2:0> - S				SOSCRDY	PBDIVRDY	PBDI\	/<1:0>	PL	LMULT<2:0>	>	x1xx(2)						
FUUU	USCCON	15:0	—		COSC<2:0)>	_		NOSC<2:0	>	CLKLOCK	ULOCK ⁽³⁾	SLOCK	SLPEN	CF	UFRCEN ⁽³⁾	SOSCEN	OSWEN	xxxx(2)
E010		31:16	_	_			_	_			_	_	_	_	—	_		_	0000
1 0 10	030101	15:0	_	_			_	_			_	_			TUN	\< 5:0>			0000
F000		31:16	_								RODIV<1	4:0>							0000
F020	REFUCUN	15:0	ON		SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	-				ROSE	L<3:0>		0000
F000	DEEOTDIM	31:16				F	OTRIM<8:	0>				_	_	_	_	_		_	0000
F030	REFUTRIM	15:0	_	_	_		_	_	_	_	_	_	_	_	_	_	_	_	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

3: This bit is only available on PIC32MX2XX devices.

REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
 - 1 = Reset all Even/Odd buffer pointers to the EVEN Buffer Descriptor banks
 - 0 = Even/Odd buffer pointers are not Reset
- bit 0 USBEN: USB Module Enable bit⁽⁴⁾
 - 1 = USB module and supporting circuitry is enabled
 - 0 = USB module and supporting circuitry is disabled

SOFEN: SOF Enable bit⁽⁵⁾

- 1 = SOF token is sent every 1 ms
- 0 = SOF token is disabled
- **Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
 - 2: All host control logic is reset any time that the value of this bit is toggled.
 - 3: Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
 - 4: Device mode.
 - 5: Host mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	ON	—	SIDL	—	—	—	—	—
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	—	_	_	_	_

REGISTER 11-3: CNCONX: CHANGE NOTICE CONTROL FOR PORTX REGISTER (X = A, B, C)

Legend:

J. S.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Change Notice (CN) Control ON bit
 - 1 = CN is enabled
 - 0 = CN is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Control bit
 - 1 = Idle mode halts CN operation
 - 0 = Idle does not affect CN operation
- bit 12-0 Unimplemented: Read as '0'

REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

- bit 3 T32: 32-Bit Timer Mode Select bit⁽²⁾
 - 1 = Odd numbered and even numbered timers form a 32-bit timer
 - 0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2 Unimplemented: Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit⁽³⁾
 - 1 = External clock from TxCK pin
 - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
 - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED) bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bit 11 = Reserved; do not use 10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters) 01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters) 00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character) bit 5 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect. 0 = Address Detect mode is disabled bit 4 **RIDLE:** Receiver Idle bit (read-only) 1 =Receiver is Idle 0 = Data is being received PERR: Parity Error Status bit (read-only) bit 3 1 = Parity error has been detected for the current character 0 = Parity error has not been detected bit 2 FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character 0 = Framing error has not been detected **OERR:** Receive Buffer Overrun Error Status bit. bit 1 This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state. 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)

- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

20.1 PMP Control Registers

TABLE 20-1: PARALLEL MASTER PORT REGISTER MAP

ess				Bits															
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
7000	DMCON	31:16	_	_		—	_	—	—	—	—	—	—		_		—	_	0000
1000	FINCON	15:0	ON	_	SIDL	ADRMU	JX<1:0>	PMPTTL	PTWREN	PTRDEN	CSF	<1:0>	ALP	_	CS1P	_	WRSP	RDSP	0000
7010		31:16	_	_	_	—	_	—	—	_	_	—	—	—	—	_	_	—	0000
7010	PININODE	15:0	BUSY	IRQM	l<1:0>	INCM	<1:0>	_	MODE	<1:0>	WAITE	3<1:0>		WAITN	/<3:0>		WAITE	<1:0>	0000
		31:16	_	_	_	—	_	_	_	_	_	_	_	_	_	_	_	_	0000
7020	PMADDR	45.0		CS1															0000
		15.0	_	ADDR14	_	_	_					/	ADDR<10:0	>					
7020		31:16									T-21.05								0000
7030	PINDOUT	15:0								DAIAOU	1<31.0>								0000
7040		31:16									~21.0>								0000
7040	FINIDIN	15:0								DATAIN	~31.0~								0000
7050		31:16	—	_	_	—	_	—	—	—	—	_	_			_	_		0000
7050	PIVIAEN	15:0	- PTEN14 0000																
7060		31:16	_	—	_	—	—	—	_	_	—	—	—	—	—	_	—	_	0000
1060	PINSTAT	15:0	IBF	IBOV	_	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	_	_	OB3E	OB2E	OB1E	OB0E	0081

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

25.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 37. "Charge Time Measurement Unit (CTMU)" (DS60001167), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.



- Up to 13 channels available for capacitive or time measurement input
- · On-chip precision current source
- 16-edge input trigger sources
- · Selection of edge or level-sensitive inputs
- · Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- · High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- · Integrated temperature sensing diode
- · Control of current source during auto-sampling
- · Four current source ranges
- · Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 25-1.



© 2011-2016 Microchip Technology Inc.

NOTES:

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHA	ARACTER	ISTICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$						
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Conditions		
Operati	ng Voltag	e							
DC10	Vdd	Supply Voltage (Note 2)	2.3		3.6	V	—		
DC12	Vdr	RAM Data Retention Voltage (Note 1)	1.75	_	—	V	—		
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	1.75	_	2.1	V	_		
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.00005	_	0.115	V/μs	_		

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.



TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

АС СНА	ARACTERIS	TICS ⁽¹⁾		Star (un Ope	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Charac	Characteristics ⁽²⁾		Min.	Typical	Max.	Units	Conditions		
TA10	Т⊤хН	TxCK High Time	Synchrono with presc	ous, aler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15		
			Asynchronous, with prescaler		10	—		ns	—		
TA11	ΤτxL	TxCK Low Time	Synchrono with presc	ous, aler	[(12.5 ns or 1 ТРв)/N] + 25 ns	—		ns	Must also meet parameter TA15		
			Asynchror with presc	nous, aler	10	—		ns	—		
TA15	ΤτχΡ	TxCK Input Period	Synchrono with presc	ous, aler	[(Greater of 25 ns or 2 TPB)/N] + 30 ns	-	_	ns	VDD > 2.7V		
					[(Greater of 25 ns or 2 TPB)/N] + 50 ns	—	_	ns	VDD < 2.7V		
			Asynchror with presc	nous, aler	20	-	_	ns	VDD > 2.7V (Note 3)		
					50	-	_	ns	VDD < 2.7V (Note 3)		
OS60	FT1	SOSC1/T1C Input Freque (oscillator en the TCS (T1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by set the TCS (T1CON<1>) bi		32	_	100	kHz	_		
TA20	TCKEXTMRL	Delay from E Clock Edge t Increment	External Tx0 to Timer	СК	_	_	1	Трв	_		

Note 1: Timer1 is a Type A timer.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

TABLE A-1:	MAJOR SECTION UPDATES	(CONTINUED)	
------------	-----------------------	-------------	--

Section	Update Description
29.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings (removed Voltage on VCORE with respect to Vss).
	Added the SPDIP specification to the Thermal Packaging Characteristics (see Table 29-2).
	Updated the Typical values for parameters DC20-DC24 in the Operating Current (IDD) specification (see Table 29-5).
	Updated the Typical values for parameters DC30a-DC34a in the Idle Current (IIDLE) specification (see Table 29-6).
	Updated the Typical values for parameters DC40i and DC40n and removed parameter DC40m in the Power-down Current (IPD) specification (see Table 29-7).
	Removed parameter D320 (VCORE) from the Internal Voltage Regulator Specifications and updated the Comments (see Table 29-13).
	Updated the Minimum, Typical, and Maximum values for parameter F20b in the Internal FRC Accuracy specification (see Table 29-17).
	Removed parameter SY01 (TPWRT) and removed all Conditions from Resets Timing (see Table 29-20).
	Updated all parameters in the CTMU Specifications (see Table 29-39).
31.0 "Packaging Information"	Added the 28-lead SPDIP package diagram information (see 31.1 " Package Marking Information " and 31.2 " Package Details ").
"Product Identification System"	Added the SPDIP (SP) package definition.

Revision C (November 2011)

All major changes are referenced by their respective section in Table A-2.

TABLE A-2:	MAJOR SECTION UPDATES
------------	------------------------------

Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Revised the source/sink on I/O pins (see "Input/Output" on page 1). Added the SPDIP package to the PIC32MX220F032B device in the PIC32MX2XX USB Family Features (see Table 2).
4.0 "Memory Organization"	Removed ANSB6 from the ANSELB register and added the ODCB6, ODCB10, and ODCB11 bits in the PORTB Register Map (see Table 4-20).
29.0 "Electrical Characteristics"	Updated the minimum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 29-16).

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

U1OTGSTAT (USB OTG Status)	110
U1PWRC (USB Power Control)	112
U1SOF (USB SOF Threshold)	123
U1STAT (USB Status)	118
U1TOK (USB Token)	122
UxMODE (UARTx Mode)	
UxSTA (UARTx Status and Control)	185
WDTCON (Watchdog Timer Control)	155
Resets	
Revision History	329
RTCALRM (RTC ALARM Control)	

S

Serial Peripheral Interface (SPI)	
Software Simulator (MPLAB SIM)	
Special Features	

Т

Timer1 Module	43 47
10-Rit Analog-to-Digital Conversion	
(ASAM = 0, SSRC<2:0> = 000)	93
10-Bit Analog-to-Digital Conversion (ASAM = 1,	
SSRC<2:0> = 111, SAMC<4:0> = 00001)2	94
EJTAG	00
External Clock20	69
I/O Characteristics2	72
I2Cx Bus Data (Master Mode)22	83
I2Cx Bus Data (Slave Mode)22	86
I2Cx Bus Start/Stop Bits (Master Mode)	83
I2Cx Bus Start/Stop Bits (Slave Mode)	86
Input Capture (CAPx)2	76
OCx/PWM	77
Output Compare (OCx)2	77
Parallel Master Port Read29	96
Parallel Master Port Write2	97

Parallel Slave Port	. 295
SPIx Master Mode (CKE = 0)	. 278
SPIx Master Mode (CKE = 1)	. 279
SPIx Slave Mode (CKE = 0)	. 280
SPIx Slave Mode (CKE = 1)	. 281
Timer1, 2, 3, 4, 5 External Clock	. 275
UART Reception	. 187
UART Transmission (8-bit or 9-bit Data)	. 187
Timing Requirements	
CLKO and I/O	. 272
Timing Specifications	
I2Cx Bus Data Requirements (Master Mode)	. 284
I2Cx Bus Data Requirements (Slave Mode)	. 287
Input Capture Requirements	. 276
Output Compare Requirements	. 277
Simple OCx/PWM Mode Requirements	. 277
SPIx Master Mode (CKE = 0) Requirements	. 278
SPIx Master Mode (CKE = 1) Requirements	. 279
SPIx Slave Mode (CKE = 1) Requirements	. 281
SPIx Slave Mode Requirements (CKE = 0)	. 280
Timing Specifications (50 MHz)	
SPIx Master Mode (CKE = 0) Requirements	. 304
SPIx Master Mode (CKE = 1) Requirements	. 304
SPIx Slave Mode (CKE = 1) Requirements	. 305
SPIx Slave Mode Requirements (CKE = 0)	. 305
U	
	101

UART	
USB On-The-Go (OTG)	103
V	
VCAP nin	250

VCAP pin	
Voltage Regulator (On-Chip)	250
W	
M/M/M/ Addross	3/1

WWW Address	. 341
WWW, On-Line Support	16