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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f256d-50i-pt

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/SPDIP/SOIC	36-pin VTLA	44-pin QFN/TQFP/VTLA			
RC0	—	—	3	25	I/O	ST	PORTC is a bidirectional I/O port
RC1	—	—	4	26	I/O	ST	
RC2	—	—	—	27	I/O	ST	
RC3	—	—	11	36	I/O	ST	
RC4	—	—	—	37	I/O	ST	
RC5	—	—	—	38	I/O	ST	
RC6	—	—	—	2	I/O	ST	
RC7	—	—	—	3	I/O	ST	
RC8	—	—	—	4	I/O	ST	
RC9	—	—	20	5	I/O	ST	
T1CK	9	12	10	34	I	ST	Timer1 external clock input
T2CK	PPS	PPS	PPS	PPS	I	ST	Timer2 external clock input
T3CK	PPS	PPS	PPS	PPS	I	ST	Timer3 external clock input
T4CK	PPS	PPS	PPS	PPS	I	ST	Timer4 external clock input
T5CK	PPS	PPS	PPS	PPS	I	ST	Timer5 external clock input
U1CTS	PPS	PPS	PPS	PPS	I	ST	UART1 clear to send
U1RTS	PPS	PPS	PPS	PPS	O	—	UART1 ready to send
U1RX	PPS	PPS	PPS	PPS	I	ST	UART1 receive
U1TX	PPS	PPS	PPS	PPS	O	—	UART1 transmit
U2CTS	PPS	PPS	PPS	PPS	I	ST	UART2 clear to send
U2RTS	PPS	PPS	PPS	PPS	O	—	UART2 ready to send
U2RX	PPS	PPS	PPS	PPS	I	ST	UART2 receive
U2TX	PPS	PPS	PPS	PPS	O	—	UART2 transmit
SCK1	22	25	28	14	I/O	ST	Synchronous serial clock input/output for SPI1
SDI1	PPS	PPS	PPS	PPS	I	ST	SPI1 data in
SDO1	PPS	PPS	PPS	PPS	O	—	SPI1 data out
SS1	PPS	PPS	PPS	PPS	I/O	ST	SPI1 slave synchronization or frame pulse I/O
SCK2	23	26	29	15	I/O	ST	Synchronous serial clock input/output for SPI2
SDI2	PPS	PPS	PPS	PPS	I	ST	SPI2 data in
SDO2	PPS	PPS	PPS	PPS	O	—	SPI2 data out
SS2	PPS	PPS	PPS	PPS	I/O	ST	SPI2 slave synchronization or frame pulse I/O
SCL1	14	17	18	44	I/O	ST	Synchronous serial clock input/output for I2C1

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input

O = Output

PPS = Peripheral Pin Select

P = Power

I = Input

— = N/A

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. “Oscillator Configuration”** (DS60001112), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MX1XX/2XX 28/36/44-pin Family oscillator system has the following modules and features:

- Four external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

A block diagram of the oscillator system is provided in Figure 8-1.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCCEN	CRCCAPP ⁽¹⁾	CRCTYP	—	—	CRCCH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (i.e., reverse source byte order)

00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)

0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCCEN:** CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCCAPP bit cannot be set.

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REGISTER 9-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0> ⁽¹⁾							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0> ⁽¹⁾							
7:0	S-0 CFORCE	S-0 CABORT	R/W-0 PATEN	R/W-0 SIRQEN	R/W-0 AIRQEN	U-0 —	U-0 —	U-0 —

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits⁽¹⁾

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•
•
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits⁽¹⁾

11111111 = Interrupt 255 will initiate a DMA transfer

•
•
•

00000001 = Interrupt 1 will initiate a DMA transfer

00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

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REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit

- 1 = A change in the ID state was detected
- 0 = No change in the ID state was detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit

- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit

- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit

- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit

- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit

- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit

- 1 = A change on the session valid input was detected
- 0 = No change on the session valid input was detected

TABLE 11-5: PORTC REGISTER MAP

Virtual Address (BF88-#)	Register Name ^(1,2)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	ANSC3 ⁽⁴⁾	ANSC2 ⁽³⁾	ANSC1	ANSC0	000F
6210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISC9	TRISC8 ⁽³⁾	TRISC7 ⁽³⁾	TRISC6 ⁽³⁾	TRISC5 ⁽³⁾	TRISC4 ⁽³⁾	TRISC3	TRISC2 ⁽³⁾	TRISC1	TRISC0	03FF
6220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RC9	RC8 ⁽³⁾	RC7 ⁽³⁾	RC6 ⁽³⁾	RC5 ⁽³⁾	RC4 ⁽³⁾	RC3	RC2 ⁽³⁾	RC1	RC0	xxxx
6230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATC9	LATC8 ⁽³⁾	LATC7 ⁽³⁾	LATC6 ⁽³⁾	LATC5 ⁽³⁾	LATC4 ⁽³⁾	LATC3	LATC2 ⁽³⁾	LATC1	LATC0	xxxx
6240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCC9	ODCC8 ⁽³⁾	ODCC7 ⁽³⁾	ODCC6 ⁽³⁾	ODCC5 ⁽³⁾	ODCC4 ⁽³⁾	ODCC3	ODCC2 ⁽³⁾	ODCC1	ODCC0	0000
6250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUC9	CNPUC8 ⁽³⁾	CNPUC7 ⁽³⁾	CNPUC6 ⁽³⁾	CNPUC5 ⁽³⁾	CNPUC4 ⁽³⁾	CNPUC3	CNPUC2 ⁽³⁾	CNPUC1	CNPUC0	0000
6260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDC9	CNPDC8 ⁽³⁾	CNPDC7 ⁽³⁾	CNPDC6 ⁽³⁾	CNPDC5 ⁽³⁾	CNPDC4 ⁽³⁾	CNPDC3	CNPDC2 ⁽³⁾	CNPDC1	CNPDC0	0000
6270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIEC9	CNIEC8 ⁽³⁾	CNIEC7 ⁽³⁾	CNIEC6 ⁽³⁾	CNIEC5 ⁽³⁾	CNIEC4 ⁽³⁾	CNIEC3	CNIEC2 ⁽³⁾	CNIEC1	CNIEC0	0000
6290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNSTATC9	CNSTATC8 ⁽³⁾	CNSTATC7 ⁽³⁾	CNSTATC6 ⁽³⁾	CNSTATC5 ⁽³⁾	CNSTATC4 ⁽³⁾	CNSTATC3	CNSTATC2 ⁽³⁾	CNSTATC1	CNSTATC0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.
- 2: PORTC is not available on 28-pin devices.
- 3: This bit is only available on 44-pin devices.
- 4: This bit is only available on USB-enabled devices with 36 or 44 pins.

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REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 SPISGNEXT	U-0 —	U-0 —	R/W-0 FRMERREN	R/W-0 SPIROVEN	R/W-0 SPITUREN	R/W-0 IGNROV	R/W-0 IGNTUR
7:0	R/W-0 AUDEN ⁽¹⁾	U-0 —	U-0 —	U-0 —	R/W-0 AUDMONO ^(1,2)	U-0 —	R/W-0 AUDMOD<1:0> ^(1,2)	R/W-0 —

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit

1 = Data from RX FIFO is sign extended

0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit

1 = Frame Error overflow generates error events

0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit

1 = Receive overflow generates error events

0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit

1 = Transmit underrun generates error events

0 = Transmit underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)

1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data

0 = A ROV is a critical error that stops SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)

1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty

0 = A TUR is a critical error that stops SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit⁽¹⁾

1 = Audio protocol enabled

0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit^(1,2)

1 = Audio data is mono (Each data word is transmitted on both left and right channels)

0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit^(1,2)

11 = PCM/DSP mode

10 = Right-Justified mode

01 = Left-Justified mode

00 = I²S mode

Note 1: This bit can only be written when the ON bit = 0.

2: This bit is only valid for AUDEN = 1.

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REGISTER 19-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5 **ABAUD**: Auto-Baud Enable bit
 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55);
 cleared by hardware upon completion
 0 = Baud rate measurement disabled or completed
- bit 4 **RXINV**: Receive Polarity Inversion bit
 1 = UxRX Idle state is '0'
 0 = UxRX Idle state is '1'
- bit 3 **BRGH**: High Baud Rate Enable bit
 1 = High-Speed mode – 4x baud clock enabled
 0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1 **PDSEL<1:0>**: Parity and Data Selection bits
 11 = 9-bit data, no parity
 10 = 8-bit data, odd parity
 01 = 8-bit data, even parity
 00 = 8-bit data, no parity
- bit 0 **STSEL**: Stop Selection bit
 1 = 2 Stop bits
 0 = 1 Stop bit

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 22-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	—	—	SAMC<4:0> ⁽¹⁾				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
	ADCS<7:0> ⁽²⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit

1 = Clock derived from FRC

0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits⁽¹⁾

11111 = 31 TAD

•
•
•

00001 = 1 TAD

00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits⁽²⁾

11111111 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 512 \cdot TPB = TAD$

•
•
•

00000001 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 4 \cdot TPB = TAD$

00000000 = $TPB \cdot 2 \cdot (ADCS<7:0> + 1) = 2 \cdot TPB = TAD$

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.

2: This bit is not used if the ADRC (AD1CON3<15>) bit = 1.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 EDG1MOD	R/W-0 EDG1POL	R/W-0 EDG1SEL<3:0>				R/W-0 EDG2STAT	R/W-0 EDG1STAT
23:16	R/W-0 EDG2MOD	R/W-0 EDG2POL	R/W-0 EDG2SEL<3:0>				U-0 —	U-0 —
15:8	R/W-0 ON	U-0 —	R/W-0 CTMUSIDL	R/W-0 TGEN ⁽¹⁾	R/W-0 EDGEN	R/W-0 EDGSEQEN	R/W-0 IDISSEN ⁽²⁾	R/W-0 CTTRIG
7:0	R/W-0 ITRIM<5:0>						R/W-0 IRNG<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **EDG1MOD:** Edge1 Edge Sampling Select bit

1 = Input is edge-sensitive

0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit

1 = Edge1 programmed for a positive edge response

0 = Edge1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits

1111 = C3OUT pin is selected

1110 = C2OUT pin is selected

1101 = C1OUT pin is selected

1100 = IC3 Capture Event is selected

1011 = IC2 Capture Event is selected

1010 = IC1 Capture Event is selected

1001 = CTED8 pin is selected

1000 = CTED7 pin is selected

0111 = CTED6 pin is selected

0110 = CTED5 pin is selected

0101 = CTED4 pin is selected

0100 = CTED3 pin is selected

0011 = CTED1 pin is selected

0010 = CTED2 pin is selected

0001 = OC1 Compare Event is selected

0000 = Timer1 Event is selected

bit 25 **EDG2STAT:** Edge2 Status bit

Indicates the status of Edge2 and can be written to control edge source

1 = Edge2 has occurred

0 = Edge2 has not occurred

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 30-41) in **Section 30.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
	—	—	—	—	—	—	FWDTWINSZ<1:0>	
23:16	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ<1:0>**: Watchdog Timer Window Size bits

11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN**: Watchdog Timer Enable bit

1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS**: Watchdog Timer Window Enable bit

1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>**: Watchdog Timer Postscale Select bits

10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

All other combinations not shown result in operation = 10100

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

- bit 15-14 **FCKSM<1:0>**: Clock Switching and Monitor Selection Configuration bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
- bit 13-12 **FPBDIV<1:0>**: Peripheral Bus Clock Divisor Default Value bits
11 = PBCLK is SYSCLK divided by 8
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1
- bit 11 **Reserved**: Write '1'
- bit 10 **OSCIOFNC**: CLKO Enable Configuration bit
1 = CLKO output disabled
0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)
- bit 9-8 **POSCMOD<1:0>**: Primary Oscillator Configuration bits
11 = Primary Oscillator is disabled
10 = HS Oscillator mode is selected
01 = XT Oscillator mode is selected
00 = External Clock mode is selected
- bit 7 **IESO**: Internal External Switchover bit
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)
- bit 6 **Reserved**: Write '1'
- bit 5 **FSOSCEN**: Secondary Oscillator Enable bit
1 = Enable Secondary Oscillator
0 = Disable Secondary Oscillator
- bit 4-3 **Reserved**: Write '1'
- bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits
111 = Fast RC Oscillator with divide-by-N (FRCDIV)
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (Sosc)
011 = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL)
010 = Primary Oscillator (XT, HS, EC)⁽¹⁾
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
000 = Fast RC Oscillator (FRC)

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 31 **FVBUSONIO:** USB VBUSON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function
- bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function
- bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations
- bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations
- bit 27-16 **Reserved:** Write '1'
- bit 15-0 **USERID<15:0>:** User ID bits
This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 27-6: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0> ⁽¹⁾				DEVID<27:24> ⁽¹⁾			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16> ⁽¹⁾							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8> ⁽¹⁾							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0> ⁽¹⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **VER<3:0>**: Revision Identifier bits⁽¹⁾

bit 27-0 **DEVID<27:0>**: Device ID bits⁽¹⁾

Note 1: See the "PIC32 Flash Programming Specification" (DS60001145) for a list of Revision and Device ID values.

28.0 INSTRUCTION SET

The PIC32MX1XX/2XX family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

<p>Note: Refer to “MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set” at www.imgtec.com for more information.</p>
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PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode (Note 2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode (Note 2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 2)	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$TPB * (BRG + 2)$	—	ns	—
			400 kHz mode	$TPB * (BRG + 2)$	—	ns	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	ns	

Note 1: BRG is the value of the I²C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode (Note 2)	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode (Note 2)	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	—
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See Note 3

Note 1: BRG is the value of the I²C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 31-3: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial	
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions
Idle Current (I_{IDLE}): Core Off, Clock on Base Current (Note 1)				
MDC34a	8	13	mA	50 MHz

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = V_{DD}$
- RTCC and JTAG are disabled

2: Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial	
Param. No.	Typical ⁽²⁾	Max.	Units	Conditions
Power-Down Current (I_{PD}) (Note 1)				
MDC40k	10	25	μA	-40°C
MDC40n	250	500	μA	+85°C
Module Differential Current				
MDC41e	10	55	μA	3.6V
MDC42e	23	55	μA	3.6V
MDC43d	1100	1300	μA	3.6V

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = V_{DD}$
- RTCC and JTAG are disabled

2: Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

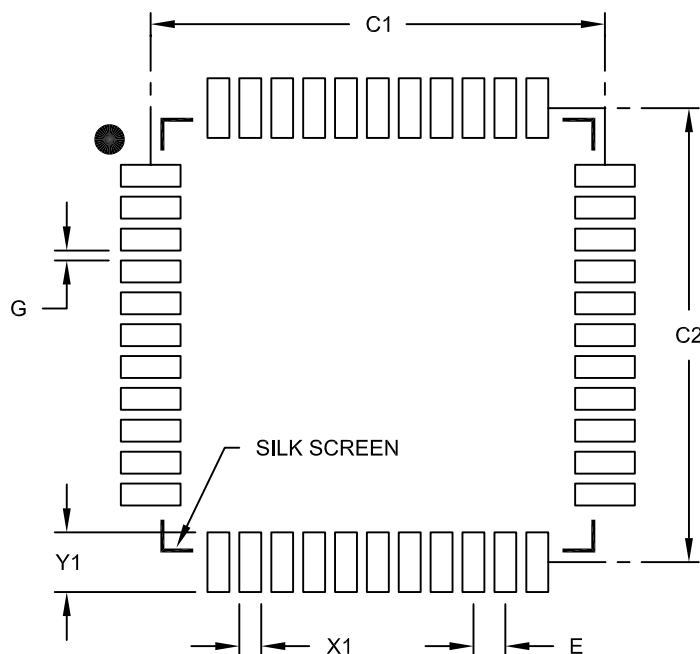
3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B