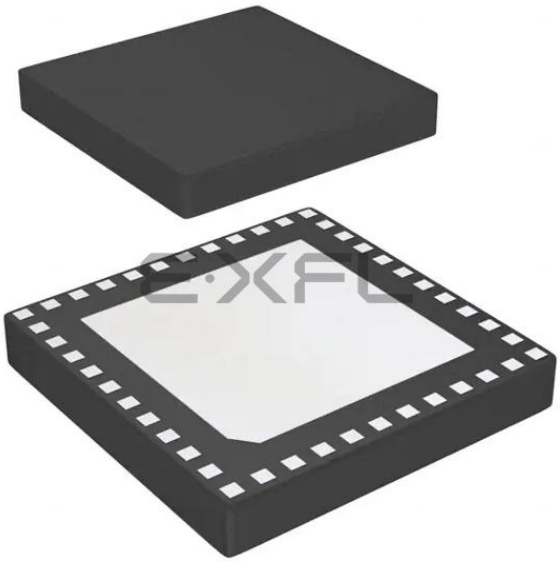
Microchip Technology - PIC32MX170F256DT-V/TL Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f256dt-v-tl

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
OC1	PPS	PPS	PPS	PPS	O	—	Output Compare Output 1
OC2	PPS	PPS	PPS	PPS	O	—	Output Compare Output 2
OC3	PPS	PPS	PPS	PPS	O	—	Output Compare Output 3
OC4	PPS	PPS	PPS	PPS	O	—	Output Compare Output 4
OC5	PPS	PPS	PPS	PPS	O	—	Output Compare Output 5
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault B Input
INT0	13	16	17	43	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4
RA0	27	2	33	19	I/O	ST	PORTA is a bidirectional I/O port
RA1	28	3	34	20	I/O	ST	
RA2	6	9	7	30	I/O	ST	
RA3	7	10	8	31	I/O	ST	
RA4	9	12	10	34	I/O	ST	
RA7	—	—	—	13	I/O	ST	
RA8	—	—	—	32	I/O	ST	
RA9	—	—	—	35	I/O	ST	
RA10	—	—	—	12	I/O	ST	
RB0	1	4	35	21	I/O	ST	PORTB is a bidirectional I/O port
RB1	2	5	36	22	I/O	ST	
RB2	3	6	1	23	I/O	ST	
RB3	4	7	2	24	I/O	ST	
RB4	8	11	9	33	I/O	ST	
RB5	11	14	15	41	I/O	ST	
RB6	12(2)	15(2)	16(2)	42(2)	I/O	ST	
RB7	13	16	17	43	I/O	ST	
RB8	14	17	18	44	I/O	ST	
RB9	15	18	19	1	I/O	ST	
RB10	18	21	24	8	I/O	ST	
RB11	19	22	25	9	I/O	ST	
RB12	20(2)	23(2)	26(2)	10(2)	I/O	ST	
RB13	21	24	27	11	I/O	ST	
RB14	22	25	28	14	I/O	ST	
RB15	23	26	29	15	I/O	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP03<2:0>			IS03<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP02<2:0>			IS02<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP01<2:0>			IS01<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP00<2:0>			IS00<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP03<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS03<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP02<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

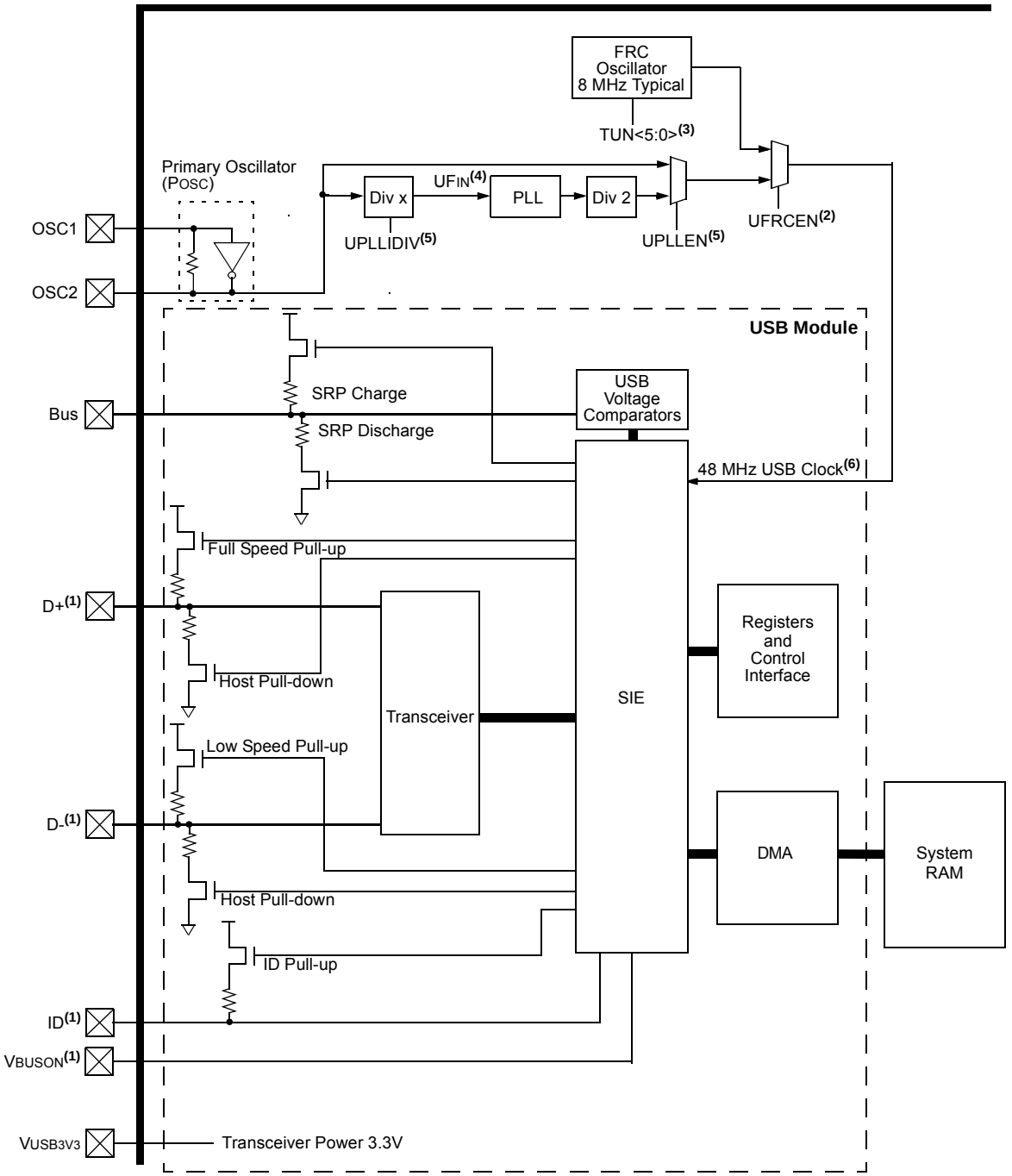
bit 17-16 **IS02<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP01<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

FIGURE 10-1: PIC32MX1XX/2XX 28/36/44-PIN FAMILY FAMILY USB INTERFACE DIAGRAM



Note 1: Pins can be used as digital input/output when USB is not enabled.
2: This bit field is contained in the OSCCON register.
3: This bit field is contained in the OSCTRM register.
4: USB PLL UFIN requirements: 4 MHz.
5: This bit field is contained in the DEVCFG2 register.
6: A 48 MHz clock is required for proper USB operation.

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REGISTER 10-5: U1PWRC: USB POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	—	—	USLPGRD	USBBUSY(1)	—	USUSPEND	USBPWR

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB bus activity has been detected; however, an interrupt is pending, which has yet to be generated
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode
  (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit
- 1 = USB module is turned on
- 0 = USB module is disabled
  (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

Note 1: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

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REGISTER 10-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

REGISTER 10-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

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REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	—	—	FORM<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
	SSRC<2:0>			CLRASAM	—	ASAM	SAMP(2)	DONE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit(1)
- 1 = ADC module is operating
- 0 = ADC module is not operating

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits
- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
- 000 =Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.

3: This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON(1)	COE	CPOL(2)	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit(1)
- 1 = Module is enabled. Setting this bit does not affect the other bits in this register
- 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is driven on the output CxOUT pin
- 0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit(2)
- 1 = Output is inverted
- 0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
- 1 = Output of the Comparator is a '1'
- 0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
- 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
- 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
- 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
- 00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit
- 1 = Comparator non-inverting input is connected to the internal CVREF
- 0 = Comparator non-inverting input is connected to the CXINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
- 11 = Comparator inverting input is connected to the IVREF
- 10 = Comparator inverting input is connected to the CxIND pin
- 01 = Comparator inverting input is connected to the CxINC pin
- 00 = Comparator inverting input is connected to the CxINB pin

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

TABLE 26-2: PERIPHERAL MODULE DISABLE REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F240	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CVRMD	—	—	—	CTMUMD	—	—	—	—	—	—	—	AD1MD	0000
F250	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD	0000
F260	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
F270	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	T5MD	T4MD	T3MD	T2MD	T1MD	0000
F280	PMD5	31:16	—	—	—	—	—	—	—	USB1MD	—	—	—	—	—	—	I2C1MD	I2C1MD	0000
		15:0	—	—	—	—	—	—	SPI2MD	SPI1MD	—	—	—	—	—	—	U2MD	U1MD	0000
F290	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PMPMD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	RTCCMD	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

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REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits
- 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
- 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-12 **FPBDIV<1:0>:** Peripheral Bus Clock Divisor Default Value bits
- 11 = PBCLK is SYSCLK divided by 8
- 10 = PBCLK is SYSCLK divided by 4
- 01 = PBCLK is SYSCLK divided by 2
- 00 = PBCLK is SYSCLK divided by 1

bit 11 **Reserved:** Write '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit
- 1 = CLKO output disabled
- 0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits
- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock mode is selected

bit 7 **IESO:** Internal External Switchover bit
- 1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
- 0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **Reserved:** Write '1'

bit 5 **FSOSCEN:** Secondary Oscillator Enable bit
- 1 = Enable Secondary Oscillator
- 0 = Disable Secondary Oscillator

bit 4-3 **Reserved:** Write '1'

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
- 111 = Fast RC Oscillator with divide-by-N (FRCDIV)
- 110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (POSC) with PLL module (XT+PLL, HS+PLL, EC+PLL)
- 010 = Primary Oscillator (XT, HS, EC)(1)
- 001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
- 000 = Fast RC Oscillator (FRC)

Note 1: Do not disable the POSC (POSCMOD = 11) when using this oscillator source.

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REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FVBUSONIO:** USB VBUSON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function

bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDI1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27-16 **Reserved:** Write '1'

bit 15-0 **USERID<15:0>:** User ID bits
This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	40 40	MHz MHz	EC **(Note 4)** ECPLL **(Note 3)**
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT **(Note 4)**
OS12			4	—	10	MHz	XTPLL **(Notes 3,4)**
OS13			10	—	25	MHz	HS **(Note 5)**
OS14			10	—	25	MHz	HSPLL **(Notes 3,4)**
OS15			32	32.768	100	kHz	SOSC **(Note 4)**
OS20	TOSC	TOSC = 1/FOSC = TCY **(Note 2)**	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.45 x TOSC	—	—	ns	EC **(Note 4)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x TOSC	ns	EC **(Note 4)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 4)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 4)**
OS42	GM	External Oscillator Transconductance (Primary Oscillator only)	—	12	—	mA/V	VDD = 3.3V, TA = +25°C **(Note 4)**

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

2: Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

3: PLL input requirements: 4 MHz ≤ FPLLIN ≤ 5 MHz (use PLL prescaler to reduce FOSC). This parameter is characterized, but tested at 10 MHz only at manufacturing.

4: This parameter is characterized, but not tested in manufacturing.

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FIGURE 30-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

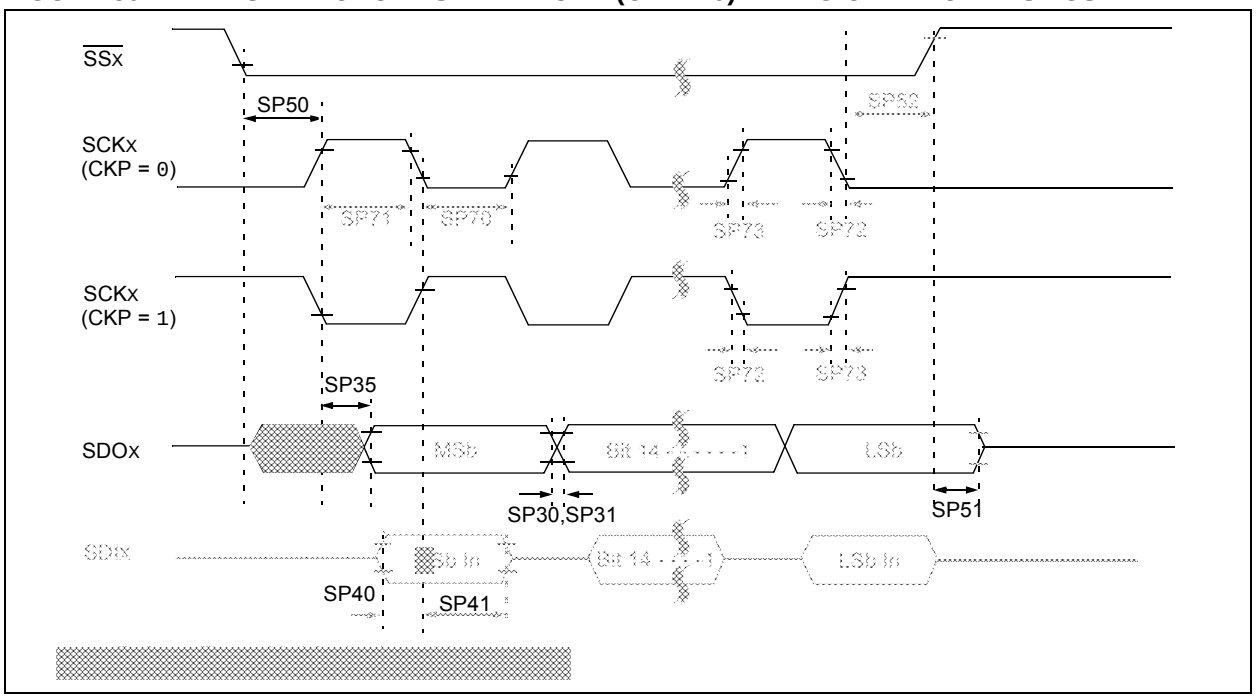

TABLE 30-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	175	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 3)**	5	—	25	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	Tsck + 20	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns.

4: Assumes 50 pF load on all SPIx pins.

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TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	—
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	—
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 2)**	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	ns	—
			400 kHz mode	TPB * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	ns	

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

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TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode **(Note 2)**	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	—
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

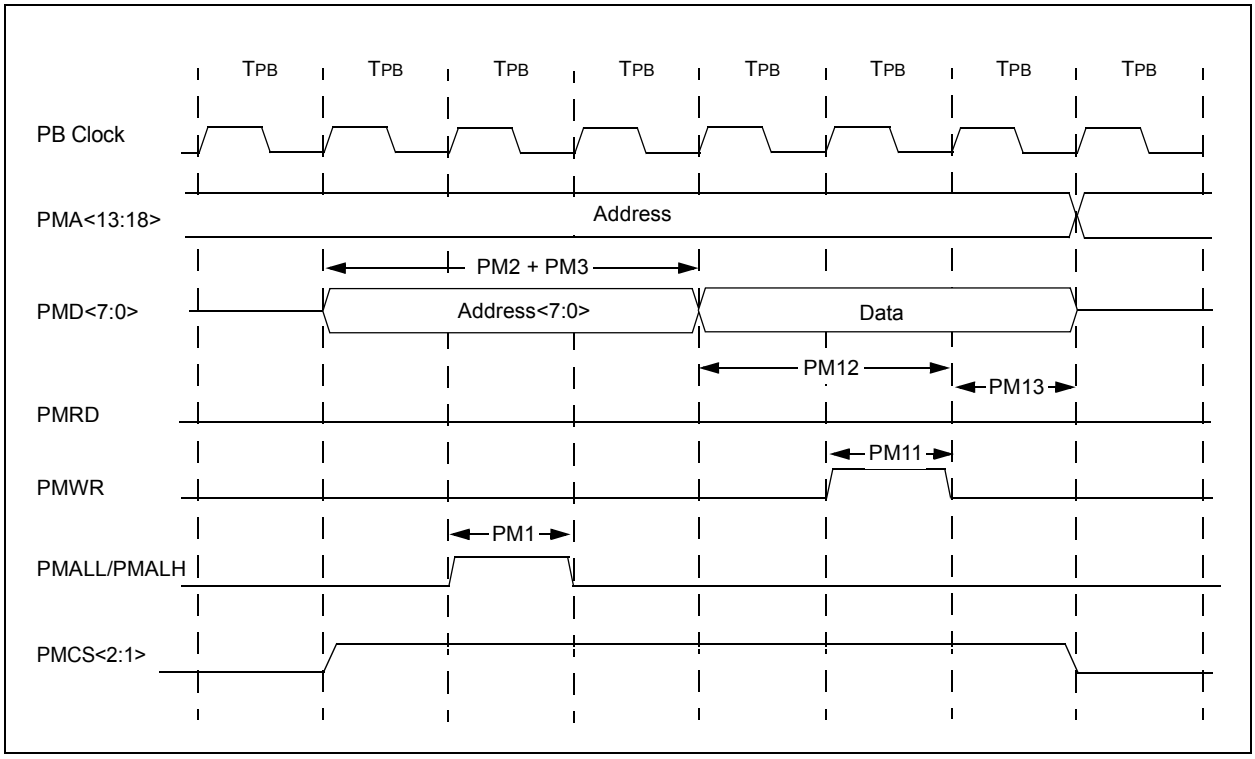
3: The typical value for this parameter is 104 ns.

TABLE 30-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	—
PM2	TADSU	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 TPB	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

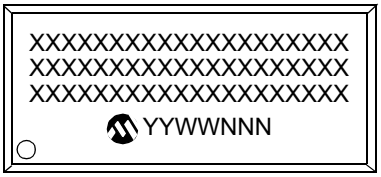
FIGURE 30-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM



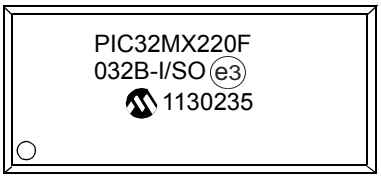
33.0 PACKAGING INFORMATION

33.1 Package Marking Information

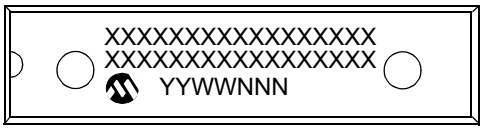
28-Lead SOIC



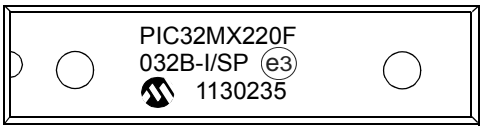
Example



28-Lead SPDIP



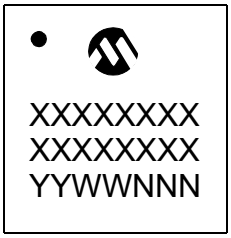
Example



28-Lead SSOP

Example

28-Lead QFN



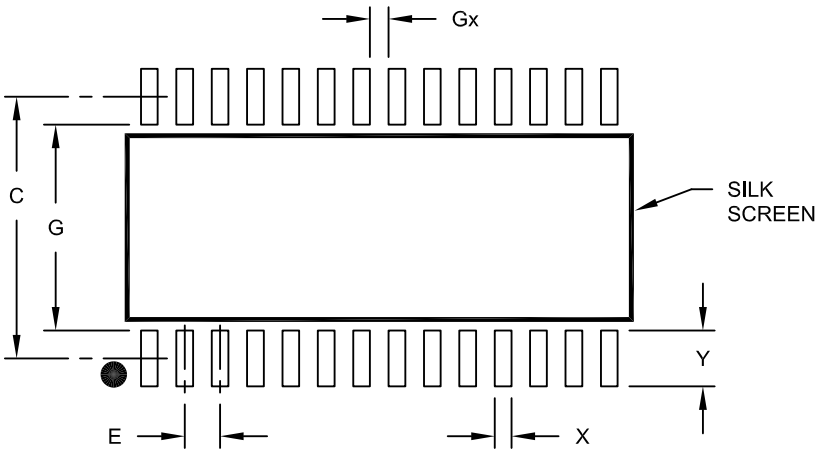
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

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TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section	Update Description
29.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings (removed Voltage on VCORE with respect to VSS). Added the SPDIP specification to the Thermal Packaging Characteristics (see Table 29-2). Updated the Typical values for parameters DC20-DC24 in the Operating Current (IDD) specification (see Table 29-5). Updated the Typical values for parameters DC30a-DC34a in the Idle Current (IIDLE) specification (see Table 29-6). Updated the Typical values for parameters DC40i and DC40n and removed parameter DC40m in the Power-down Current (IPD) specification (see Table 29-7). Removed parameter D320 (VCORE) from the Internal Voltage Regulator Specifications and updated the Comments (see Table 29-13). Updated the Minimum, Typical, and Maximum values for parameter F20b in the Internal FRC Accuracy specification (see Table 29-17). Removed parameter SY01 (TPWRT) and removed all Conditions from Resets Timing (see Table 29-20). Updated all parameters in the CTMU Specifications (see Table 29-39).
31.0 "Packaging Information"	Added the 28-lead SPDIP package diagram information (see **31.1 "Package Marking Information"** and **31.2 "Package Details"**).
"Product Identification System**"**	Added the SPDIP (SP) package definition.

Revision C (November 2011)

All major changes are referenced by their respective section in Table A-2.

TABLE A-2: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog**"**	Revised the source/sink on I/O pins (see **"Input/Output"** on page 1). Added the SPDIP package to the PIC32MX220F032B device in the PIC32MX2XX USB Family Features (see Table 2).
4.0 "Memory Organization"	Removed ANSB6 from the ANSELB register and added the ODCB6, ODCB10, and ODCB11 bits in the PORTB Register Map (see Table 4-20).
29.0 "Electrical Characteristics"	Updated the minimum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 29-16).

NOTES:

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