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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

-XF

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx210f016b-i-ss

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# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

		Pin Nu	mber <sup>(1)</sup>				
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		_	_	27	0	_	Parallel Master Port address
PMA3				38	0	—	(Demultiplexed Master modes)
PMA4				37	0	—	
PMA5		_	_	4	0	_	
PMA6		_	_	5	0	_	
PMA7				13	0	—	
PMA8		_	_	32	0	_	
PMA9		_	_	35	0	_	
PMA10		_	_	12	0	_	
PMCS1	23	26	29	15	0	_	Parallel Master Port Chip Select 1 strobe
	20 <sup>(2)</sup>	23 <sup>(2)</sup>	26 <sup>(2)</sup>	10 <sup>(2)</sup>	1/0	TTI /CT	Parallel Master Port data (Demultiplexed
	1 <sup>(3)</sup>	4 <sup>(3)</sup>	35 <sup>(3)</sup>	21 <sup>(3)</sup>	1/0	111/31	Master mode) or address/data
	19 <b>(2)</b>	22 <sup>(2)</sup>	25 <sup>(2)</sup>	9(2)	1/0	TTI /CT	(Multiplexed Master modes)
	2 <sup>(3)</sup>	5 <sup>(3)</sup>	36 <sup>(3)</sup>	22 <sup>(3)</sup>	1/0	111/31	
	18 <sup>(2)</sup>	21 <sup>(2)</sup>	24 <sup>(2)</sup>	8 <sup>(2)</sup>	1/0	TTI /ST	
	3(3)	6 <sup>(3)</sup>	1 <sup>(3)</sup>	23 <sup>(3)</sup>	1/0	116/01	
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12 <sup>(2)</sup>	15 <sup>(2)</sup>	16 <sup>(2)</sup>	42 <sup>(2)</sup>	1/0	тті /ет	1
	28 <sup>(3)</sup>	3(3)	34 <b>(3)</b>	20 <sup>(3)</sup>	1/0	111/31	
PMD7	11(2)	14 <sup>(2)</sup>	15 <b>(2)</b>	41 <sup>(2)</sup>	1/0	TTI /ST	
	27 <sup>(3)</sup>	2 <sup>(3)</sup>	33 <b>(3)</b>	19 <sup>(3)</sup>	1/0	112/01	
PMRD	21	24	27	11	0	—	Parallel Master Port read strobe
	22 <sup>(2)</sup>	25 <sup>(2)</sup>	28 <sup>(2)</sup>	14 <sup>(2)</sup>	0		Parallel Master Port write strope
	4 <sup>(3)</sup>	7 <sup>(3)</sup>	2 <sup>(3)</sup>	24 <sup>(3)</sup>	Ŭ		T arallel master Fort while strobe
VBUS	12 <sup>(3)</sup>	15 <sup>(3)</sup>	16 <b>(3)</b>	42 <sup>(3)</sup>	Ι	Analog	USB bus power monitor
VUSB3V3	20 <sup>(3)</sup>	23 <sup>(3)</sup>	26 <sup>(3)</sup>	10 <sup>(3)</sup>	Р	_	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22 <sup>(3)</sup>	25 <sup>(3)</sup>	28 <sup>(3)</sup>	14 <sup>(3)</sup>	0		USB Host and OTG bus power control output
D+	18 <sup>(3)</sup>	21 <sup>(3)</sup>	24 <sup>(3)</sup>	8 <sup>(3)</sup>	I/O	Analog	USB D+
D-	19 <sup>(3)</sup>	22 <sup>(3)</sup>	25 <sup>(3)</sup>	9(3)	I/O	Analog	USB D-
Legend:	CMOS = C	MOS compa	atible input	or output		Analog =	Analog input P = Power
	ST = Schmi	tt Trigger in	put with CN	NOS levels		O = Outp	but I=Input
	L  =   L	nput buffer				PPS = P	eripheral Pin Select — = N/A

#### 

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7  $\mu F$  to 47  $\mu F$ . This capacitor should be located as close to the device as possible.

## 2.3 Capacitor on Internal Voltage Regulator (VCAP)

### 2.3.1 INTERNAL REGULATOR MODE

A low-ESR (3 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **30.0 "Electrical Characteristics"** for additional information on CEFC specifications.

## 2.4 Master Clear (MCLR) Pin

The  $\overline{\text{MCLR}}$  pin provides two specific device functions:

- Device Reset
- Device programming and debugging

Pulling The  $\overline{\text{MCLR}}$  pin low generates a device Reset. Figure 2-2 illustrates a typical  $\overline{\text{MCLR}}$  circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the  $\overline{\text{MCLR}}$  pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.



# EXAMPLE OF MCLR PIN CONNECTIONS



**3:** No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

## 2.9 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-5 and Figure 2-6.





FIGURE 2-6: AUDIO PLAYBACK APPLICATION





#### FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 256 KB FLASH)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
31:24	—	—	—	—	—	—	—	—					
	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1					
23:16	—	—	—	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS					
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
15:8	—	—	—	—	-	—	_	—					
	U-0	R/W-1	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1					
7:0	_	BMX WSDRM	_	_	_	E	3MXARB<2:0	>					

## REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

## bit 31-21 Unimplemented: Read as '0'

	Ommplemented. Read as 0
bit 20	BMXERRIXI: Enable Bus Error from IXI bit
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus</li> </ul>
bit 19	BMXERRICD: Enable Bus Error from ICD Debug Unit bit
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from ICD</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from ICD</li> </ul>
bit 18	BMXERRDMA: Bus Error from DMA bit
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from DMA</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from DMA</li> </ul>
bit 17	BMXERRDS: Bus Error from CPU Data Access bit (disabled in Debug mode)
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access</li> </ul>
bit 16	BMXERRIS: Bus Error from CPU Instruction Access bit (disabled in Debug mode)
	<ul> <li>1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access</li> <li>0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access</li> </ul>
bit 15-7	Unimplemented: Read as '0'
bit 6	BMXWSDRM: CPU Instruction or Data Access from Data RAM Wait State bit
	<ul> <li>1 = Data RAM accesses from CPU have one wait state for address setup</li> <li>0 = Data RAM accesses from CPU have zero wait states for address setup</li> </ul>
bit 5-3	Unimplemented: Read as '0'
bit 2-0	BMXARB<2:0>: Bus Matrix Arbitration Mode bits
	111 = Reserved (using these Configuration modes will produce undefined behavior)
	•
	•
	<ul><li>011 = Reserved (using these Configuration modes will produce undefined behavior)</li><li>010 = Arbitration Mode 2</li></ul>
	001 = Arbitration Mode 1 (default) 000 = Arbitration Mode 0

### REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

bit 3	CF: Clock Fail Detect bit
	1 = FSCM has detected a clock failure
	0 = No clock failure has been detected
bit 2	UFRCEN: USB FRC Clock Enable bit <sup>(1)</sup>
	<ul> <li>1 = Enable the FRC as the clock source for the USB clock source</li> <li>0 = Use the Primary Oscillator or USB PLL as the USB clock source</li> </ul>
bit 1	SOSCEN: Secondary Oscillator (Sosc) Enable bit
	1 = Enable the Secondary Oscillator
	0 = Disable the Secondary Oscillator
bit 0	OSWEN: Oscillator Switch Enable bit
	<ul> <li>1 = Initiate an oscillator switch to selection specified by NOSC&lt;2:0&gt; bits</li> <li>0 = Oscillator switch is complete</li> </ul>
Note 1:	This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

## 9.1 DMA Control Registers

#### TABLE 9-1: DMA GLOBAL REGISTER MAP

ess	Register Name <sup>(1)</sup>	0		Bits													6		
Virtual Addr (BF88_#)		Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
2000		31:16	_	-	_	—	—	—	—	_	_	—	—	—	_	—	—	_	0000
3000	DIVIACON	15:0	ON	—	—	SUSPEND	DMABUSY	_	_	_	_	_	—	_	—	—	—	—	0000
3010	DMASTAT	31:16	—	-	—	—	_	_	_	_	_	_	_	_	_	—	_	—	0000
3010	DIVIASTAT	15:0			_	_	_	_	_	_	_	_	_	_	RDWR	DI	MACH<2:0>	(2)	0000
3020		31:16									D-31.05								0000
3020 DMA/	DIVIAADDIN	15:0								DIVIAADL	N<51.02								0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

#### TABLE 9-2: DMA CRC REGISTER MAP

ess		÷.		Bits															
Virtual Addr (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2020	DCBCCON	31:16	—	—	BYTC	)<1:0>	WBO	—	—	BITO	_	—	_	_	_	_	_	_	0000
3030	DCRCCON	15:0	_	_	_			PLEN<4:0>	•		CRCEN	CRCAPP	CRCTYP	—	_	C	RCCH<2:0	>	0000
2040		31:16															0000		
3040	DCRCDAIA	15:0								DURUDA	IA-51.02								0000
2050	DCBCVOB	31:16												0000					
3050	DCRCXOR	15:0								DURUN	51.02								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

NOTES:

## 11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

### 11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

### 11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digitalonly peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I<sup>2</sup>C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin.

Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

#### 11.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

## 11.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

#### FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	_	—	-		
00.40	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
23:10	—	—	—	MONTH10	MONTH01<3:0>					
45.0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15:8	—	—	DAY1	0<1:0>		DAY01	<3:0>			
7.0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x		
7:0			_	_	_	WDAY01<2:0>				

## REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER

## Legend:

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 Unimplemented: Read as '0'

bit 20 MONTH10: Binary Coded Decimal value of months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9 bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 DAY10<1:0>: Binary Coded Decimal value of days bits, 10s place digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 Unimplemented: Read as '0'

bit 2-0 WDAY01<2:0>: Binary Coded Decimal value of weekdays bits; contains a value from 0 to 6

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0						
31.24	—	—	—	—	—		—	_
00.40	U-0	U-0						
23:10	-	—	—	—	—		—	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
15:8	ON <sup>(1)</sup>	—	SIDL	—	—	F	ORM<2:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
7:0		SSRC<2:0>		CLRASAM		ASAM	SAMP <sup>(2)</sup>	DONE <sup>(3)</sup>

#### REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit<sup>(1)</sup>
  - 1 = ADC module is operating
  - 0 = ADC module is not operating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
  - 1 = Discontinue module operation when device enters Idle mode
  - 0 = Continue module operation when the device enters Idle mode

#### bit 12-11 Unimplemented: Read as '0'

- bit 10-8 **FORM<2:0>:** Data Output Format bits
  - 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
  - 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
  - 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
  - 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
  - 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
  - 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)

  - 000 =Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

#### bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
  - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
31:24	—	—	—	—	—	—	—	—
00.40	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
23:16	—	—	—	—	—	FPLLODIV<2:0>		
45.0	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
15:8	UPLLEN <sup>(1)</sup>	—	—	_	_	UPLLIDIV<2:0> <sup>(1)</sup>		
7:0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
	_	FPLLMUL<2:0>			_	FPLLIDIV<2:0>		

#### **DEVCFG2: DEVICE CONFIGURATION WORD 2 REGISTER 27-3:**

Legend:	r = Reserved bit P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-19 Reserved: Write '1'

bit 15

bit 7

bit 18-16 FPLLODIV<2:0>: Default PLL Output Divisor bits

- 111 = PLL output divided by 256 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2 000 = PLL output divided by 1 UPLLEN: USB PLL Enable bit<sup>(1)</sup> 1 = Disable and bypass USB PLL 0 = Enable USB PLL bit 14-11 Reserved: Write '1' bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits<sup>(1)</sup> 111 = 12x divider 110 = 10x divider 101 = 6x divider100 = 5x divider 011 = 4x divider 010 = 3x divider 010 = 3x divider 001 = 2x divider000 = 1x divider Reserved: Write '1'
- bit 6-4 FPLLMUL<2:0>: PLL Multiplier bits
  - 111 = 24x multiplier 110 = 21x multiplier
  - 101 = 20x multiplier
  - 100 = 19x multiplier
  - 011 = 18x multiplier
  - 010 = 17x multiplier
  - 001 = 16x multiplier
  - 000 = 15x multiplier
- bit 3 Reserved: Write '1'

Note 1: This bit is only available on PIC32MX2XX devices.

## 28.0 INSTRUCTION SET

The PIC32MX1XX/2XX family instruction set complies with the MIPS32<sup>®</sup> Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- · Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

**Note:** Refer to *"MIPS32<sup>®</sup> Architecture for Programmers Volume II: The MIPS32<sup>®</sup> Instruction Set"* at www.imgtec.com for more information.

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp				
Param. No.	Symbol	Characteristics	Min. Typical <sup>(1)</sup> Max. Units Conditions				
		Program Flash Memory <sup>(3)</sup>					
D130	Eр	Cell Endurance	20,000	—	—	E/W	_
D131	Vpr	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	_	10	—	mA	_
	Tww	Word Write Cycle Time	—	411	—	es	See Note 4
D136	Trw	Row Write Cycle Time	—	6675	—	Cycl	See Note 2,4
D137	Тре	Page Erase Cycle Time	—	20011	—	с С	See Note 4
	TCE	Chip Erase Cycle Time	—	80180		ц Ц	See Note 4

#### TABLE 30-12: DC CHARACTERISTICS: PROGRAM MEMORY

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on FRC accuracy (See Table 30-19) and FRC tuning values (See Register 8-2).

#### TABLE 30-41: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 3):2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
CTMU CUR	RENT SOUR	CE					
CTMUI1	IOUT1	Base Range <sup>(1)</sup>	_	0.55		μA	CTMUCON<9:8> = 01
CTMUI2	IOUT2	10x Range <sup>(1)</sup>	_	5.5	_	μA	CTMUCON<9:8> = 10
CTMUI3	IOUT3	100x Range <sup>(1)</sup>	_	55		μA	CTMUCON<9:8> = 11
CTMUI4	IOUT4	1000x Range <sup>(1)</sup>	_	550	_	μA	CTMUCON<9:8> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage <sup>(1,2)</sup>		0.598	—	V	TA = +25°C, CTMUCON<9:8> = 01
				0.658	—	V	TA = +25°C, CTMUCON<9:8> = 10
			_	0.721	_	V	TA = +25°C, CTMUCON<9:8> = 11
CTMUFV2 VFVR Tem		Temperature Diode Rate of	—	-1.92		mV/ºC	CTMUCON<9:8> = 01
		Change <sup>(1,2)</sup>	—	-1.74	_	mV/ºC	CTMUCON<9:8> = 10
			_	-1.56		mV/ºC	CTMUCON<9:8> = 11

**Note 1:** Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

**2:** Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL
- **3:** The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

NOTES:

## 33.0 PACKAGING INFORMATION

## 33.1 Package Marking Information

28-Lead SOIC



#### 28-Lead SPDIP



Example



### Example



#### 28-Lead SSOP



#### 28-Lead QFN



Example



### Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	If the full N line, thus I	Aicrochip part number cannot be marked on one line, it is carried over to the next imiting the number of available characters for customer-specific information.

## Revision G (April 2015)

This revision includes the addition of the following devices:

- PIC32MX130F256B
   PIC32MX230F256B
- PIC32MX130F256D PIC32MX230F256D

The title of the document was updated to avoid confusion with the PIC32MX1XX/2XX/5XX 64/100-pin Family data sheet.

#### TABLE A-6: MAJOR SECTION UPDATES

All peripheral SFR maps have been relocated from the Memory chapter to their respective peripheral chapters.

In addition, this revision includes the following major changes as described in Table A-6, as well as minor updates to text and formatting, which were incorporated throughout the document.

Section	Update Description
32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog	Added new devices to the family features (see Table 1 and Table 2). Updated pin diagrams to include new devices (see Pin Diagrams).
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Updated these sections: 2.2 "Decoupling Capacitors", 2.3 "Capacitor on Internal Voltage Regulator (VCAP)", 2.4 "Master Clear (MCLR) Pin", 2.8.1 "Crystal Oscillator Design Consideration"
4.0 "Memory Organization"	Added Memory Map for new devices (see Figure 4-6).
14.0 "Watchdog Timer (WDT)"	New chapter created from content previously located in the Special Features chapter.
30.0 "Electrical Characteristics"	Removed parameter D312 (TSET) from the Comparator Specifications (see Table 30-12).
	Added the Comparator Voltage Reference Specifications (see Table 30-13).
	Updated Table 30-12.

### **Revision H (July 2015)**

This revision includes the following major changes as described in Table A-7, as well as minor updates to text and formatting, which were incorporated throughout the document.

#### TABLE A-7: MAJOR SECTION UPDATES

Section	Update Description
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Section 2.9 "Sosc Design Recommendation" was removed.
8.0 "Oscillator Configuration"	The Primary Oscillator (Posc) logic in the Oscillator diagram was updated (see Figure 8-1).
30.0 "Electrical Characteristics"	The Power-Down Current (IPD) DC Characteristics parameter DC40k was updated (see Table 30-7).
	Table 30-9: "DC Characteristics: I/O Pin Input Injection current           Specifications" was added.

## Revision J (April 2016)

This revision includes the following major changes as described in Table A-8, as well as minor updates to text and formatting, which were incorporated throughout the document.

## TABLE A-8: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	The PIC32MX270FDB device and Note 4 were added to TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features".
2.0 "Guidelines for Getting Started with 32-bit MCUs"	EXAMPLE 2-1: "Crystal Load Capacitor Calculation" was updated.
30.0 "Electrical Characteristics"	Parameter DO50a (Csosc) was removed from the Capacitive Loading Requirements on Output Pins AC Characteristics (see Table 30-16).
"Product Identification System"	The device mapping was updated to include type B for Software Targeting.