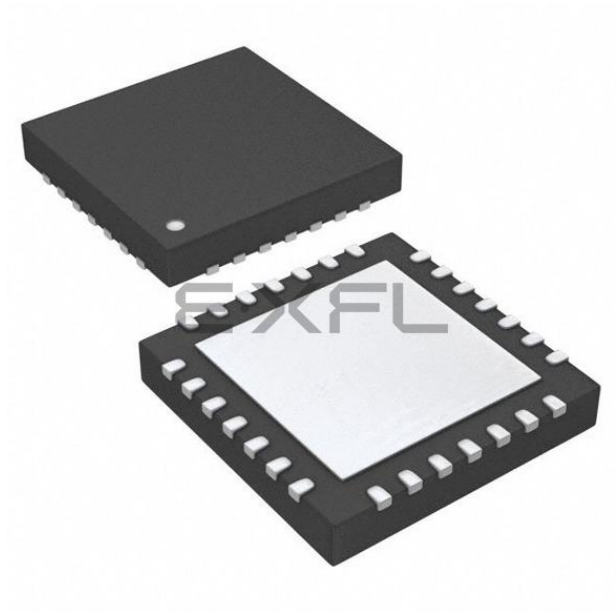
Microchip Technology - PIC32MX210F016BT-I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx210f016bt-i-ml

Pin Diagrams

TABLE 3: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES

28-PIN SOIC, SPDIP, SSOP (TOP VIEW)(1,2,3)

PIC32MX110F016B
PIC32MX120F032B
PIC32MX130F064B
PIC32MX130F256B
PIC32MX150F128B
PIC32MX170F256B

Pin #	Full Pin Name	Pin #	Full Pin Name
1	$\overline{\text{MCLR}}$	15	PGEC3/RPB6/PMD6/RB6
2	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	16	TDI/RPB7/CTED3/PMD5/INT0/RB7
3	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
4	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
5	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	19	VSS
6	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	20	VCAP
7	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	21	PGED2/RPB10/CTED11/PMD2/RB10
8	VSS	22	PGEC2/TMS/RPB11/PMD1/RB11
9	OSC1/CLKI/RPA2/RA2	23	AN12/PMD0/RB12
10	OSC2/CLKO/RPA3/PMA0/RA3	24	AN11/RPB13/CTPLS/PMRD/RB13
11	SOSCI/RPB4/RB4	25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
12	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
13	VDD	27	AVSS
14	PGED3/RPB5/PMD7/RB5	28	AVDD

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32® architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

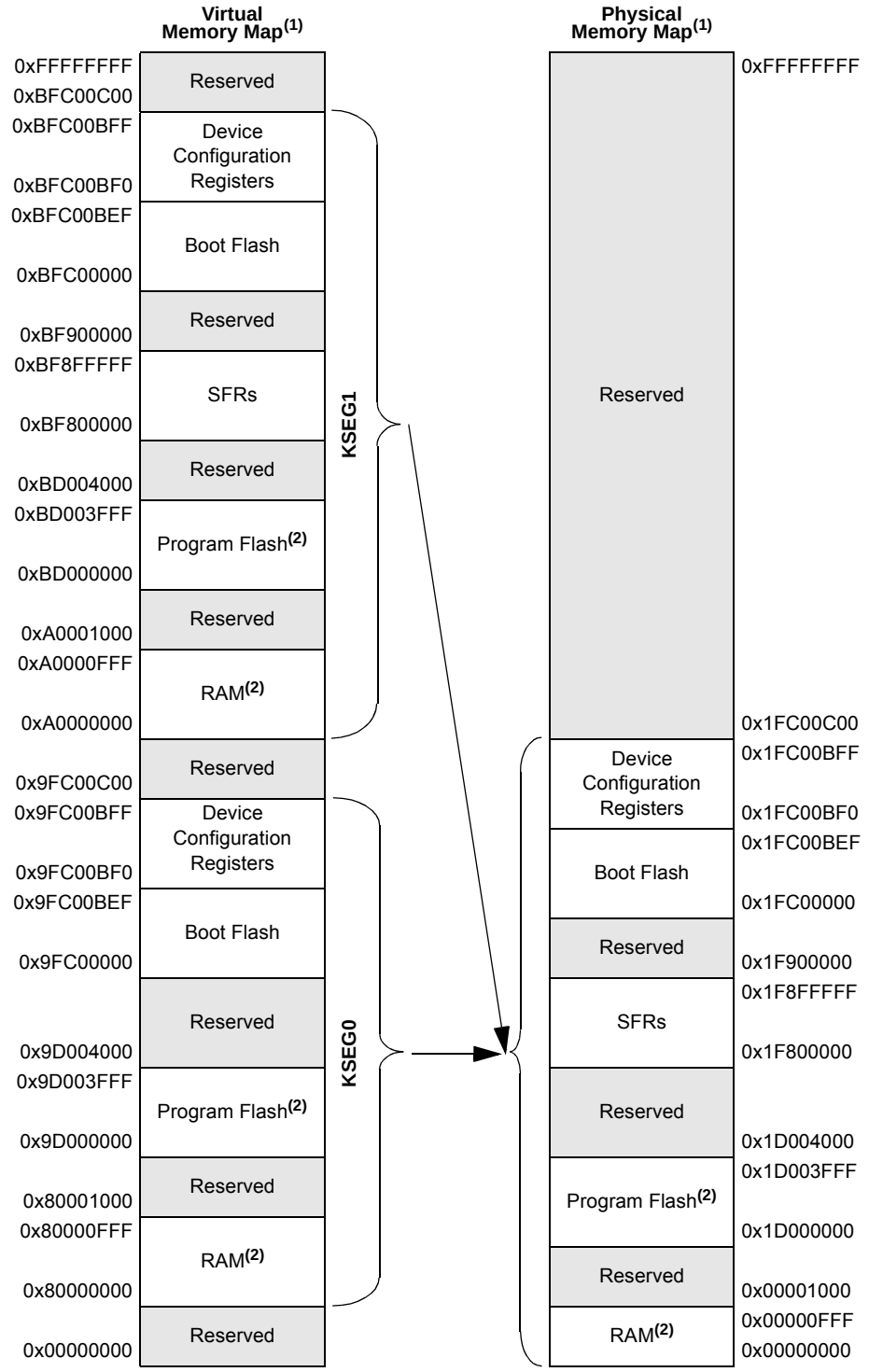
In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX1XX/2XX family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers.
8	BadVAddr(1)	Reports the address for the most recent address-related exception.
9	Count(1)	Processor cycle count.
10	Reserved	Reserved in the PIC32MX1XX/2XX family core.
11	Compare(1)	Timer interrupt control.
12	Status(1)	Processor status and control.
12	IntCtl(1)	Interrupt system status and control.
12	SRSCtl(1)	Shadow register set status and control.
12	SRSMap(1)	Provides mapping from vectored interrupt to a shadow set.
13	Cause(1)	Cause of last general exception.
14	EPC(1)	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration Register 1.
16	Config2	Configuration Register 2.
16	Config3	Configuration Register 3.
17-22	Reserved	Reserved in the PIC32MX1XX/2XX family core.
23	Debug(2)	Debug control and exception status.
24	DEPC(2)	Program counter at last debug exception.
25-29	Reserved	Reserved in the PIC32MX1XX/2XX family core.
30	ErrorEPC(1)	Program counter at last error.
31	DESAVE(2)	Debug handler scratchpad register.

Note 1: Registers used in exception processing.
2: Registers used during debug.

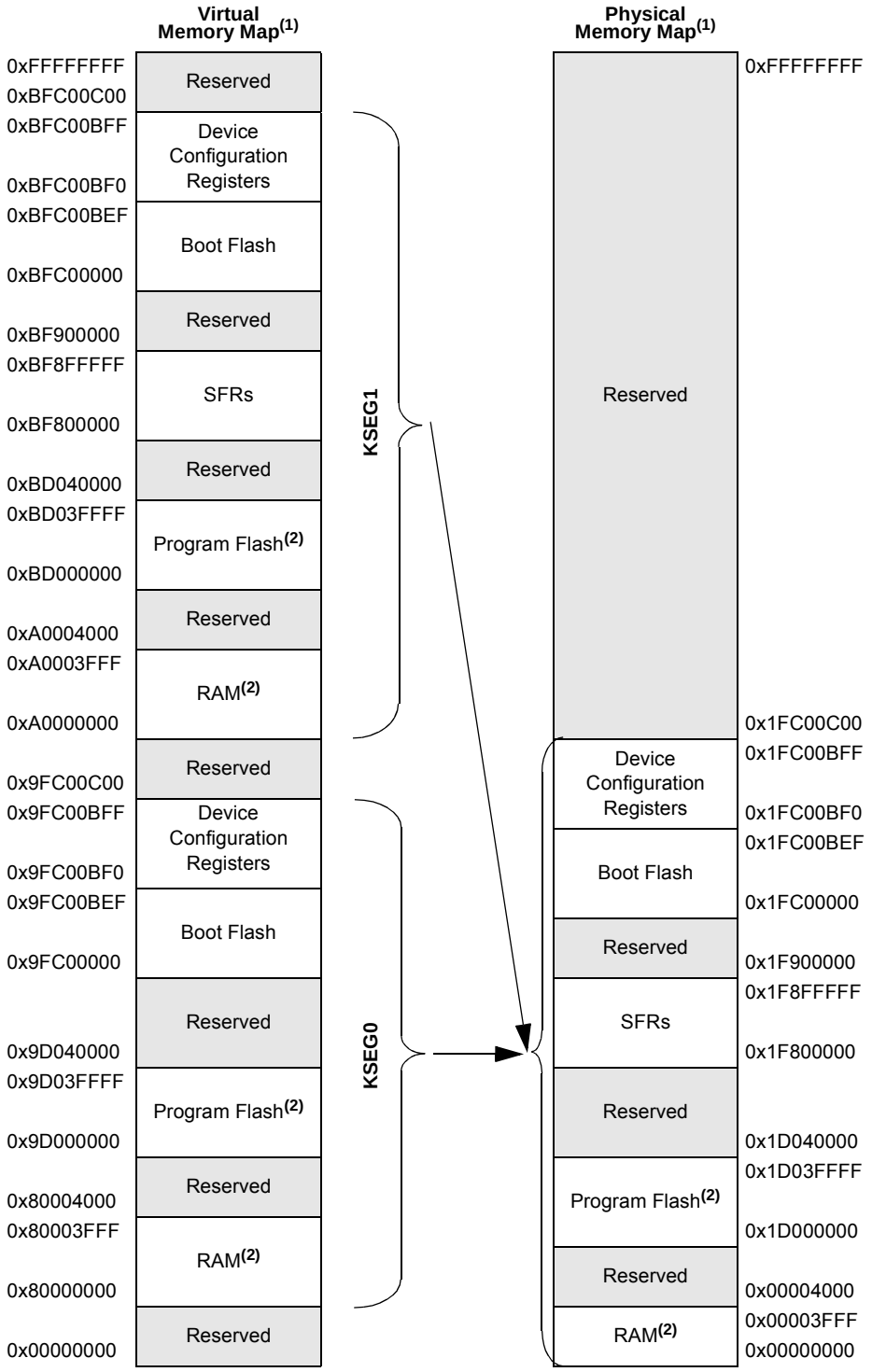
FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX110/210 DEVICES (4 KB RAM, 16 KB FLASH)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 256 KB FLASH)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-1	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1
	—	BMX WSDRM	—	—	—	BMXARB<2:0>		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **BMXERRIXI:** Enable Bus Error from IXI bit
1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus
0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus

bit 19 **BMXERRICD:** Enable Bus Error from ICD Debug Unit bit
1 = Enable bus error exceptions for unmapped address accesses initiated from ICD
0 = Disable bus error exceptions for unmapped address accesses initiated from ICD

bit 18 **BMXERRDMA:** Bus Error from DMA bit
1 = Enable bus error exceptions for unmapped address accesses initiated from DMA
0 = Disable bus error exceptions for unmapped address accesses initiated from DMA

bit 17 **BMXERRDS:** Bus Error from CPU Data Access bit (disabled in Debug mode)
1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access
0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access

bit 16 **BMXERRIS:** Bus Error from CPU Instruction Access bit (disabled in Debug mode)
1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access
0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **BMXWSDRM:** CPU Instruction or Data Access from Data RAM Wait State bit
1 = Data RAM accesses from CPU have one wait state for address setup
0 = Data RAM accesses from CPU have zero wait states for address setup

bit 5-3 **Unimplemented:** Read as '0'

bit 2-0 **BMXARB<2:0>:** Bus Matrix Arbitration Mode bits
111 = Reserved (using these Configuration modes will produce undefined behavior)
•
•
•
011 = Reserved (using these Configuration modes will produce undefined behavior)
010 = Arbitration Mode 2
001 = Arbitration Mode 1 (default)
000 = Arbitration Mode 0

REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXDRMSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXDRMSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXDRMSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXDRMSZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXDRMSZ<31:0>:** Data RAM Memory (DRM) Size bits
Static value that indicates the size of the Data RAM in bytes:
0x00001000 = Device has 4 KB RAM
0x00002000 = Device has 8 KB RAM
0x00004000 = Device has 16 KB RAM
0x00008000 = Device has 32 KB RAM
0x00010000 = Device has 64 KB RAM

REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	BMXPUPBA<19:16>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
	BMXPUPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXPUPBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-11 **BMXPUPBA<19:11>:** Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>:** Read-Only bits
This value is always '0', which forces 2 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.
2: The value in this register must be less than or equal to BMXPFMSZ.

TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
30A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

REGISTER 10-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE(1)	URSTIE(2) / DETACHIE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
- 1 = STALL interrupt is enabled
- 0 = STALL interrupt is disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit
- 1 = ATTACH interrupt is enabled
- 0 = ATTACH interrupt is disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit
- 1 = RESUME interrupt is enabled
- 0 = RESUME interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
- 1 = Idle interrupt is enabled
- 0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
- 1 = TRNIF interrupt is enabled
- 0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
- 1 = SOFIF interrupt is enabled
- 0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
- 1 = USB Error interrupt is enabled
- 0 = USB Error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
- 1 = URSTIF interrupt is enabled
- 0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit(3)
- 1 = DATTCHIF interrupt is enabled
- 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE (U1IE<1>) bit must be set.
2: Device mode.
3: Host mode.

REGISTER 10-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

REGISTER 10-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

NOTES:

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(2)		ALP(2)	—	CS1P(2)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit(1)
- 1 = PMP enabled
- 0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
- 11 = Lower 8 bits of address are multiplexed on PMD<7:0> pins; upper 8 bits are not used
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<10:8> and PMA<14>
- 00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
- 1 = PMWR/PMENB port enabled
- 0 = PMWR/PMENB port disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
- 1 = PMRD/PMWR port enabled
- 0 = PMRD/PMWR port disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
- 11 = Reserved
- 10 = PMCS1 functions as Chip Select
- 01 = PMCS1 functions as PMA<14>
- 00 = PMCS1 functions as PMA<14>

bit 5 **ALP:** Address Latch Polarity bit(2)
- 1 = Active-high (PMALL and PMALH)
- 0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 4 **Unimplemented:** Read as '0'

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 21-4: RTCDATE: RTC DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	MONTH10	MONTH01<3:0>			
15:8	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	DAY10<1:0>		DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	—	—	—	—	—	WDAY01<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **YEAR10<3:0>:** Binary-Coded Decimal Value of Years bits, 10s place digit; contains a value from 0 to 9

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1s place digit; contains a value from 0 to 9

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MONTH10:** Binary-Coded Decimal Value of Months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAY10<1:0>:** Binary-Coded Decimal Value of Days bits, 10s place digit; contains a value of 0 to 3

bit 11-8 **DAY01<3:0>:** Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY01<2:0>:** Binary-Coded Decimal Value of Weekdays bits; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	—	—	FORM<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
	SSRC<2:0>			CLRASAM	—	ASAM	SAMP(2)	DONE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit(1)
- 1 = ADC module is operating
- 0 = ADC module is not operating

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits
- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
- 000 =Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.

3: This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits
- 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
- 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-12 **FPBDIV<1:0>:** Peripheral Bus Clock Divisor Default Value bits
- 11 = PBCLK is SYSCLK divided by 8
- 10 = PBCLK is SYSCLK divided by 4
- 01 = PBCLK is SYSCLK divided by 2
- 00 = PBCLK is SYSCLK divided by 1

bit 11 **Reserved:** Write '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit
- 1 = CLKO output disabled
- 0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits
- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock mode is selected

bit 7 **IESO:** Internal External Switchover bit
- 1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
- 0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **Reserved:** Write '1'

bit 5 **FSOSCEN:** Secondary Oscillator Enable bit
- 1 = Enable Secondary Oscillator
- 0 = Disable Secondary Oscillator

bit 4-3 **Reserved:** Write '1'

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
- 111 = Fast RC Oscillator with divide-by-N (FRCDIV)
- 110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (POSC) with PLL module (XT+PLL, HS+PLL, EC+PLL)
- 010 = Primary Oscillator (XT, HS, EC)(1)
- 001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
- 000 = Fast RC Oscillator (FRC)

Note 1: Do not disable the POSC (POSCMOD = 11) when using this oscillator source.

REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FVBUSONIO:** USB VBUSON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function

bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDI1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27-16 **Reserved:** Write '1'

bit 15-0 **USERID<15:0>:** User ID bits
This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

30.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX 28/36/44-pin Family AC characteristics and timing parameters.

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

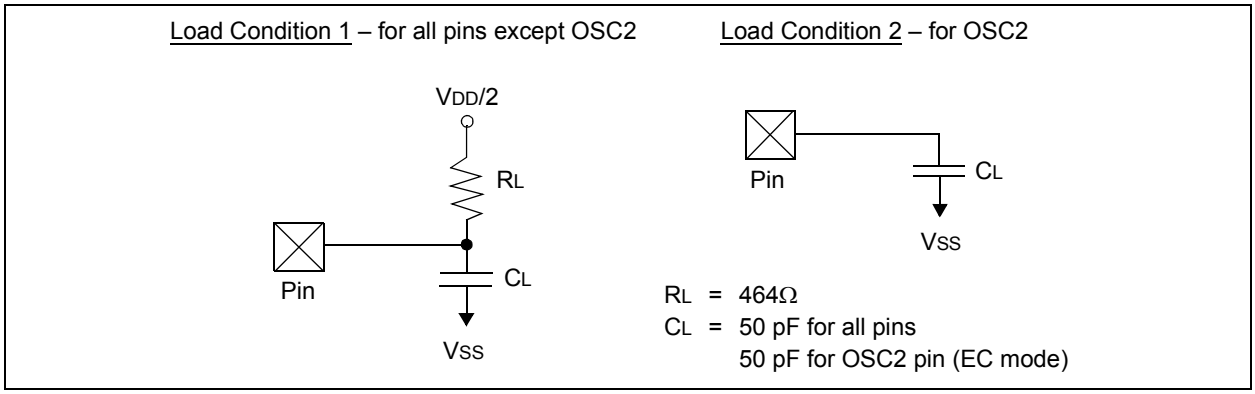


TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO56	CIO	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-2: EXTERNAL CLOCK TIMING

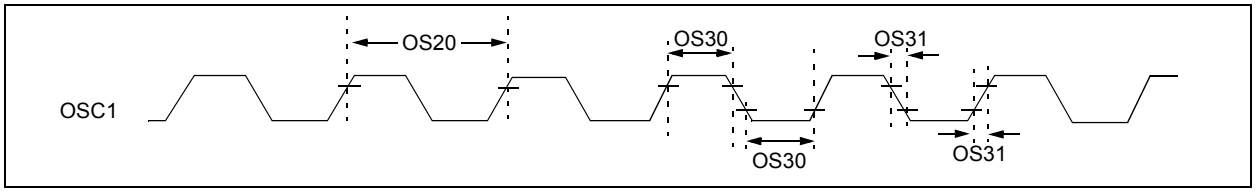


TABLE 31-5: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
MOS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	50 50	MHz MHz	EC **(Note 2)** ECPLL **(Note 1)**

Note 1: PLL input requirements: 4 MHz ≤ FPLLIN ≤ 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 31-6: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
MSP10	TscL	SCKx Output Low Time **(Note 1,2)**	TSCK/2	—	—	ns	—
MSP11	TscH	SCKx Output High Time **(Note 1,2)**	TSCK/2	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

TABLE 31-7: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MSP10	TscL	SCKx Output Low Time **(Note 1,2)**	TSCK/2	—	—	ns	—
MSP11	TscH	SCKx Output High Time **(Note 1,2)**	TSCK/2	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 32-1: I/O OUTPUT VOLTAGE HIGH (VOH)

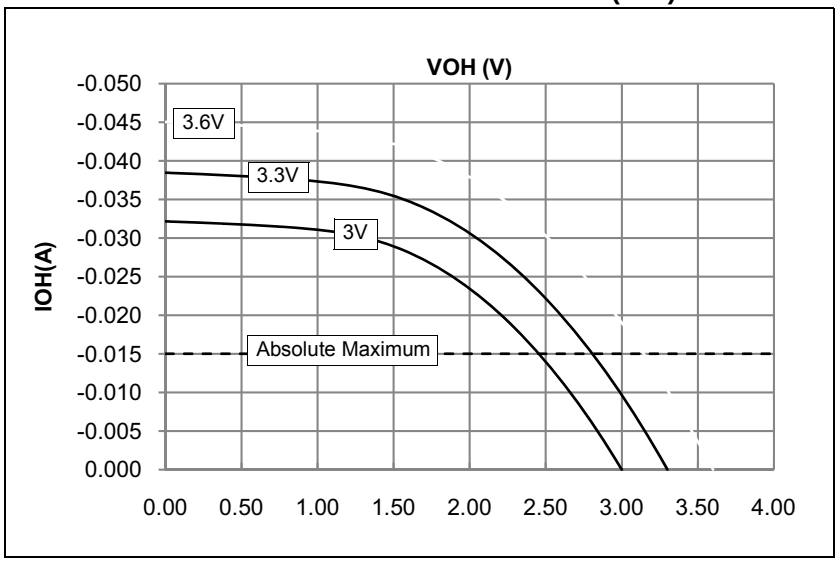


FIGURE 32-2: I/O OUTPUT VOLTAGE LOW (VOL)

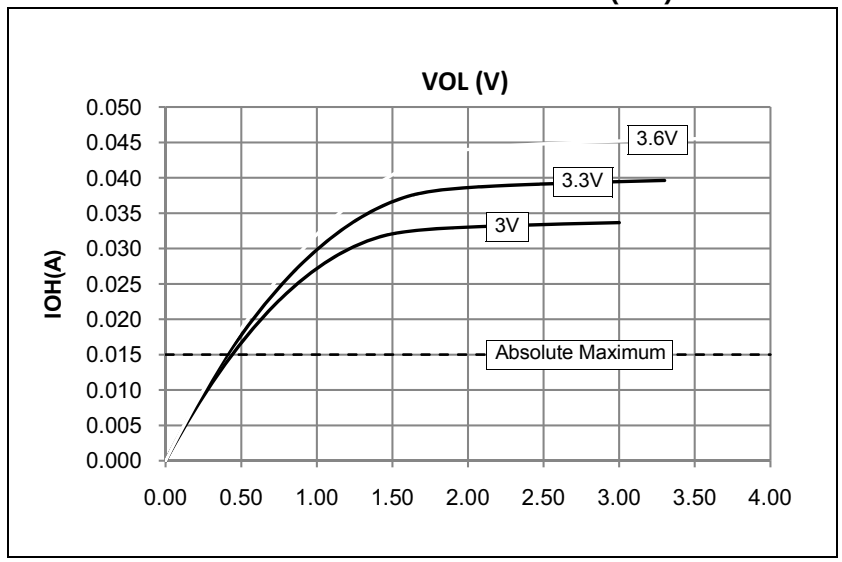


TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section	Update Description
4.0 "Memory Organization"	Added Memory Maps for the new devices (see Figure 4-3 and Figure 4-4). Removed the BMXCHEDMA bit from the Bus Matrix Register map (see Table 4-1). Added the REFOTRIM register, added the DIVSWEN bit to the REFOCON registers, added Note 4 to the ULOCK and SOSCEN bits and added the PBDIVRDY bit in the OSCCON register in the in the System Control Register map (see Table 4-16). Removed the ALTI2C1 and ALTI2C2 bits from the DEVCFG3 register and added Note 1 to the UPLLEN and UPLLIDIV<2:0> bits of the DEVCFG2 register in the Device Configuration Word Summary (see Table 4-17). Updated Note 1 in the Device and Revision ID Summary (see Table 4-18). Added Note 2 to the PORTA Register map (see Table 4-19). Added the ANSB6 and ANSB12 bits to the ANSELB register in the PORTB Register map (see Table 4-20). Added Notes 2 and 3 to the PORTC Register map (see Table 4-21). Updated all register names in the Peripheral Pin Select Register map (see Table 4-23). Added values in support of new devices (16 KB RAM and 32 KB RAM) in the Data RAM Size register (see Register 4-5). Added values in support of new devices (64 KB Flash and 128 KB Flash) in the Data RAM Size register (see Register 4-5).
8.0 "Oscillator Configuration"	Added Note 5 to the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1). Added the PBDIVRDY bit and Note 2 to the Oscillator Control register (see Register 8-1). Added the DIVSWEN bit and Note 3 to the Reference Oscillator Control register (see Register 8-3). Added the REFOTRIM register (see Register 8-4).
21.0 "10-bit Analog-to-Digital Converter (ADC)"	Updated the ADC1 Module Block Diagram (see Figure 21-1). Updated the Notes in the ADC Input Select register (see Register 21-4).
24.0 "Charge Time Measurement Unit (CTMU)"	Updated the CTMU Block Diagram (see Figure 24-1). Added Note 3 to the CTMU Control register (see Register 24-1)
26.0 "Special Features"	Added Note 1 and the PGEC4/PGED4 pin pair to the ICESEL<1:0> bits in DEVCFG0: Device Configuration Word 0 (see Register 26-1). Removed the ALTI2C1 and ALTI2C2 bits from the Device Configuration Word 3 register (see Register 26-4). Removed 26.3.3 "Power-up Requirements". Added Note 3 to the Connections for the On-Chip Regulator diagram (see Figure 26-2). Updated the Block Diagram of Programming, Debugging and Trace Ports diagram (see Figure 26-3).