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Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx210f016dt-v-tl

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUs

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX 28/36/44-pin Family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see 2.2 “Decoupling Capacitors”)
- All AVDD and AVSS pins, even if the ADC module is not used (see 2.2 “Decoupling Capacitors”)
- VCAP pin (see 2.3 “Capacitor on Internal Voltage Regulator (VCAP)”)
- MCLR pin (see 2.4 “Master Clear (MCLR) Pin”)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see 2.5 “ICSP Pins”)
- OSC1 and OSC2 pins, when external oscillator source is used (see 2.7 “External Oscillator Pins”)

The following pins may be required:

- VREF+/VREF- pins – used when external voltage reference for the ADC module is implemented

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 μF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

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REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDKPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDKPBA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits

When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** Read-Only bits

This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST ⁽¹⁾

Legend:

HC = Cleared by hardware

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit⁽¹⁾

1 = Enable Software Reset event

0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit is written. Refer to **Section 6. "Oscillator"** (DS60001168J) in the *"PIC32 Family Reference Manual"* for details.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-y	R/W-y	R/W-y	R/W-0	R/W-0	R/W-1
	—	—	PLLODIV<2:0>			FRCDIV<2:0>		
23:16	U-0	R-0	R-1	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>		
15:8	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-y	R/W-0
	CLKLOCK	ULOCK ⁽¹⁾	SLOCK	SLPEN	CF	UFRocen ⁽¹⁾	SOSCEN	OSWEN

Legend: y = Value set from Configuration bits on POR
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2 (default setting)
- 000 = FRC divided by 1

bit 23 **Unimplemented:** Read as '0'

bit 22 **SOSCRDY:** Secondary Oscillator (Sosc) Ready Indicator bit

- 1 = The Secondary Oscillator is running and is stable
- 0 = The Secondary Oscillator is still warming up or is turned off

bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit

- 1 = PBDIV<1:0> bits can be written
- 0 = PBDIV<1:0> bits cannot be written

bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits

- 11 = PBCLK is SYSCLK divided by 8 (default)
- 10 = PBCLK is SYSCLK divided by 4
- 01 = PBCLK is SYSCLK divided by 2
- 00 = PBCLK is SYSCLK divided by 1

Note 1: This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the "PIC32 Family Reference Manual" for details.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

- bit 3 **CF:** Clock Fail Detect bit
 1 = FSCM has detected a clock failure
 0 = No clock failure has been detected
- bit 2 **UFRCE:** USB FRC Clock Enable bit⁽¹⁾
 1 = Enable the FRC as the clock source for the USB clock source
 0 = Use the Primary Oscillator or USB PLL as the USB clock source
- bit 1 **SOSCEN:** Secondary Oscillator (Sosc) Enable bit
 1 = Enable the Secondary Oscillator
 0 = Disable the Secondary Oscillator
- bit 0 **OSWEN:** Oscillator Switch Enable bit
 1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
 0 = Oscillator switch is complete

Note 1: This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. “Oscillator”** (DS60001112) in the *“PIC32 Family Reference Manual”* for details.

TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
30A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000

Legend: × = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.

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REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

- bit 6 **CRCAPP:** CRC Append Mode bit⁽¹⁾
 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5 **CRCTYP:** CRC Type Selection bit
 1 = The CRC module will calculate an IP header checksum
 0 = The CRC module will calculate a LFSR CRC
- bit 4-3 **Unimplemented:** Read as '0'
- bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
 111 = CRC is assigned to Channel 7
 110 = CRC is assigned to Channel 6
 101 = CRC is assigned to Channel 5
 100 = CRC is assigned to Channel 4
 011 = CRC is assigned to Channel 3
 010 = CRC is assigned to Channel 2
 001 = CRC is assigned to Channel 1
 000 = CRC is assigned to Channel 0

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/W-0 BTSEE	R/W-0 BMXEE	R/W-0 DMAEE	R/W-0 BTOEE	R/W-0 DFN8EE	R/W-0 CRC16EE	R/W-0 CRC5EE ⁽¹⁾ EOFEE ⁽²⁾	R/W-0 PIDEE

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit

1 = BTSEF interrupt is enabled

0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit

1 = BMXEF interrupt is enabled

0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit

1 = DMAEF interrupt is enabled

0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit

1 = BTOEF interrupt is enabled

0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit

1 = DFN8EF interrupt is enabled

0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit

1 = CRC16EF interrupt is enabled

0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit⁽¹⁾

1 = CRC5EF interrupt is enabled

0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit⁽²⁾

1 = EOF interrupt is enabled

0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit

1 = PIDEF interrupt is enabled

0 = PIDEF interrupt is disabled

Note 1: Device mode.

2: Host mode.

Note: For an interrupt to propagate the USBIF register, the UERRIE (U1IE<1>) bit must be set.

TABLE 11-4: PORTB REGISTER MAP

Virtual Address (BF88.#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB15	ANSB14	ANSB13	ANSB12 ⁽²⁾	—	—	—	—	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	E00F
6110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12 ⁽²⁾	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6 ⁽²⁾	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12 ⁽²⁾	RB11	RB10	RB9	RB8	RB7	RC6 ⁽²⁾	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
6130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12 ⁽²⁾	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6 ⁽²⁾	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
6140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12 ⁽²⁾	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
6150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12 ⁽²⁾	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6 ⁽²⁾	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
6160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12 ⁽²⁾	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6 ⁽²⁾	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
6170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB15	CNIEB14	CNIEB13	CNIEB11 ⁽²⁾	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6 ⁽²⁾	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
6190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12 ⁽²⁾	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6 ⁽²⁾	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.
- 2:** This bit is not available on PIC32MX2XX devices. The reset value for the TRISB register when this bit is not available is 0x0000EFBF.

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REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 FRMEN	R/W-0 FRMSYNC	R/W-0 FRMPOL	R/W-0 MSSEN	R/W-0 FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0 MCLKSEL ⁽²⁾	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 SPIFE	R/W-0 ENHBUF ⁽²⁾
15:8	R/W-0 ON ⁽¹⁾	U-0 —	R/W-0 SIDL	R/W-0 DISSDO	R/W-0 MODE32	R/W-0 MODE16	R/W-0 SMP	R/W-0 CKE ⁽³⁾
7:0	R/W-0 SSEN	R/W-0 CKP ⁽⁴⁾	R/W-0 MSTEN	R/W-0 DISSDI	R/W-0 STXISEL<1:0>	R/W-0 SRXISEL<1:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled (\overline{SSx} pin used as FSYNC input/output)
0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on \overline{SSx} pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)
- bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low
- bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The \overline{SS} pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.
- bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in FRAMED_SYNC mode.
111 = Reserved; do not use
110 = Reserved; do not use
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character
- bit 23 **MCLKSEL:** Master Clock Enable bit⁽²⁾
1 = REFCLK is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator
- bit 22-18 **Unimplemented:** Read as '0'

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLOCK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit can only be written when the ON bit = 0.
- 3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

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19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

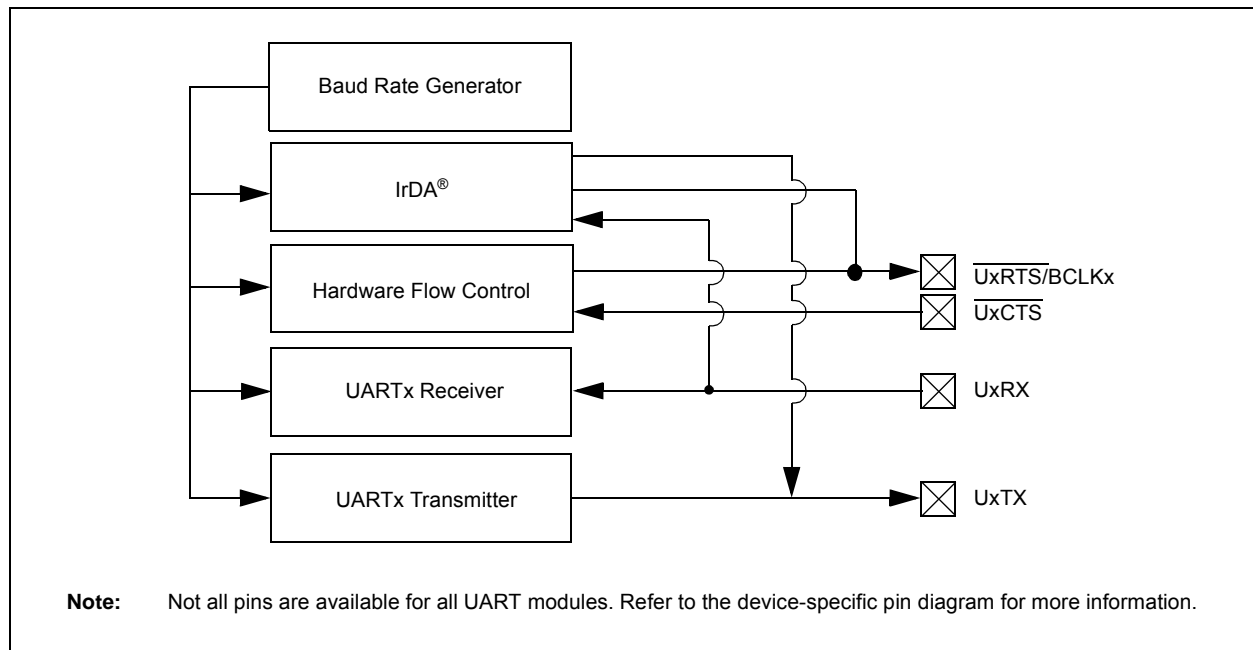
The UART module is one of the serial I/O modules available in PIC32MX1XX/2XX 28/36/44-pin Family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The UART module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

Key features of the UART module include:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 38 bps to 12.5 Mbps at 50 MHz
- 8-level deep First In First Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 19-1 illustrates a simplified block diagram of the UART module.

FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM



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REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R-0 BUSY	R/W-0 IRQM<1:0>	R/W-0 IRQM<1:0>	R/W-0 INCM<1:0>	R/W-0 INCM<1:0>	U-0 —	R/W-0 MODE<1:0>	R/W-0 MODE<1:0>
7:0	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITE<1:0> ⁽¹⁾	R/W-0 WAITE<1:0> ⁽¹⁾

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)

1 = Port is busy

0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

11 = Reserved, do not use

10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> = 11 (Addressable Slave mode only)

01 = Interrupt generated at the end of the read/write cycle

00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits

11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)

10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾

01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾

00 = No increment or decrement of address

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits

11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)

10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)

01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)

00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits⁽¹⁾

11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB

10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB

01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB

00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits⁽¹⁾

1111 = Wait of 16 TPB

.

.

.

0001 = Wait of 2 TPB

0000 = Wait of 1 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

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The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

26.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

Note 1: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a Posc of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.

- 2: Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from Posc to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to Posc, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

26.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

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REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
	—	—	—	—	—	—	FWDTWINSZ<1:0>	
23:16	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits

11 = Window size is 25%
 10 = Window size is 37.5%
 01 = Window size is 50%
 00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit

1 = Watchdog Timer is enabled and cannot be disabled by software
 0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit

1 = Watchdog Timer is in non-Window mode
 0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576
 10011 = 1:524288
 10010 = 1:262144
 10001 = 1:131072
 10000 = 1:65536
 01111 = 1:32768
 01110 = 1:16384
 01101 = 1:8192
 01100 = 1:4096
 01011 = 1:2048
 01010 = 1:1024
 01001 = 1:512
 01000 = 1:256
 00111 = 1:128
 00110 = 1:64
 00101 = 1:32
 00100 = 1:16
 00011 = 1:8
 00010 = 1:4
 00001 = 1:2
 00000 = 1:1
 All other combinations not shown result in operation = 10100

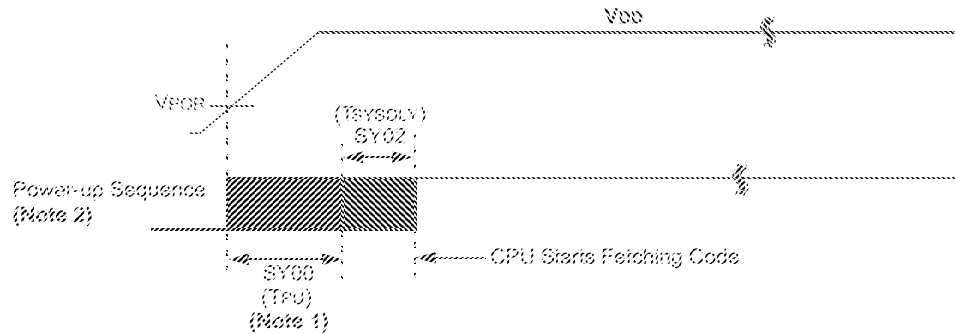
Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

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FIGURE 30-4: POWER-ON RESET TIMING CHARACTERISTICS

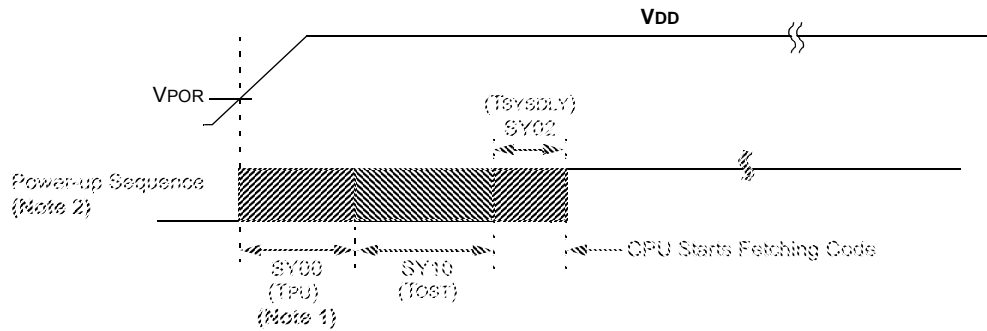
Internal Voltage Regulator Enabled

Clock Sources = {FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC}



Internal Voltage Regulator Enabled

Clock Sources = {HS, HSPLL, XT, XTPLL and Sosc}



Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($VDD < VDDMIN$).

2: Includes interval voltage regulator stabilization delay.

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TABLE 30-41: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
CTMU CURRENT SOURCE							
CTMUI1	IOUT1	Base Range ⁽¹⁾	—	0.55	—	μA	CTMUCON<9:8> = 01
CTMUI2	IOUT2	10x Range ⁽¹⁾	—	5.5	—	μA	CTMUCON<9:8> = 10
CTMUI3	IOUT3	100x Range ⁽¹⁾	—	55	—	μA	CTMUCON<9:8> = 11
CTMUI4	IOUT4	1000x Range ⁽¹⁾	—	550	—	μA	CTMUCON<9:8> = 00
CTMUUFV1	VF	Temperature Diode Forward Voltage ^(1,2)	—	0.598	—	V	T _A = +25°C, CTMUCON<9:8> = 01
			—	0.658	—	V	T _A = +25°C, CTMUCON<9:8> = 10
			—	0.721	—	V	T _A = +25°C, CTMUCON<9:8> = 11
CTMUUFV2	VFVR	Temperature Diode Rate of Change ^(1,2)	—	-1.92	—	mV/°C	CTMUCON<9:8> = 01
			—	-1.74	—	mV/°C	CTMUCON<9:8> = 10
			—	-1.56	—	mV/°C	CTMUCON<9:8> = 11

Note 1: Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksp/s
- All PMD bits are cleared (PMDx = 0)
- Executing a `while(1)` statement
- Device operating from the FRC with no PLL

3: The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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TABLE 31-8: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
MSP70	TsCL	SCKx Input Low Time (Note 1,2)	$T_{SCK}/2$	—	—	ns	—
MSP71	TsCH	SCKx Input High Time (Note 1,2)	$T_{SCK}/2$	—	—	ns	—
MSP51	TssH2boZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance (Note 2)	5	—	25	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns.

TABLE 31-9: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
SP70	TsCL	SCKx Input Low Time (Note 1,2)	$T_{SCK}/2$	—	—	ns	—
SP71	TsCH	SCKx Input High Time (Note 1,2)	$T_{SCK}/2$	—	—	ns	—

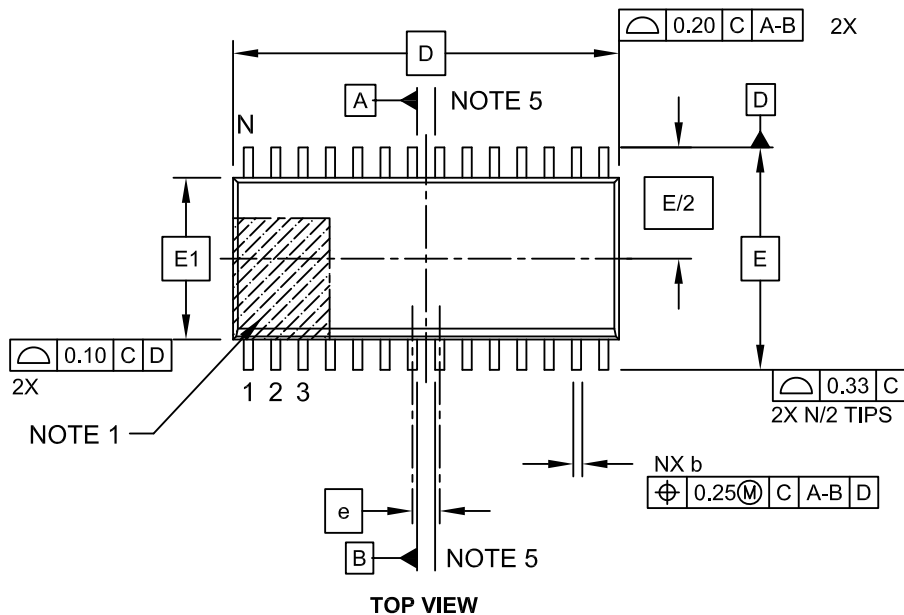
Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Revision E (October 2012)

All singular pin diagram occurrences of CVREF were changed to: CVREFOUT. In addition, minor text and formatting changes were incorporated throughout the document.

All major changes are referenced by their respective section in Table A-4.

TABLE A-4: MAJOR SECTION UPDATES

Section	Update Description
“32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog”	Updated the following feature sections: <ul style="list-style-type: none">• “Operating Conditions”• “Communication Interfaces”
2.0 “Guidelines for Getting Started with 32-bit MCUs”	Removed Section 2.8 “Configuration of Analog and Digital Pins During ICSP Operations”.
3.0 “CPU”	Removed references to GPR shadow registers in 3.1 “Features” and 3.2.1 “Execution Unit” .
4.0 “Memory Organization”	Updated the BRG bit range in the SPI1 and SPI2 Register Map (see Table 4-8). Added the PWP<6> bit to the Device Configuration Word Summary (see Table 4-17).
5.0 “Flash Program Memory”	Added a note with Flash page size and row size information.
7.0 “Interrupt Controller”	Updated the TPC<2:0> bit definitions (see Register 7-1). Updated the IPTMR<31:0> bit definition (see Register 7-3).
8.0 “Oscillator Configuration”	Updated the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1). Updated the RODIV<14:0> bit definitions (see Register 8-3).
10.0 “USB On-The-Go (OTG)”	Updated the Notes in the USB Interface Diagram (see Figure 10-1).
18.0 “Universal Asynchronous Receiver Transmitter (UART)”	Updated the baud rate range in the list of primary features.
26.0 “Special Features”	Added the PWP<6> bit to the Device Configuration Word 0 (see Register 26-1).
29.0 “Electrical Characteristics”	Added Note 1 to Operating MIPS vs. Voltage (see Table 29-1). Added Note 2 to DC Temperature and Voltage Specifications (see Table 29-4). Updated the Conditions for parameter DC25 in DC Characteristics: Operating Current (IDD) (see Table 29-5). Added Note 2 to Electrical Characteristics: BOR (see Table 29-10). Added Note 4 to Comparator Specifications (see Table 29-12). Added Note 5 to ADC Module Specifications (see Table 29-32). Updated the 10-bit Conversion Rate Parameters and added Note 3 (see Table 29-33). Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 29-34). Added Note 3 to CTMU Current Source Specifications (see Table 29-39).
30.0 “50 MHz Electrical Characteristics”	New chapter with electrical characteristics for 50 MHz devices.
31.0 “Packaging Information”	The 36-pin and 44-pin VTLA packages have been updated.

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NOTES: