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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx220f032bt-50i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). This document contains device-specific information for PIC32MX1XX/2XX 28/36/44-pin Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/36/44-pin Family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.



FIGURE 1-1: BLOCK DIAGRAM



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 μF to 47 μF . This capacitor should be located as close to the device as possible.

2.3 Capacitor on Internal Voltage Regulator (VCAP)

2.3.1 INTERNAL REGULATOR MODE

A low-ESR (3 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **30.0 "Electrical Characteristics"** for additional information on CEFC specifications.

2.4 Master Clear (MCLR) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions:

- Device Reset
- Device programming and debugging

Pulling The $\overline{\text{MCLR}}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{\text{MCLR}}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.



EXAMPLE OF MCLR PIN CONNECTIONS



3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	—	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	_	—	_	—	—	_	_	_			
15:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
15:8	_	_	_	—	—	—	_	—			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC			
7:0	_	_	_	_	_	_	_	SWRST ⁽¹⁾			

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Legend: HC = Cleared by hardware							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-1 Unimplemented: Read as '0'

- bit 0 SWRST: Software Reset Trigger bit⁽¹⁾ 1 = Enable Software Reset event
 - 0 = No effect
- Note 1: The system unlock sequence must be performed before the SWRST bit is written. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
					RDWR	DMACH<2:0>		

REGISTER 9-2: DMASTAT: DMA STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-4 Unimplemented: Read as '0'

- bit 3 RDWR: Read/Write Status bit
 - 1 = Last DMA bus access was a read
 - 0 = Last DMA bus access was a write
- bit 2-0 **DMACH<2:0>:** DMA Channel bits These bits contain the value of the most recent active DMA channel.

REGISTER 9-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
31:24	DMAADDR<31:24>										
00.40	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
23:10	DMAADDR<23:16>										
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
10.0	DMAADDR<15:8>										
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
				DMAADD	R<7:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 DMAADDR<31:0>: DMA Module Address bits

These bits contain the address of the most recent DMA access.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	_	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	_	—	—
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
15:8	CHBUSY	—	—	—	—	_	_	CHCHNS ⁽¹⁾
7.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
7:0	CHEN ⁽²⁾	CHAED	CHCHN	CHAEN	—	CHEDET	CHPF	RI<1:0>

REGISTER 9-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-16 Unimplemented: Read as '0'

- bit 15 CHBUSY: Channel Busy bit
 - 1 = Channel is active or has been enabled
 - 0 = Channel is inactive or has been disabled
- bit 14-9 Unimplemented: Read as '0'
- bit 8 CHCHNS: Chain Channel Selection bit⁽¹⁾
 - 1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
 - 0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 CHEN: Channel Enable bit⁽²⁾

- 1 = Channel is enabled
- 0 = Channel is disabled

bit 6 CHAED: Channel Allow Events If Disabled bit

- 1 = Channel start/abort events will be registered, even if the channel is disabled
- 0 = Channel start/abort events will be ignored if the channel is disabled

bit CHCHN: Channel Chain Enable bit

- 1 = Allow channel to be chained
- 0 = Do not allow channel to be chained
- bit 4 CHAEN: Channel Automatic Enable bit
 - 1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
 0 = Channel is disabled on block transfer complete

bit 3 Unimplemented: Read as '0'

- bit 2 CHEDET: Channel Event Detected bit
 - 1 = An event has been detected
 - 0 = No events have been detected
- bit 1-0 CHPRI<1:0>: Channel Priority bits
 - 11 = Channel has priority 3 (highest)
 - 10 = Channel has priority 2
 - 01 = Channel has priority 1
 - 00 = Channel has priority 0
- Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).
 - 2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP

SS										В	its								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
EBOO		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	_	0000
1 800	NEAUN	15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPAC	<3:0>		0000
FB04	RPA1R	31:16	_	_	—	—	—	_		—			—	—	—		—	—	0000
1 004	NAIN	15:0	_	_	—	—	—	_		—			—	—		RPA1	<3:0>		0000
FB08	RPA2R	31:16	_	—	—	—	—	—	—	_			—	_	—	—	—	_	0000
1 000		15:0	_	—	—	—	—	—	—	_			—	_		RPA2	<3:0>		0000
FB0C	RPA3R	31:16	—	—	—	—	—	—	-	—	—	—	—	—	—	—	—	—	0000
1 800		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPA3	<3:0>		0000
FB10	RPA4R	31:16	—	-	—	—	—	-	-	—	—	—	-	—	—	—	—	—	0000
1 0 10		15:0	—	-	—	—	—	-	-	—	—	—	-	—		RPA4	<3:0>		0000
FB20	RPA8R(1)	31:16			—	—	—			—			—	—	—	—	—	—	0000
1 020		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPA8	<3:0>		0000
FB24	RPA9R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—			—	0000
1 02 1		15:0			—	—	—			—			—	—		RPAS	<3:0>		0000
FB2C	RPB0R	31:16	_		—	—	—			—	_	_		—	—	—	—	—	0000
. 520		15:0	_		—	—	—			—	_	_		—		RPBC	<3:0>		0000
FB30	RPB1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPB1	<3:0>		0000
FB34	RPB2R	31:16	—		—					—	—	—		—	—	—	—	—	0000
		15:0	—	—		—	—	—		—	—	—		—		RPB2	2<3:0>		0000
FB38	RPB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—					0000
		15:0	—		—					—	—	—		—		RPB3	<3:0>		0000
FB3C	RPB4R	31:16	—		—					—	—	—		—	—	—	—	—	0000
		15:0	—		—					—	—	—		—		RPB4	<3:0>		0000
FB40	RPB5R	31:16			_					—				—	—		—	—	0000
		15:0	—		—					—	—	—		—		RPB5	5<3:0>		0000
FB44	RPB6R ⁽²⁾	31:16	—		—					—	—	—		—	—		_	—	0000
		15:0	—	-	—	-	-	-	-	—	—	—	-	—		RPB6	6<3:0>		0000
FB48	RPB7R	31:16	—	-	—	-	-	-	-	—	—	—	-	—	—	—	—	—	0000
	15:0	—	—	—	—	—	—	—	—	—	—	—	—	1	RPB7	'<3:0>		0000	

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x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

This register is only available on 44-pin devices. Note 1:

2: This register is only available on PIC32MX1XX devices.

3: This register is only available on 36-pin and 44-pin devices. PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	_	—	_	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:10	—	_	—	—	—	—	—	—		
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
10.0	—	_	—	—	—	—	—	—		
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0	_	—	_	_		[pin name]R<3:0>				

REGISTER 11-1: [pin name]R: PERIPHERAL PIN SELECT INPUT REGISTER

Legend:

Logona.						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-4 Unimplemented: Read as '0'

bit 3-0 [*pin name*]R<3:0>: Peripheral Pin Select Input bits Where [*pin name*] refers to the pins that are used to configure peripheral input mapping. See Table 11-1 for input pin selection values.

Note: Register values can only be changed if the Configuration bit, IOLOCK (CFGCON<13>), = 0.

REGISTER 11-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	_	—	_		_	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	_	—	_	—	_	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	—	_	—	_	—	_	—
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0						RPnR	<3:0>	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 Unimplemented: Read as '0'

bit 3-0 **RPnR<3:0>:** Peripheral Pin Select Output bits See Table 11-2 for output pin selection values.

Note: Register values can only be changed if the Configuration bit, IOLOCK (CFGCON<13>), = 0.

18.0 INTER-INTEGRATED CIRCUIT (I²C)

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 24. "Inter-
	Integrated Circuit (I ² C)" (DS60001116),
	which is available from the Documentation
	> Reference Manual section of the Micro-
	chip PIC32 web site
	(www.microchip.com/pic32).

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard. Figure 18-1 illustrates the I^2C module block diagram.

Each I^2C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module offers the following key features:

- I²C interface supporting both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation; detects bus collision and arbitrates accordingly
- · Provides support for address bit masking

20.1 PMP Control Registers

TABLE 20-1: PARALLEL MASTER PORT REGISTER MAP

ess		0		Bits															
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
7000	7000 PMCON 31:	31:16		_	—	—	—	—	—	—		—	—			—	_	—	0000
7000	FINCON	15:0	ON	_	SIDL	ADRMU	JX<1:0>	PMPTTL	PTWREN	PTRDEN	CSF	<1:0>	ALP	_	CS1P	—	WRSP	RDSP	0000
7010		31:16	—	_	—	—	_	_	_	—	_	—	_	_	_	_	_	—	0000
7010	PININODE	15:0	BUSY	BUSY IRQM<1:0> INCM		<1:0>	— MODE<1:0>		WAITB<1:0> WAI		WAITN	AITM<3:0>		WAITE	=<1:0>	0000			
		31:16	—	_	_	—	_	_	_	_	_	—	_	_	_	—	_	—	0000
7020	PMADDR	45.0		CS1															0000
		15:0	_	ADDR14	_	_	_					/	ADDR<10:0	>					
7000		31:16								DATAOU	T -04-05								0000
7030	PIVIDOUT	15:0								DATAOU	1<31.0>								0000
7040		31:16									1-21:05								0000
7040	PIVIDIN	15:0								DATAIN	1<31.0>								0000
7050		31:16	—	_	_	—	_	_	-	_	_	_	-	_	_	-	_	_	0000
7050	PMAEN	15:0	_	PTEN14	_	_	_						PTEN<10:0	>					0000
7000	DMOTAT	31:16		_	_	_	_	_	—	—	_	—	—	_	—	—	_	_	0000
1060	PINSTAL	15:0	IBF	IBOV	_	_	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	_	_	OB3E	OB2E	OB1E	OB0E	008F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	ADRML	JX<1:0>	PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(2)		ALP ⁽²⁾	_	CS1P ⁽²⁾	_	WRSP	RDSP

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾
 - 1 = PMP enabled
 - 0 = PMP disabled, no off-chip access performed
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when the device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode
- bit 12-11 ADRMUX<1:0>: Address/Data Multiplexing Selection bits
 - 11 = Lower 8 bits of address are multiplexed on PMD<7:0> pins; upper 8 bits are not used
 - 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
 - 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<10:8> and PMA<14>
 - 00 = Address and data appear on separate pins
- bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
 - 1 = PMP module uses TTL input buffers
 - 0 = PMP module uses Schmitt Trigger input buffer
- bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
 - 1 = PMWR/PMENB port enabled
 - 0 = PMWR/PMENB port disabled
- bit 8 PTRDEN: Read/Write Strobe Port Enable bit
 - 1 = PMRD/PMWR port enabled
 - 0 = PMRD/PMWR port disabled
- bit 7-6 CSF<1:0>: Chip Select Function bits⁽²⁾
 - 11 = Reserved
 - 10 = PMCS1 functions as Chip Select
 - 01 = PMCS1 functions as PMA<14>
 - 00 = PMCS1 functions as PMA<14>
- bit 5 ALP: Address Latch Polarity bit⁽²⁾
 - 1 = Active-high (PMALL and PMALH)
 - $0 = \text{Active-low} (\overline{\text{PMALL}} \text{ and } \overline{\text{PMALH}})$
 - **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - 2: These bits have no effect when their corresponding pins are used as address lines.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	_	-	_	_	_	—	_	—	
45.0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	
15:8	BUSY	IRQM	<1:0>	INCM	<1:0>	—	MODE<1:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	WAITB<1:0>(1)			WAITM	WAITE<1:0> ⁽¹⁾				

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **BUSY:** Busy bit (Master mode only)
 - 1 = Port is busy
 - 0 = Port is not busy

bit 14-13 IRQM<1:0>: Interrupt Request Mode bits

- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

bit 12-11 INCM<1:0>: Increment Mode bits

- 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾
- 01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾
- 00 = No increment or decrement of address
- bit 10 Unimplemented: Read as '0'
- bit 9-8 MODE<1:0>: Parallel Port Mode Select bits
 - 11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)
 - 10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)
 - 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
 - 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)
- bit 7-6 WAITB<1:0>: Data Setup to Read/Write Strobe Wait States bits⁽¹⁾
 - 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
 - 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
 - 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
 - 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

bit 5-2 WAITM<3:0>: Data Read/Write Strobe Wait States bits⁽¹⁾

- 1111 = Wait of 16 Трв •
- . 0001 = Wait of 2 Трв 0000 = Wait of 1 Трв (default)
- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

REGISTER 22-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Legend:

Logena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CSSL<15:0>: ADC Input Pin Scan Selection bits^(1,2)

1 = Select ANx for input scan

0 = Skip ANx for input scan

- **Note 1:** CSSL = ANx, where 'x' = 0-12; CSSL13 selects CTMU input for scan; CSSL14 selects IVREF for scan; CSSL15 selects Vss for scan.
 - 2: On devices with less than 13 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
15:8	ON ⁽¹⁾	COE	CPOL ⁽²⁾	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL	_<1:0>	_	CREF	_	_	CCH	<1:0>

REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER

Legend:

5					
R = Readable bit	W = Writable bit	Writable bit U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Comparator ON bit⁽¹⁾
 - 1 = Module is enabled. Setting this bit does not affect the other bits in this register
 - 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register
- bit 14 **COE:** Comparator Output Enable bit
 - 1 = Comparator output is driven on the output CxOUT pin
 - 0 = Comparator output is not driven on the output CxOUT pin
- bit 13 **CPOL:** Comparator Output Inversion bit⁽²⁾
 - 1 = Output is inverted
 - 0 = Output is not inverted
- bit 12-9 Unimplemented: Read as '0'
- bit 8 **COUT:** Comparator Output bit
 - 1 = Output of the Comparator is a '1'
 - 0 = Output of the Comparator is a '0'
- bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
 - 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
 - 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
 - 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
 - 00 = Comparator interrupt generation is disabled
- bit 5 Unimplemented: Read as '0'
- bit 4 CREF: Comparator Positive Input Configure bit
 - 1 = Comparator non-inverting input is connected to the internal CVREF
 - 0 = Comparator non-inverting input is connected to the CXINA pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Negative Input Select bits for Comparator
 - 11 = Comparator inverting input is connected to the IVREF
 - 10 = Comparator inverting input is connected to the CxIND pin
 - 01 = Comparator inverting input is connected to the CxINC pin
 - 00 = Comparator inverting input is connected to the CxINB pin
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 15-14 FCKSM<1:0>: Clock Switching and Monitor Selection Configuration bits

- 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
- 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
- bit 13-12 FPBDIV<1:0>: Peripheral Bus Clock Divisor Default Value bits
 - 11 = PBCLK is SYSCLK divided by 8
 - 10 = PBCLK is SYSCLK divided by 4
 - 01 = PBCLK is SYSCLK divided by 2
 - 00 = PBCLK is SYSCLK divided by 1
- bit 11 Reserved: Write '1'
- bit 10 OSCIOFNC: CLKO Enable Configuration bit
 - 1 = CLKO output disabled
 - 0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits

- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock mode is selected
- bit 7 IESO: Internal External Switchover bit
 - 1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
 - 0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)
- bit 6 **Reserved:** Write '1'
- bit 5 **FSOSCEN:** Secondary Oscillator Enable bit
 - 1 = Enable Secondary Oscillator
 - 0 = Disable Secondary Oscillator
- bit 4-3 Reserved: Write '1'
- bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
 - 111 = Fast RC Oscillator with divide-by-N (FRCDIV)
 - 110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
 - 101 = Low-Power RC Oscillator (LPRC)
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL)
 - 010 = Primary Oscillator (XT, HS, EC)⁽¹⁾
 - 001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
 - 000 = Fast RC Oscillator (FRC)
- **Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

NOTES:

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Conditions
Operating Voltage							
DC10	Vdd	Supply Voltage (Note 2)	2.3		3.6	V	—
DC12	VDR	RAM Data Retention Voltage (Note 1)	1.75	_	—	V	—
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	1.75	_	2.1	V	_
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.00005	_	0.115	V/μs	_

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
PM1	Tlat	PMALL/PMALH Pulse Width	—	1 Трв		—	_
PM2	Tadsu	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 Трв	_	—	_
PM3	Tadhold	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	_	1 Трв	_	_	_
PM4	Tahold	PMRD Inactive to Address Out Invalid (address hold time)	5	_	_	ns	_
PM5	Trd	PMRD Pulse Width	_	1 Трв	_		—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	_	ns	_
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	_	ns	

TABLE 30-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

Note 1: These parameters are characterized, but not tested in manufacturing.





28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Number of Pins	N	28				
Pitch	е	1.27 BSC				
Overall Height	A	-	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D	17.90 BSC				
Chamfer (Optional)	h	0.25	-	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1	1.40 REF				
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision A (May 2011)

This is the initial released version of this document.

Revision B (October 2011)

The following two global changes are included in this revision:

- All packaging references to VLAP have been changed to VTLA throughout the document
- All references to VCORE have been removed
- All occurrences of the ASCL1, ASCL2, ASDA1, and ASDA2 pins have been removed
- V-temp temperature range (-40°C to +105°C) was added to all electrical specification tables

This revision includes the addition of the following devices:

- PIC32MX130F064B
- PIC32MX130F064C
- PIC32MX130F064D
- PIC32MX150F128B
- PIC32MX150F128CPIC32MX150F128D
- PIC32MX250F128C
 PIC32MX250F128D

PIC32MX230F064B

PIC32MX230F064C

PIC32MX230F064D

PIC32MX250F128B

Text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-1.

Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio	Split the existing Features table into two: PIC32MX1XX General Purpose Family Features (Table 1) and PIC32MX2XX USB Family Features (Table 2).
and Graphics Interfaces, USB, and Advanced Analog"	Added the SPDIP package reference (see Table 1, Table 2, and " Pin Diagrams ").
	Added the new devices to the applicable pin diagrams.
	Changed PGED2 to PGED1 on pin 35 of the 36-pin VTLA diagram for PIC32MX220F032C, PIC32MX220F016C, PIC32MX230F064C, and PIC32MX250F128C devices.
1.0 "Device Overview"	Added the SPDIP package reference and updated the pin number for AN12 for 44-pin QFN devices in the Pinout I/O Descriptions (see Table 1-1).
	Added the PGEC4/PGED4 pin pair and updated the C1INA-C1IND and C2INA-C2IND pin numbers for 28-pin SSOP/SPDIP/SOIC devices in the Pinout I/O Descriptions (see Table 1-1).
2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).

TABLE A-1: MAJOR SECTION UPDATES

Revision E (October 2012)

All singular pin diagram occurrences of CVREF were changed to: CVREFOUT. In addition, minor text and formatting changes were incorporated throughout the document.

All major changes are referenced by their respective section in Table A-4.

TABLE A-4:	MAJOR SECTION UPDATES
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Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Updated the following feature sections: "Operating Conditions" "Communication Interfaces"
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Removed Section 2.8 "Configuration of Analog and Digital Pins During ICSP Operations".
3.0 "CPU"	Removed references to GPR shadow registers in 3.1 "Features" and 3.2.1 "Execution Unit" .
4.0 "Memory Organization"	Updated the BRG bit range in the SPI1 and SPI2 Register Map (see Table 4-8). Added the PWP<6> bit to the Device Configuration Word Summary (see Table 4-17).
5.0 "Flash Program Memory"	Added a note with Flash page size and row size information.
7.0 "Interrupt Controller"	Updated the TPC<2:0> bit definitions (see Register 7-1). Updated the IPTMR<31:0> bit definition (see Register 7-3).
8.0 "Oscillator Configuration"	Updated the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1). Updated the RODIV<14:0> bit definitions (see Register 8-3).
10.0 "USB On-The-Go (OTG)"	Updated the Notes in the USB Interface Diagram (see Figure 10-1).
18.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the baud rate range in the list of primary features.
26.0 "Special Features"	Added the PWP<6> bit to the Device Configuration Word 0 (see Register 26-1).
29.0 "Electrical Characteristics"	 Added Note 1 to Operating MIPS vs. Voltage (see Table 29-1). Added Note 2 to DC Temperature and Voltage Specifications (see Table 29-4). Updated the Conditions for parameter DC25 in DC Characteristics: Operating Current (IDD) (see Table 29-5). Added Note 2 to Electrical Characteristics: BOR (see Table 29-10). Added Note 4 to Comparator Specifications (see Table 29-12). Added Note 5 to ADC Module Specifications (see Table 29-32). Updated the 10-bit Conversion Rate Parameters and added Note 3 (see Table 29-33). Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 29-34). Added Note 3 to CTMU Current Source Specifications (see Table 29-39).
30.0 "50 MHz Electrical Characteristics"	New chapter with electrical characteristics for 50 MHz devices.
31.0 "Packaging Information"	The 36-pin and 44-pin VTLA packages have been updated.