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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx220f032bt-v-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 13: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

44-PIN VTLA (TOP VIEW)^(1,2,3,5)

PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	VDD
7	VCAP	29	Vss
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVdd	39	Vss
18	MCLR	40	VDD
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

44

1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

5: Shaded pins are 5V tolerant.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31:24		NVMDATA<31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23:10	NVMDATA<23:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	NVMDATA<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				NVMD	ATA<7:0>					

REGISTER 5-4: NVMDATA: FLASH PROGRAM DATA REGISTER

Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMDATA<31:0>: Flash Programming Data bits

Note: The bits in this register are only reset by a Power-on Reset (POR).

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
		NVMSRCADDR<31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23:10	NVMSRCADDR<23:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	NVMSRCADDR<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				NVMSRC	ADDR<7:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMSRCADDR<31:0>: Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				CHPDA	Γ<7:0>			

REGISTER 9-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 CHPDAT<7:0>: Channel Data Register bits

Pattern Terminate mode: Data to be matched must be stored in this register to allow a "terminate on match".

All other modes: Unused.

INPUT CAPTURE 15.0

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 15. "Input Capture" (DS60001122), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- · Simple capture event modes:
 - Capture timer value on every rising and falling edge of input at ICx pin
 - Capture timer value on every edge (rising and falling)
 - Capture timer value on every edge (rising and falling), specified edge first.

- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- · Device wake-up from capture pin during Sleep and Idle modes
- · Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- · Input capture can also be used to provide additional sources of external interrupts

Figure 15-1 illustrates a general block diagram of the Input Capture module.



NOTES:

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 23. "Serial Peripheral Interface (SPI)" (DS60001106), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontrollers. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), etc. The PIC32 SPI module is compatible with Motorola[®] SPI and SIOP interfaces. Some of the key features of the SPI module are:

- · Master mode and Slave mode support
- · Four clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
 FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- · Operation during Sleep and Idle modes
- Audio Codec Support:
 - I²S protocol
 - Left-justified
 - Right-justified
 - PCM



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REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 5 **MSTEN:** Master Mode Enable bit
 - 1 = Master mode
 - 0 = Slave mode
- bit 4 DISSDI: Disable SDI bit
 - 1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
 - 0 = SDI pin is controlled by the SPI module
- bit 3-2 STXISEL<1:0>: SPI Transmit Buffer Empty Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
 - 10 = Interrupt is generated when the buffer is empty by one-half or more
 - 01 = Interrupt is generated when the buffer is completely empty
 - 00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
- bit 1-0 SRXISEL<1:0>: SPI Receive Buffer Full Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is full
 - 10 = Interrupt is generated when the buffer is full by one-half or more
 - 01 = Interrupt is generated when the buffer is not empty
 - 00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit can only be written when the ON bit = 0.
 - 3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - 4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	-	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—		—
45.0	R-0	R/W-0, HSC	U-0	U-0	R-0	R-0	R-0	R-0
15:8	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HSC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	_	_	OB3E	OB2E	OB1E	OB0E

REGISTER 20-5: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Legend:	HSC = Set by Hardware; Cleared by Software				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-16 Unimplemented: Read as '0'

- bit 15 IBF: Input Buffer Full Status bit
 - 1 = All writable input buffer registers are full
 - 0 = Some or all of the writable input buffer registers are empty
- bit 14 IBOV: Input Buffer Overflow Status bit
 - 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
 0 = No overflow occurred
- bit 13-12 Unimplemented: Read as '0'
- bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits
 - 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
 - 0 = Input Buffer does not contain any unread data
- bit 7 **OBE:** Output Buffer Empty Status bit
 - 1 = All readable output buffer registers are empty
 - 0 = Some or all of the readable output buffer registers are full
- bit 6 **OBUF:** Output Buffer Underflow Status bit
 - 1 = A read occurred from an empty output byte buffer (must be cleared in software)0 = No underflow occurred
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
 - 1 = Output buffer is empty (writing data to the buffer will clear this bit)
 - 0 = Output buffer contains data that has not been transmitted

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	_	—	—	—	_	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
45.0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC ⁽³⁾	AMASK<3:0> ⁽²⁾				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
				ARPT<7:0	_{>} (2)				

REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ALRMEN: Alarm Enable bit^(1,2)
 - 1 = Alarm is enabled
 - 0 = Alarm is disabled

bit 14 CHIME: Chime Enable bit⁽²⁾

- 1 = Chime is enabled ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse. When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 ALRMSYNC: Alarm Sync bit⁽³⁾

- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 AMASK<3:0>: Alarm Mask Configuration bits⁽²⁾

- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved; do not use
- 1011 = Reserved; do not use
- 11xx = Reserved; do not use
- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

TABLE 22-1: ADC REGISTER MAP (CONTINUED)

ess		đ								Bi	ts								s
Virtual Addr (BF80_#)	Register Name	Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
9120	ADC1BUEB	31:16	ADC Result Word B (ADC1BUFB<31:0>)														0000		
0120		15:0														0000			
0120	ADC1BUFC	31:16	ADC Result Word C (ADC1BUEC<31:0>)													0000			
9130		15:0													0000				
0140		31:16	ADC Deput Word D (ADC10LED <21:05)														0000		
9140	ADCIDUFD	15:0	ADG RESUIT WORD D (ADC1BUFD<31:0>)												0000				
0150		31:16								ult Word E		E<31.0>)							0000
9150	ADCIDUIL	15:0							ADC Nes			L~31.0~)							0000
0160		31:16										E-31:05)							0000
9160	ADGIBUFF	15:0							ADC Res			r>31.02)							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for details.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

25.1 CTMU Control Registers

TABLE 25-1: CTMU REGISTER MAP

ess		Bit Range	Bits												6				
Virtual Addr (BF80_#) Register	Register Name ⁽¹⁾		31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
A 200		31:16	EDG1MOD	EDG1POL		EDG15	SEL<3:0>		EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL		EDG28	SEL<3:0>		—	—	0000
A200	CIMUCON	15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG			ITRIM	<5:0>			IRNG	i<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

26.0 POWER-SAVING FEATURES

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 10. "Power-
	Saving Features" (DS60001130), which
	is available from the Documentation >
	Reference Manual section of the
	Microchip PIC32 web site
	(www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX1XX/2XX 28/36/44-pin Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

26.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- Sosc Run mode: the CPU is clocked from the Sosc clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

26.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- Posc Idle mode: the system clock is derived from the Posc. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- Sosc Idle mode: the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.

- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

26.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

26.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See Section 26.3.3 "Peripheral Bus Scaling Method" for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

NOTES:

			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)							
			Operating tempe	erature -4	40°C ≤ TA	≤ +85°C ≤ +105°	C for Industrial C for V-temp			
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions			
	VIL	Input Low Voltage								
DI10		I/O Pins with PMP	Vss	—	0.15 Vdd	V				
		I/O Pins	Vss	—	0.2 Vdd	V				
DI18		SDAx, SCLx	Vss	_	0.3 Vdd	V	SMBus disabled (Note 4)			
DI19		SDAx, SCLx	Vss	_	0.8	V	SMBus enabled (Note 4)			
	VIH	Input High Voltage								
DI20		I/O Pins not 5V-tolerant ⁽⁵⁾	0.65 VDD	_	Vdd	V	(Note 4,6)			
		I/O Pins 5V-tolerant with PMP ⁽⁵⁾	0.25 VDD + 0.8V	_	5.5	V	(Note 4,6)			
		I/O Pins 5V-tolerant ⁽⁵⁾	0.65 VDD	—	5.5	V				
DI28		SDAx, SCLx	0.65 VDD	_	5.5	V	SMBus disabled (Note 4,6)			
DI29		SDAx, SCLx	2.1	_	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 (Note 4,6)			
DI30	ICNPU	Change Notification Pull-up Current	—	—	-50	μA	VDD = 3.3V, VPIN = VSS (Note 3,6)			
DI31	ICNPD	Change Notification Pull-down Current ⁽⁴⁾	—	—	-50	μA	VDD = 3.3V, VPIN = VDD			
	lı∟	Input Leakage Current (Note 3)								
DI50		I/O Ports	_	—	<u>+</u> 1	μA	Vss \leq VPIN \leq VDD, Pin at high-impedance			
DI51		Analog Input Pins	_	_	<u>+</u> 1	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance			
DI55		MCLR(2)	_	—	<u>+</u> 1	μA	$VSS \leq VPIN \leq VDD$			
DI56		OSC1	_	_	<u>+</u> 1	μA	$\label{eq:VSS} \begin{split} &V{\sf SS} \leq V{\sf PIN} \leq V{\sf DD}, \\ &X{\sf T} \text{ and }H{\sf S} \text{ modes} \end{split}$			

TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: See the "Pin Diagrams" section for the 5V-tolerant pins.
- 6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the userselectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 30-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS SCKx (CKP = 0) SP11 SP10 SP21 SP20 SCKx (CKP = 1) SP35 SP20 SP21 SDOx MSb Bit 14 -1 LSb **SP31** SP30 SDIx LSb In MSb In Bit 14 SP40 'SP41' Note: Refer to Figure 30-1 for load conditions.

TABLE 30-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

АС СНА	ARACTERIST	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions	
SP10	TscL	SCKx Output Low Time (Note 3)	Тѕск/2			ns	_	
SP11	TscH	SCKx Output High Time (Note 3)	Тѕск/2	_		ns	_	
SP20	TscF	SCKx Output Fall Time (Note 4)	_	_		ns	See parameter DO32	
SP21	TscR	SCKx Output Rise Time (Note 4)	_	—		ns	See parameter DO31	
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	—	—		ns	See parameter DO32	
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_			ns	See parameter DO31	
SP35	TSCH2DOV,	SDOx Data Output Valid after			15	ns	VDD > 2.7V	
	ISCL2DOV	SCKx Edge	—	—	20	ns	VDD < 2.7V	
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	10	_		ns		
SP41	TscH2dlL, TscL2dlL	Hold Time of SDIx Data Input to SCKx Edge	10			ns	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.







TABLE 30-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

АС СНА	RACTERIS	STICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param. No.	Symbol	Charact	Min.	Max.	Units	Conditions			
IS34	THD:STO	Stop Condition	100 kHz mode	4000	_	ns	_		
		Hold Time	400 kHz mode	600	—	ns			
			1 MHz mode (Note 1)	250		ns			
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—		
			400 kHz mode	0	1000	ns			
			1 MHz mode (Note 1)	0	350	ns			
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus		
			400 kHz mode	1.3	—	μs	must be free before a new		
			1 MHz mode (Note 1)	0.5	—	μS	transmission can start		
IS50 CB Bus Capacitive Loading			_	400	pF	—			

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 31-5: EXTERNAL CLOCK TIMING REQUIREMENTS

АС СНА	RACTERI	STICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
Param. No.	Param. No. Symbol Characteristics		Min.	Typical	Max.	Units	Conditions		
MOS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4		50 50	MHz MHz	EC (Note 2) ECPLL (Note 1)		

Note 1: PLL input requirements: 4 MHz \leq FPLLIN \leq 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 31-6:SPIX MASTER MODE (CKE = 0) TIMING REQUIREMENTS

АС СНА	RACTERIS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions	
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—	—	ns	_	
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2	_	_	ns	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

TABLE 31-7: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

АС СНА	ARACTERIS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions	
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—	_	ns	—	
MSP11	TscH	SCKx Output High Time (Note 1,2)	Tsck/2	—	—	ns	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

APPENDIX A: REVISION HISTORY

Revision A (May 2011)

This is the initial released version of this document.

Revision B (October 2011)

The following two global changes are included in this revision:

- All packaging references to VLAP have been changed to VTLA throughout the document
- All references to VCORE have been removed
- All occurrences of the ASCL1, ASCL2, ASDA1, and ASDA2 pins have been removed
- V-temp temperature range (-40°C to +105°C) was added to all electrical specification tables

This revision includes the addition of the following devices:

- PIC32MX130F064B
- PIC32MX130F064C
- PIC32MX130F064D
- PIC32MX150F128B
- PIC32MX150F128CPIC32MX150F128D
- PIC32MX250F128C
 PIC32MX250F128D

PIC32MX230F064B

PIC32MX230F064C

PIC32MX230F064D

PIC32MX250F128B

Text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-1.

Section	Update Description					
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio	Split the existing Features table into two: PIC32MX1XX General Purpose Family Features (Table 1) and PIC32MX2XX USB Family Features (Table 2).					
and Graphics Interfaces, USB, and Advanced Analog"	Added the SPDIP package reference (see Table 1, Table 2, and " Pin Diagrams ").					
	Added the new devices to the applicable pin diagrams.					
	Changed PGED2 to PGED1 on pin 35 of the 36-pin VTLA diagram for PIC32MX220F032C, PIC32MX220F016C, PIC32MX230F064C, and PIC32MX250F128C devices.					
1.0 "Device Overview"	Added the SPDIP package reference and updated the pin number for AN12 for 44-pin QFN devices in the Pinout I/O Descriptions (see Table 1-1).					
	Added the PGEC4/PGED4 pin pair and updated the C1INA-C1IND and C2INA-C2IND pin numbers for 28-pin SSOP/SPDIP/SOIC devices in the Pinout I/O Descriptions (see Table 1-1).					
2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).					

TABLE A-1: MAJOR SECTION UPDATES