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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx220f032bt-v-so

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-y	R/W-y	R/W-y	R/W-0	R/W-0	R/W-1
	—	—	PLLODIV<2:0>			FRCDIV<2:0>		
23:16	U-0	R-0	R-1	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>		
15:8	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-y	R/W-0
	CLKLOCK	ULOCK ⁽¹⁾	SLOCK	SLPEN	CF	UFRGEN ⁽¹⁾	SOSCEN	OSWEN

Legend: y = Value set from Configuration bits on POR
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2 (default setting)
- 000 = FRC divided by 1

bit 23 **Unimplemented:** Read as '0'

bit 22 **SOSCRDY:** Secondary Oscillator (Sosc) Ready Indicator bit

- 1 = The Secondary Oscillator is running and is stable
- 0 = The Secondary Oscillator is still warming up or is turned off

bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit

- 1 = PBDIV<1:0> bits can be written
- 0 = PBDIV<1:0> bits cannot be written

bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits

- 11 = PBCLK is SYSCLK divided by 8 (default)
- 10 = PBCLK is SYSCLK divided by 4
- 01 = PBCLK is SYSCLK divided by 2
- 00 = PBCLK is SYSCLK divided by 1

Note 1: This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8> ^(1,3)						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0> ^(1,3)							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON	—	SIDL	OE	RSLP ⁽²⁾	—	DIVSWEN	ACTIVE
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0> ⁽¹⁾			

Legend:	HC = Hardware Clearable	HS = Hardware Settable
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits^(1,3)

The value selects the reference clock divider bits. See Figure 8-1 for information.

bit 15 **ON:** Output Enable bit

1 = Reference Oscillator module is enabled

0 = Reference Oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12 **OE:** Reference Clock Output Enable bit

1 = Reference clock is driven out on REFCLKO pin

0 = Reference clock is not driven out on REFCLKO pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit⁽²⁾

1 = Reference Oscillator module output continues to run in Sleep

0 = Reference Oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit

1 = Divider switch is in progress

0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit

1 = Reference clock request is active

0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable port number.

11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin.

Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

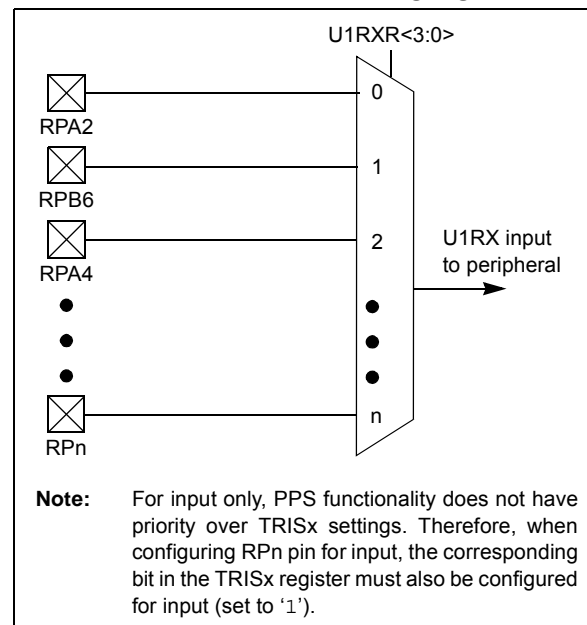
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [pin name]R registers, where [pin name] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



11.4 Ports Control Registers

TABLE 11-3: PORTA REGISTER MAP

Virtual Address (BF88..#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSA1	ANSA0	0003
6010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	TRISA10 ⁽²⁾	TRISA9 ⁽²⁾	TRISA8 ⁽²⁾	TRISA7 ⁽²⁾	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
6020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RA10 ⁽²⁾	RA9 ⁽²⁾	RA8 ⁽²⁾	RA7 ⁽²⁾	—	—	RA4	RA3	RA2	RA1	RA0	xxxx
6030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	LATA10 ⁽²⁾	LATA9 ⁽²⁾	LATA8 ⁽²⁾	LATA7 ⁽²⁾	—	—	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	ODCA10 ⁽²⁾	ODCA9 ⁽²⁾	ODCA8 ⁽²⁾	ODCA7 ⁽²⁾	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
6050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNPUA10 ⁽²⁾	CNPUA9 ⁽²⁾	CNPUA8 ⁽²⁾	CNPUA7 ⁽²⁾	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
6060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNPDA10 ⁽²⁾	CNPDA9 ⁽²⁾	CNPDA8 ⁽²⁾	CNPDA7 ⁽²⁾	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
6070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNIEA10 ⁽²⁾	CNIEA9 ⁽²⁾	CNIEA8 ⁽²⁾	CNIEA7 ⁽²⁾	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
6090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNSTATA10 ⁽²⁾	CNSTATA9 ⁽²⁾	CNSTATA8 ⁽²⁾	CNSTATA7 ⁽²⁾	—	—	CNSTATA4	CNSTATA3	CNSTATA2	CNSTATA1	CNSTATA0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.
- 2: This bit is only available on 44-pin devices.

TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FB8C	RPC8R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC8<3:0>				0000
FB90	RPC9R ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC9<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: This register is only available on 44-pin devices.
 - 2: This register is only available on PIC32MX1XX devices.
 - 3: This register is only available on 36-pin and 44-pin devices.

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REGISTER 11-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A, B, C)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit

1 = CN is enabled

0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit

1 = Idle mode halts CN operation

0 = Idle does not affect CN operation

bit 12-0 **Unimplemented:** Read as '0'

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REGISTER 14-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON ^(1,2)	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	—	SWDTPS<4:0>					WDTWINEN	WDTCLR

Legend:	y = Values set from Configuration bits on POR
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit^(1,2)

- 1 = Enables the WDT if it is not enabled by the device configuration
- 0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit

- 1 = Enable windowed Watchdog Timer
- 0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit

- 1 = Writing a '1' will clear the WDT
- 0 = Software cannot force this bit to a '0'

- Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
- Note 2:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

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NOTES:

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REGISTER 20-5: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HSC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HSC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:

HSC = Set by Hardware; Cleared by Software
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit

- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit

- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
- 0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits

- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit

- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit

- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits

- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

TABLE 26-2: PERIPHERAL MODULE DISABLE REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F240	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CVRMD	—	—	—	CTMUMD	—	—	—	—	—	—	—	AD1MD	0000
F250	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F260	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F270	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F280	PMD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F290	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

28.0 INSTRUCTION SET

The PIC32MX1XX/2XX family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

<p>Note: Refer to “MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set” at www.imgtec.com for more information.</p>
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PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
DI10 DI18 DI19	V _{IL}	Input Low Voltage					
		I/O Pins with PMP	V _{SS}	—	0.15 V _{DD}	V	
		I/O Pins	V _{SS}	—	0.2 V _{DD}	V	
		SDAx, SCLx	V _{SS}	—	0.3 V _{DD}	V	SMBus disabled (Note 4)
		SDAx, SCLx	V _{SS}	—	0.8	V	SMBus enabled (Note 4)
DI20 DI28 DI29	V _{IH}	Input High Voltage					
		I/O Pins not 5V-tolerant ⁽⁵⁾	0.65 V _{DD}	—	V _{DD}	V	(Note 4,6)
		I/O Pins 5V-tolerant with PMP ⁽⁵⁾	0.25 V _{DD} + 0.8V	—	5.5	V	(Note 4,6)
		I/O Pins 5V-tolerant ⁽⁵⁾	0.65 V _{DD}	—	5.5	V	
		SDAx, SCLx	0.65 V _{DD}	—	5.5	V	SMBus disabled (Note 4,6)
		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ V _{PIN} ≤ 5.5 (Note 4,6)
DI30	ICNPU	Change Notification Pull-up Current	—	—	-50	μA	V _{DD} = 3.3V, V _{PIN} = V _{SS} (Note 3,6)
DI31	ICNPD	Change Notification Pull-down Current⁽⁴⁾	—	—	-50	μA	V _{DD} = 3.3V, V _{PIN} = V _{DD}
DI50 DI51 DI55 DI56	I _{IL}	Input Leakage Current (Note 3)					
		I/O Ports	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance
		Analog Input Pins	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance
		MCLR ⁽²⁾	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
		OSC1	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT and HS modes

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** This parameter is characterized, but not tested in manufacturing.
- 5:** See the “Pin Diagrams” section for the 5V-tolerant pins.
- 6:** The V_{IH} specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic “high” internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External “input” logic inputs that require a pull-up source, to guarantee the minimum V_{IH} of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

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TABLE 30-13: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D300	VIOFF	Input Offset Voltage	—	±7.5	±25	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS (Note 2)
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max VICM = (VDD - 1)V (Note 2)
D303A	TRESP	Large Signal Response Time	—	150	400	ns	AVDD = VDD, AVSS = VSS (Note 1,2)
D303B	TSRESP	Small Signal Response Time	—	1	—	μs	This is defined as an input step of 50 mV with 15 mV of overdrive (Note 2)
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	μs	Comparator module is configured before setting the comparator ON bit (Note 2)
D305	IVREF	Internal Voltage Reference	1.14	1.2	1.26	V	—
D312	TSET	Internal Comparator Voltage DRC Reference Setting time	—	—	10	μs	(Note 3)

Note 1: Response time measured with one comparator input at $(VDD - 1.5)/2$, while the other input transitions from VSS to VDD.

2: These parameters are characterized but not tested.

3: Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

4: The Comparator module is functional at $V_{BORMIN} < VDD < VDDMIN$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP51	TssH2boZ	$\overline{\text{SS}}_x \uparrow$ to SDOx Output High-Impedance (Note 4)	5	—	25	ns	—
SP52	Tsch2ssH TscL2ssH	$\overline{\text{SS}}_x \uparrow$ after SCKx Edge	Tsck + 20	—	—	ns	—
SP60	TssL2boV	SDOx Data Output Valid after $\overline{\text{SS}}_x$ Edge	—	—	25	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

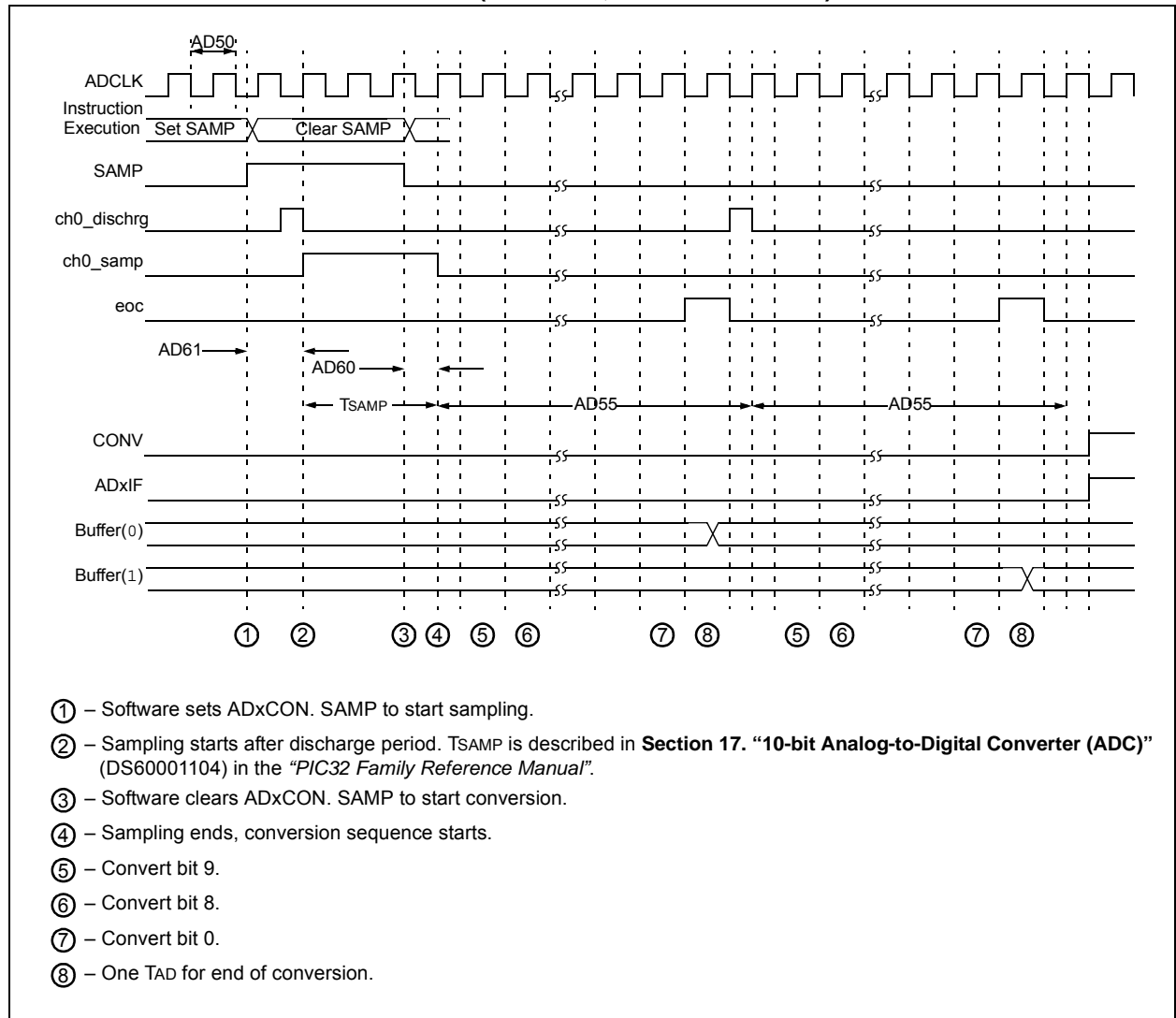
2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns.

4: Assumes 50 pF load on all SPIx pins.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 30-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

33.1 Package Marking Information (Continued)

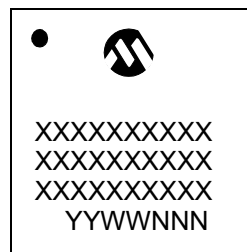
36-Lead VTLA



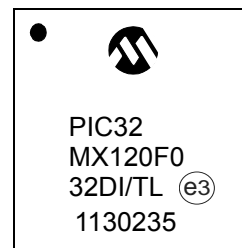
Example



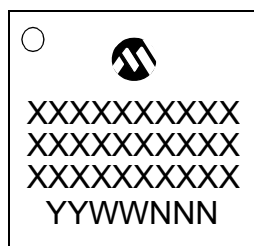
44-Lead VTLA



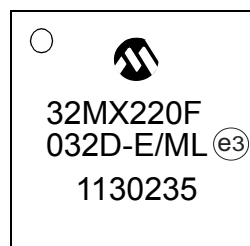
Example



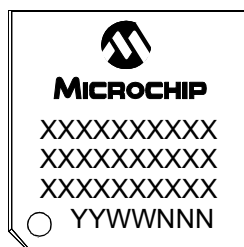
44-Lead QFN



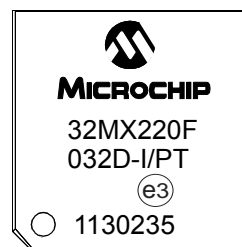
Example



44-Lead TQFP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(^{e3})	Pb-free JEDEC designator for Matte Tin (Sn)
	*(^{e3})	This package is Pb-free. The Pb-free JEDEC designator ((^{e3})) can be found on the outer packaging for this package.
Note: If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.		

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

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