What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx220f032d-50i-pt

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note:	To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 website: http://www.microchip.com/pic32

- **Section 1. "Introduction"** (DS60001127)
- **Section 2. "CPU"** (DS60001113)
- **Section 3. "Memory Organization"** (DS60001115)
- **Section 5. "Flash Program Memory"** (DS60001121)
- **Section 6. "Oscillator Configuration"** (DS60001112)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog Timer and Power-up Timer"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit (I^{2}C)"** (DS60001116)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		—	—	27	O	—	Parallel Master Port address (Demultiplexed Master modes)
PMA3		—	—	38	O	—	
PMA4		—	—	37	O	—	
PMA5		—	—	4	O	—	
PMA6		—	—	5	O	—	
PMA7		—	—	13	O	—	
PMA8		—	—	32	O	—	
PMA9		—	—	35	O	—	
PMA10		—	—	12	O	—	
PMCS1	23	26	29	15	O	—	Parallel Master Port Chip Select 1 strobe
PMD0	20[2] 1[3]	23[2] 4[3]	26[2] 35[3]	10[2] 21[3]	I/O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes)
PMD1	19[2] 2[3]	22[2] 5[3]	25[2] 36[3]	9[2] 22[3]	I/O	TTL/ST	
PMD2	18[2] 3[3]	21[2] 6[3]	24[2] 1[3]	8[2] 23[3]	I/O	TTL/ST	
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12[2] 28[3]	15[2] 3[3]	16[2] 34[3]	42[2] 20[3]	I/O	TTL/ST	
PMD7	11[2] 27[3]	14[2] 2[3]	15[2] 33[3]	41[2] 19[3]	I/O	TTL/ST	
PMRD	21	24	27	11	O	—	Parallel Master Port read strobe
PMWR	22[2] 4[3]	25[2] 7[3]	28[2] 2[3]	14[2] 24[3]	O	—	Parallel Master Port write strobe
VBUS	12[3]	15[3]	16[3]	42[3]	I	Analog	USB bus power monitor
VUSB3V3	20[3]	23[3]	26[3]	10[3]	P	—	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22[3]	25[3]	28[3]	14[3]	O	—	USB Host and OTG bus power control output
D+	18[3]	21[3]	24[3]	8[3]	I/O	Analog	USB D+
D-	19[3]	22[3]	25[3]	9[3]	I/O	Analog	USB D-

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   P = Power
ST = Schmitt Trigger input with CMOS levels   O = Output   I = Input
TTL = TTL input buffer   PPS = Peripheral Pin Select   — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX120/220 DEVICES (8 KB RAM, 32 KB FLASH)

Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).
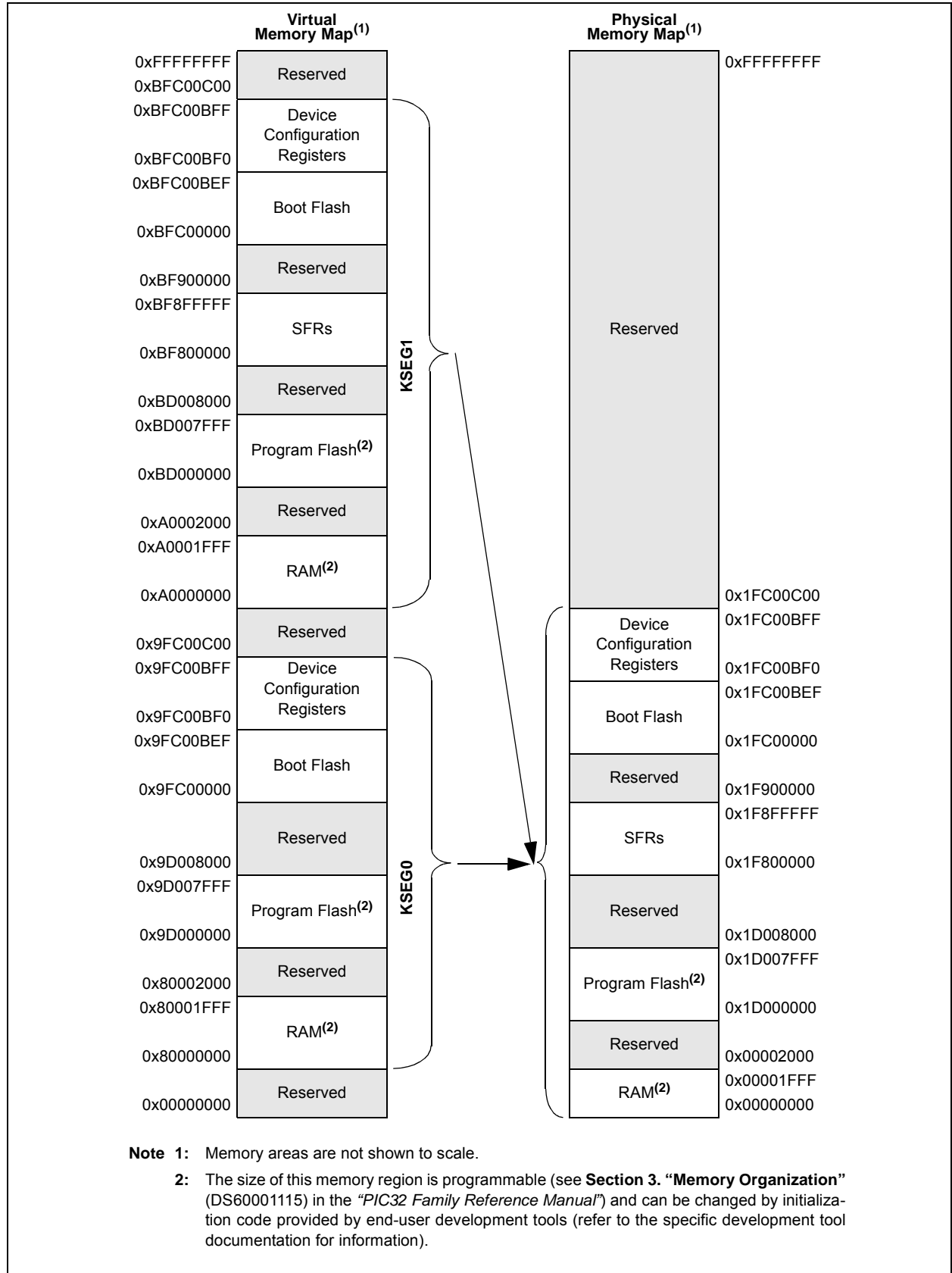
PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	**Offset Start**
Watchdog Timer		0x0000
RTCC		0x0200
Timer1-5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
IC1 and IC2		0x5000
SPI1 and SPI2		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC	0xBF80	0x9000
CV$_{REF}$		0x9800
Comparator		0xA000
CTMU		0xA200
Oscillator		0xF000
Device and Revision ID		0xF220
Peripheral Module Disable		0xF240
Flash Controller		0xF400
Reset		0xF600
PPS		0xFA04
Interrupts		0x1000
Bus Matrix		0x2000
DMA	0xBF88	0x3000
USB		0x5050
PORTA-PORTC		0x6000
Configuration	0xBFC0	0x0BF0

5.1 Flash Controller Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F400	NVMCON[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	—	—	—	—	—	—	—		NVMOP<3:0>			0000
F410	NVMKEY	31:16								NVMKEY<31:0>									0000
		15:0																	0000
F420	NVMADDR[1]	31:16								NVMADDR<31:0>									0000
		15:0																	0000
F430	NVMDATA	31:16								NVMDATA<31:0>									0000
		15:0																	0000
F440	NVMSRCADDR	31:16								NVMSRCADDR<31:0>									0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

6.0   RESETS

| Note:	This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- Power-on Reset (POR)
- Master Clear Reset pin (MCLR)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1:   SYSTEM RESET BLOCK DIAGRAM
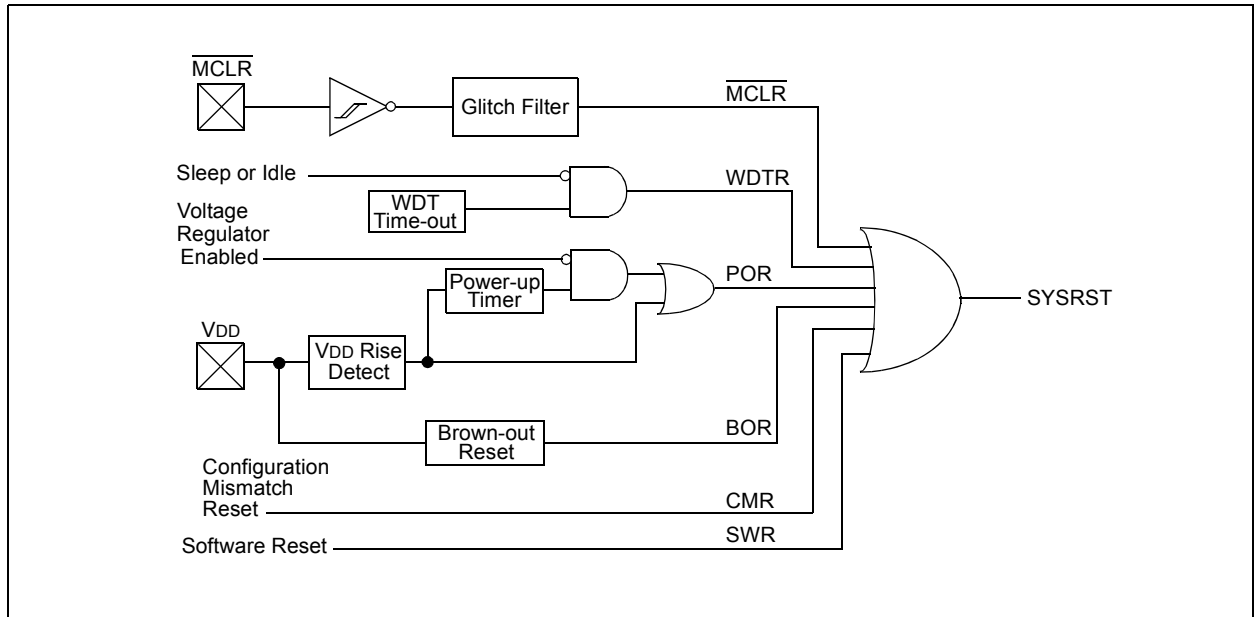
REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST[1]

Legend:			
	HC = Cleared by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit[1]

   1 = Enable Software Reset event
   0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit is written. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 10-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8   **Unimplemented:** Read as '0'

bit 7   **LSPD:** Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)
1 = Direct connection to a Low-Speed device enabled
0 = Direct connection to a Low-Speed device disabled; hub required with PRE_PID

bit 6   **RETRYDIS:** Retry Disable bit (Host mode and U1EP0 only)
1 = Retry NAKed transactions disabled
0 = Retry NAKed transactions enabled; retry done in hardware

bit 5   **Unimplemented:** Read as '0'

bit 4   **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN = 1 and EPRXEN = 1:
1 = Disable Endpoint n from Control transfers; only TX and RX transfers allowed
0 = Enable Endpoint n for Control (SETUP) transfers; TX and RX transfers also allowed
Otherwise, this bit is ignored.

bit 3   **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint n receive is enabled
0 = Endpoint n receive is disabled

bit 2   **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint n transmit is enabled
0 = Endpoint n transmit is disabled

bit 1   **EPSTALL:** Endpoint Stall Status bit
1 = Endpoint n was stalled
0 = Endpoint n was not stalled

bit 0   **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint Handshake is enabled
0 = Endpoint Handshake is disabled (typically used for isochronous endpoints)

REGISTER 11-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A, B, C)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit

1 = CN is enabled
0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit

1 = Idle mode halts CN operation
0 = Idle does not affect CN operation

bit 12-0 **Unimplemented:** Read as '0'

REGISTER 18-2: I2CxSTAT: I²C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF

Legend:		
	HS = Set in hardware	HSC = Hardware set/cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

REGISTER 19-2:   UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6   **URXISEL<1:0>:** Receive Interrupt Mode Selection bit

11 = Reserved; do not use

10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters)

01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters)

00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5   **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)

1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.

0 = Address Detect mode is disabled

bit 4   **RIDLE:** Receiver Idle bit (read-only)

1 = Receiver is Idle

0 = Data is being received

bit 3   **PERR:** Parity Error Status bit (read-only)

1 = Parity error has been detected for the current character

0 = Parity error has not been detected

bit 2   **FERR:** Framing Error Status bit (read-only)

1 = Framing error has been detected for the current character

0 = Framing error has not been detected

bit 1   **OERR:** Receive Buffer Overrun Error Status bit.

This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state.

1 = Receive buffer has overflowed

0 = Receive buffer has not overflowed

bit 0   **URXDA:** Receive Buffer Data Available bit (read-only)

1 = Receive buffer has data, at least one more character can be read

0 = Receive buffer is empty

20.1 PMP Control Registers

TABLE 20-1: PARALLEL MASTER PORT REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
7000	PMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	—	CS1P	—	WRSP	RDSP	0000
7010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		—	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
7020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	CS1 / ADDR14	—	—	—	ADDR<10:0>											0000
7030	PMDOUT	31:16	DATAOUT<31:0>																0000
		15:0																	0000
7040	PMDIN	31:16	DATAIN<31:0>																0000
		15:0																	0000
7050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	PTEN14	—	—	—	PTEN<10:0>											0000
7060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

23.0 COMPARATOR

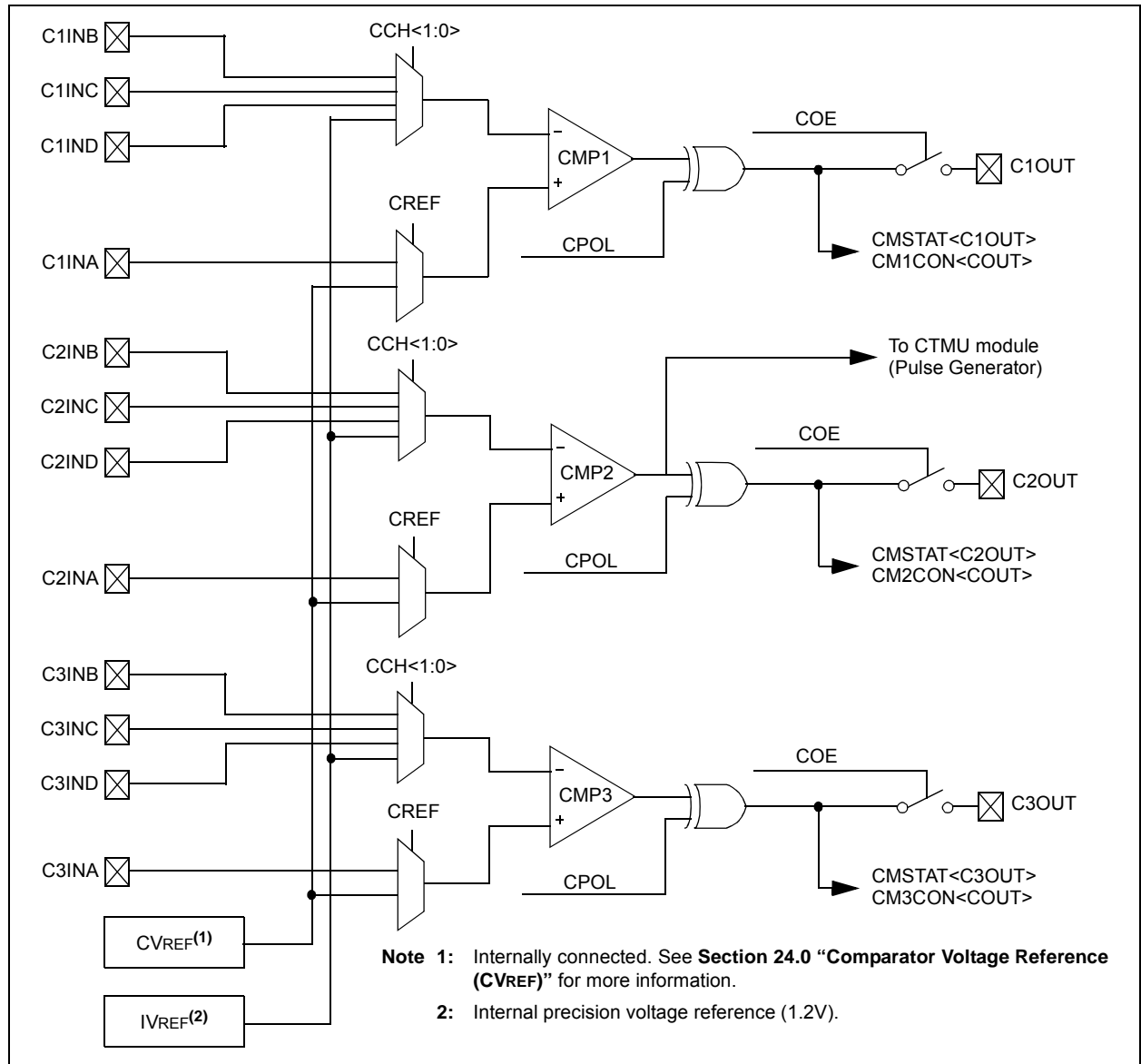| Note:	This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Analog Comparator module contains three comparators that can be configured in a variety of ways.

Following are some of the key features of this module:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be Inverted
- Selectable interrupt generation

A block diagram of the comparator module is provided in Figure 23-1.

FIGURE 23-1: COMPARATOR BLOCK DIAGRAM

Note 1: Internally connected. See **Section 24.0 "Comparator Voltage Reference (CVREF)"** for more information.

2: Internal precision voltage reference (1.2V).

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp	
Param. No.	Typical[2]	Max.	Units	Conditions	
Power-Down Current (I_{PD}) (Notes 1, 5)					
DC40k	44	70	μA	-40°C	Base Power-Down Current
DC40l	44	70	μA	+25°C	
DC40n	168	259	μA	+85°C	
DC40m	335	536	μA	+105ºC	
Module Differential Current					
DC41e	5	20	μA	3.6V	Watchdog Timer Current: ΔI$_{WDT}$ **(Note 3)**
DC42e	23	50	μA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI$_{RTCC}$ **(Note 3)**
DC43d	1000	1100	μA	3.6V	ADC: ΔI$_{ADC}$ **(Notes 3,4)**

Note 1: The test conditions for I_{PD} current measurements are as follows:
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V$_{SS}$
- $\overline{MCLR}$ = V$_{DD}$
- RTCC and JTAG are disabled

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

5: I_{PD} electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.
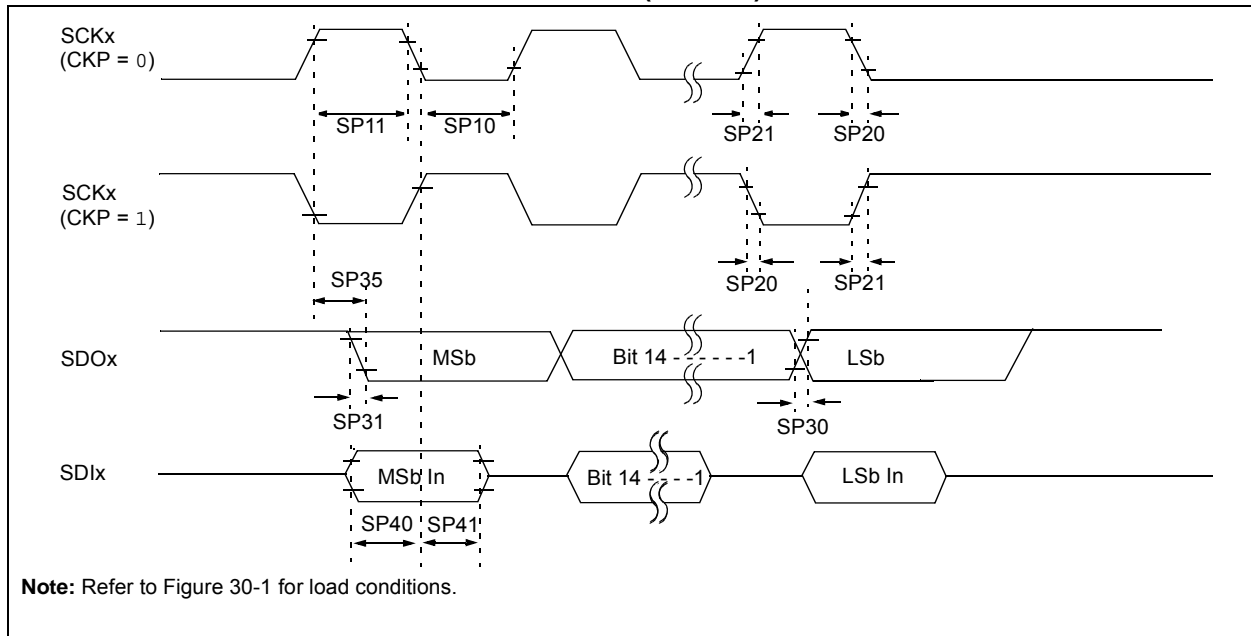
TABLE 30-9: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typ.[(1)]	Max.	Units	Conditions
DI60a	IICL	**Input Low Injection Current**	0	—	-5[(2,5)]	mA	This parameter applies to all pins, with the exception of the power pins.
DI60b	IICH	**Input High Injection Current**	0	—	+5[(3,4,5)]	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, and the SOSCI, SOSCO, OSC1, D+, and D- pins.
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and Control pins)**	-20[(6)]	—	+20[(6)]	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT)

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 3**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

FIGURE 30-10: **SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS**

Note: Refer to Figure 30-1 for load conditions.

TABLE 30-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics[1]	Min.	Typical[2]	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time **(Note 3)**	Tsck/2	—	—	ns	—
SP11	TscH	SCKx Output High Time **(Note 3)**	Tsck/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2DOV, TscL2DOV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2DIL, TscL2DIL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 31-8: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
MSP70	T_{ScL}	SCKx Input Low Time **(Note 1,2)**	$T_{SCK}/2$	—	—	ns	—
MSP71	T_{ScH}	SCKx Input High Time **(Note 1,2)**	$T_{SCK}/2$	—	—	ns	—
MSP51	$T_{SSH2DOZ}$	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 2)**	5	—	25	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

    2: The minimum clock period for SCKx is 40 ns.

TABLE 31-9: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

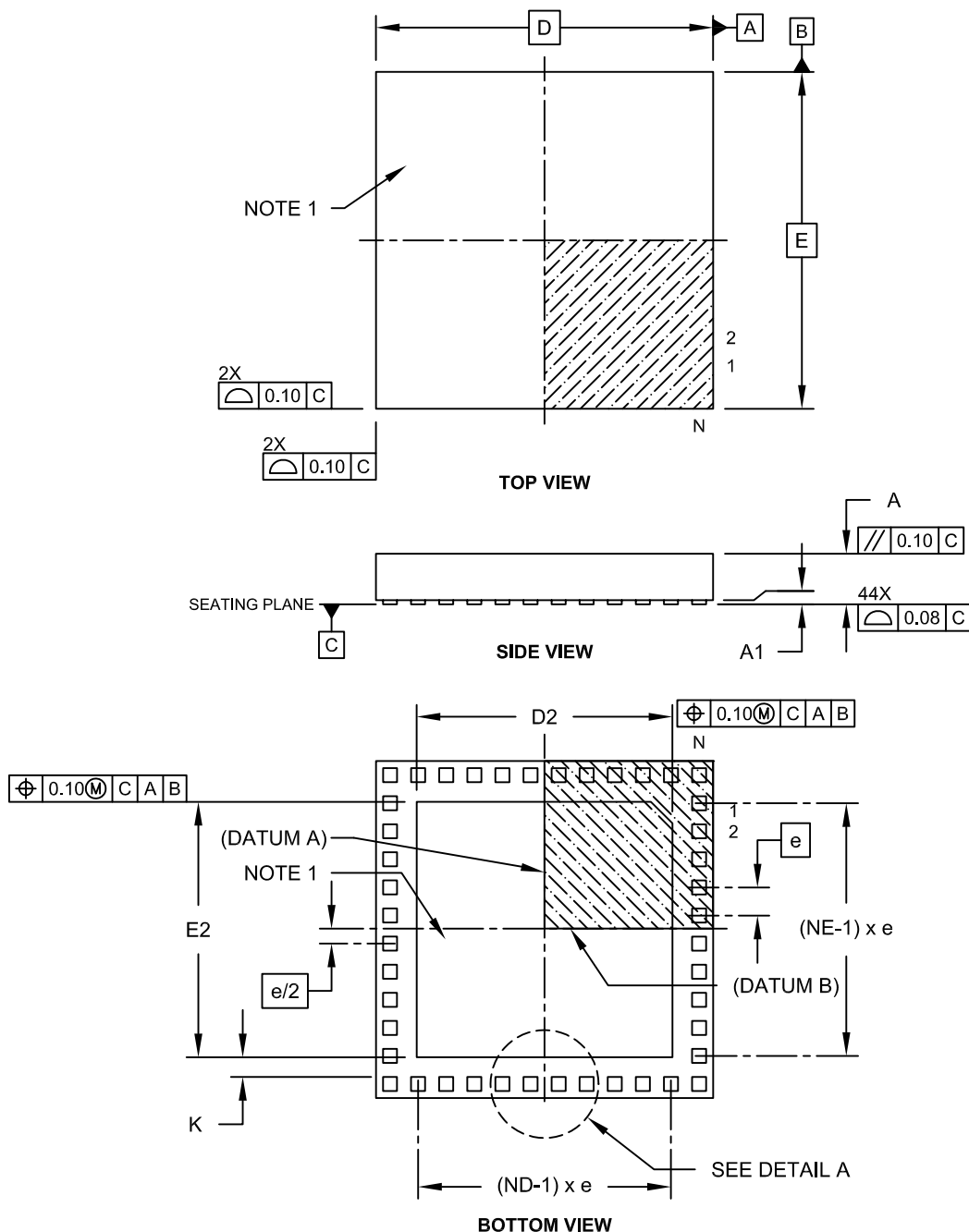| AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
SP70	T_{ScL}	SCKx Input Low Time **(Note 1,2)**	$T_{SCK}/2$	—	—	ns	—
SP71	T_{ScH}	SCKx Input High Time **(Note 1,2)**	$T_{SCK}/2$	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

    2: The minimum clock period for SCKx is 40 ns.

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

NOTE 1

2X ⌓ 0.10 C

2X ⌓ 0.10 C

SIDE VIEW

SEATING PLANE

C

// 0.10 C

44X ⌓ 0.08 C

A1

BOTTOM VIEW

⊕ 0.10 Ⓜ C A B

⊕ 0.10 Ⓜ C A B

(DATUM A)

NOTE 1

E2

e/2

K

(DATUM B)

e

(NE-1) x e

(ND-1) x e

SEE DETAIL A
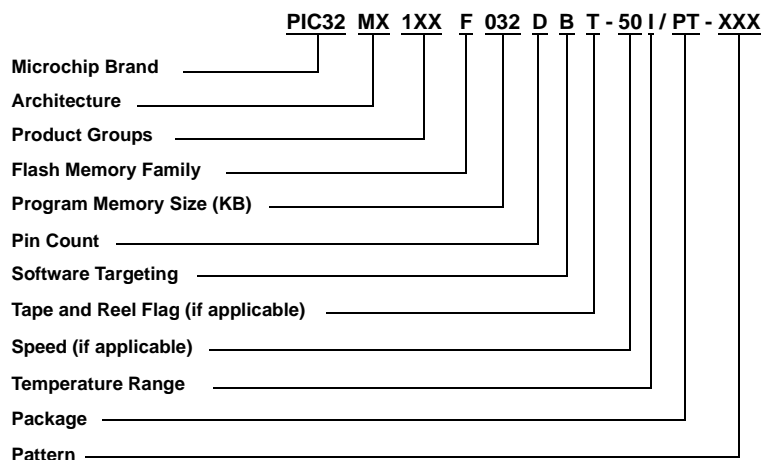
Microchip Technology Drawing C04-157C Sheet 1 of 2

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PIC32   MX   1XX   F   032   D   B   T - 50 I / PT - XXX

Microchip Brand
Architecture
Product Groups
Flash Memory Family
Program Memory Size (KB)
Pin Count
Software Targeting
Tape and Reel Flag (if applicable)
Speed (if applicable)
Temperature Range
Package
Pattern

Example:

PIC32MX110F032DT-I/PT:
General purpose PIC32,
32-bit RISC MCU with M4K® core,
32 KB program memory, 44-pin,
Industrial temperature,
TQFP package.

Flash Memory Family

Architecture	MX	= M4K® MCU core
Product Groups	1XX	= General purpose microcontroller family
	2XX	= General purpose microcontroller family
Flash Memory Family	F	= Flash program memory
Program Memory Size	016	= 16K
	032	= 32K
	064	= 64K
	128	= 128K
	256	= 256K
Pin Count	B	= 28-pin
	C	= 36-pin
	D	= 44-pin
Software Targeting	B	= Targeted for Bluetooth® Audio Break-in devices
Speed	( )	= 40 MHz – ( ) indicates a blank field; package markings for 40 MHz devices do not include the Speed
	50	= 50 MHz
Temperature Range	I	= –40°C to +85°C (Industrial)
	V	= –40°C to +105°C (V-temp)
Package	ML	= 28-Lead (6x6 mm) QFN (Plastic Quad Flatpack)
	ML	= 44-Lead (8x8 mm) QFN (Plastic Quad Flatpack)
	PT	= 44-Lead (10x10x1 mm) TQFP (Plastic Thin Quad Flatpack)
	SO	= 28-Lead (7.50 mm) SOIC (Plastic Small Outline)
	SP	= 28-Lead (300 mil) SPDIP (Skinny Plastic Dual In-line)
	SS	= 28-Lead (5.30 mm) SSOP (Plastic Shrink Small Outline)
	TL	= 36-Lead (5x5 mm) VTLA (Very Thin Leadless Array)
	TL	= 44-Lead (6x6 mm) VTLA (Very Thin Leadless Array)
Pattern		Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)
	ES	= Engineering Sample