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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f064bt-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 13: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

44-PIN VTLA (TOP VIEW)^(1,2,3,5)

PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	VDD
7	VCAP	29	Vss
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVdd	39	Vss
18	MCLR	40	VDD
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

44

1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

5: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:



FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX150/250 DEVICES (32 KB RAM, 128 KB FLASH)

2: The size of this memory region is programmable (see Section 3. "Memory Organization" (DS60001115) in the "*PIC32 Family Reference Manual*") and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
31:24 - 23:16 -	ROTRIM<8:1>											
23:16	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0				
	ROTRIM<0>	—	—	—	—	—	—	—				
45.0	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0				
15:8	—	_	_	_	_	_	—	—				
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
7:0	_	_	_	_	_	_	_	_				

REGISTER 8-4: REFOTRIM: REFERENCE OSCILLATOR TRIM REGISTER

Legend:

Logonal			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 ROTRIM<8:0>: Reference Oscillator Trim bits

Note: While the ON (REFOCON<15>) bit is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

ess										Bi	ts								
Virtual Addre (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3170	DCH1SSIZ	31:16	_	—		_	_	_	—	—		_	—	_	_	_	_	—	0000
0170	DOITIOOIZ	15:0		i		i			i	CHSSIZ	2<15:0>		t					i	0000
3180	DCH1DSIZ	31:16		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0.00	50115012	15:0								CHDSIZ	Z<15:0>								0000
3190	DCH1SPTR	31:16				_		_		—	—	—	—	—	_	—	—		0000
		15:0 CHSPTR<15:0>									0000								
31A0	DCH1DPTR	11DPTR 15:0									0000								
		10.0									~~15.0>								0000
31B0	DCH1CSIZ	15.0				_	_			CHCSIZ	 7<15:0>		_						0000
		31:16	_		_	_	_	_		_		_	_	_	_	_	_		0000
31C0	DCH1CPTR	15:0								CHCPTI	R<15:0>								0000
	DOLUDAT	31:16	_		_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
31D0	DCH1DAT	15:0	_	_	_	_	_	_	_	_				CHPDA	T<7:0>				0000
2150		31:16	_	_	_	—	_	_	—	_	_	_	_	_	_	_	_	—	0000
SIEU	DCH2CON	15:0	CHBUSY	—	—	—	—	-	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	-	CHEDET	CHPR	l<1:0>	0000
31E0	DCH2ECON	31:16	—	_	—	—	—	—	_	—			1	CHAIR	Q<7:0>				OOFF
011 0	DONZEOON	15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—		FF00
3200	DCH2INT	31:16				_	_		—		CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	_		—	—	—	—		—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3210	DCH2SSA	31:16								CHSSA	<31:0>								0000
		15:0																	0000
3220	DCH2DSA	15.0								CHDSA	<31:0>								0000
		31.16	_			_	_	_		_		_		_	_	_	_		0000
3230	DCH2SSIZ	15.0								CHSSIZ	/<15 [.] 0>								0000
		31:16	_	_		_	_	_		_	_	_	_	_	_	_	_	_	0000
3240	DCH2DSIZ	SIZ								0000									
0050	DOLIGODITO	31:16	_	_	_	—	_	_		_	_	_	_	_	_	_	_		0000
3250	DCH2SPTR	15:0								CHSPTI	R<15:0>								0000
3260		31:16	—	—	—	—	—	-	—	_	_		_	_	-	-		_	0000
5200		15:0								CHDPT	R<15:0>								0000
3270	DCH2CSI7	31:16		—	—	—	_	—		—	—	—	—	—	—	—	—		0000
00	_ 5.12001L	15:0	CHCSIZ<15:0> 0000																

Legend:

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

TABLE 11-5: PORTC REGISTER MAP

ess	_	Bits										(0							
Virtual Addr (BF88_#)	Register Name ^{(1,2})	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6200		31:16	_	—	—	—	—	—	—	—	—	—	—	—	—	—	_	—	0000
0200	ANOLLO	15:0	_	—	_	—	—	—		—	—	—	—	—	ANSC3 ⁽⁴⁾	ANSC2 ⁽³⁾	ANSC1	ANSC0	000F
6210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	_	—	0000
0210	11100	15:0	_	—		—	—	—	TRISC9	TRISC8 ⁽³⁾	TRISC7 ⁽³⁾	TRISC6 ⁽³⁾	TRISC5 ⁽³⁾	TRISC4 ⁽³⁾	TRISC3	TRISC2 ⁽³⁾	TRISC1	TRISC0	03FF
6220	PORTO	31:16	_	—		—	—	—		—	—	—	—						0000
0220	1 OKTO	15:0	_	—		—	—	—	RC9	RC8 ⁽³⁾	RC7 ⁽³⁾	RC6 ⁽³⁾	RC5 ⁽³⁾	RC4 ⁽³⁾	RC3	RC2 ⁽³⁾	RC1	RC0	xxxx
6230	LATC	31:16	_	—		—	—	—		—	—	—	—	—	—	—		—	0000
0200	L/ (I O	15:0	_	—		—	—	—	LATC9	LATC8 ⁽³⁾	LATC7 ⁽³⁾	LATC6 ⁽³⁾	LATC5 ⁽³⁾	LATC4 ⁽³⁾	LATC3	LATC2 ⁽³⁾	LATC1	LATC0	xxxx
6240	ODCC	31:16	_	—		—	—	—		—	—	—	—	—	—	—		—	0000
0240	ODCC	15:0	_	—		—	—	—	ODCC9	ODCC8 ⁽³⁾	ODCC7 ⁽³⁾	ODCC6 ⁽³⁾	ODCC5 ⁽³⁾	ODCC4 ⁽³⁾	ODCC3	ODCC2 ⁽³⁾	ODCC1	ODCC0	0000
6250	CNDUC	31:16	_	—		—	—	—		—	—	—	—	—	—	—		—	0000
0230	CINFUC	15:0	_	—		—	—	—	CNPUC9	CNPUC8 ⁽³⁾	CNPUC7 ⁽³⁾	CNPUC6 ⁽³⁾	CNPUC5 ⁽³⁾	CNPUC4 ⁽³⁾	CNPUC3	CNPUC2 ⁽³⁾	CNPUC1	CNPUC0	0000
6260		31:16	_	—	—	—	—	—		_	—	_	—	_	_		_	—	0000
0200	CINFDC	15:0	_	—	—	—	—	—	CNPDC9	CNPDC8 ⁽³⁾	CNPDC7 ⁽³⁾	CNPDC6 ⁽³⁾	CNPDC5 ⁽³⁾	CNPDC4 ⁽³⁾	CNPDC3	CNPDC2 ⁽³⁾	CNPDC1	CNPDC0	0000
6270	CNCONC	31:16	_	—	—	—	—	—		_	—	_	—	_	_		_	—	0000
0270	CINCOINC	15:0	ON	—	SIDL	—	—	—		_	—	_	—	_	_		_	—	0000
6000		31:16		_		_	—	—	—	—	—	—	—	—	_	—		_	0000
0200	CINEINC	15:0	-	_	—	—	—	—	CNIEC9	CNIEC8 ⁽³⁾	CNIEC7 ⁽³⁾	CNIEC6 ⁽³⁾	CNIEC5 ⁽³⁾	CNIEC4 ⁽³⁾	CNIEC3	CNIEC2 ⁽³⁾	CNIEC1	CNIEC0	0000
6200	CNOTATO	31:16		_	_	_	_	—	_	—	—	—	_	—	_	_	_		0000
6290	CINSTATC	15:0		_	_	_	_	—	CNSTATC9	CNSTATC8(3)	CNSTATC7(3)	CNSTATC6(3)	CNSTATC5(3)	CNSTATC4(3)	CNSTATC3	CNSTATC2(3)	CNSTATC1	CNSTATCO	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: PORTC is not available on 28-pin devices.

3: This bit is only available on 44-pin devices.

4: This bit is only available on USB-enabled devices with 36 or 44 pins.

13.2 Timer Control Registers

TABLE 13-1: TIMER2-TIMER5 REGISTER MAP

ess										Bi	its								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	TOCON	31:16	_	_			—	—	_	—	—	_	—		_		—	—	0000
0800	12000	15:0	ON	—	SIDL		—				TGATE	-	TCKPS<2:0	>	T32	_	TCS	_	0000
0010		31:16	—	_	_	_	_	_	-		_	_	_	_	_	_	_	_	0000
0810	TMR2 15:0									0000									
0000	002	31:16	_	_	_	_	-	_	_	_	—	_	-	_	_	_	_	_	0000
0820	PR2	15:0								PR2<	15:0>								FFFF
0.4.00	TACON	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_		0000
0A00	13CON	15:0	ON	_	SIDL	_	_	_	_	_	TGATE	-	TCKPS<2:0	>	_	_	TCS	_	0000
0.440		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
UATU	TMR3	15:0								TMR3	<15:0>								0000
0.4.00	000	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_		0000
0A20	PR3	15:0								PR3<	15:0>								FFFF
0000	TACON	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_		0000
0000	14CON	15:0	ON	_	SIDL	_	_	_	_	_	TGATE	-	TCKPS<2:0	>	T32	_	TCS	_	0000
0040		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0010	TMR4	15:0					•			TMR4	<15:0>								0000
0000	004	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_		0000
0020	PR4	15:0					•			PR4<	15:0>								FFFF
0500	TEOON	31:16	—	—	_		_	—	_	_	—	_	_	_	_	_		_	0000
0E00	15CON	15:0	ON	_	SIDL	_	_	_	_	_	TGATE	-	TCKPS<2:0	>	_	_	TCS	—	0000
0540	TMDC	31:16	—	_	_	_	_	_	_	_	_	_	—	—	_	_	—	—	0000
0E10	IMR5	15:0								TMR5	<15:0>								0000
0500	005	31:16	—	—	_		_	_	—	—	_	—	_	—	_	_	—	—	0000
0E20	PK5	15:0								PR5<	15:0>								FFFF

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

REGISTER 18-2: I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware set or clear when Start, Repeated Start or Stop detected.
bit 3	S: Start bit
	 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last
	Hardware set or clear when Start, Repeated Start or Stop detected.
bit 2	R_W: Read/Write Information bit (when operating as I ² C slave)
	1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave
	Hardware set or clear after reception of I ² C device address byte.
bit 1	RBF: Receive Buffer Full Status bit
	1 = Receive complete, I2CxRCV is full
	0 = Receive not complete, I2CxRCV is empty
	Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit
	1 = Transmit in progress, I2CxTRN is full

0 = Transmit complete, I2CxTRN is empty

Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31.24	—	_	—	—	—	_	—	—			
23.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	Bit 25/17/9/1 U-0 U-0 R/W-0 (<3:0>(2) R/W-0	—			
45.0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC ⁽³⁾		AMASK	<3:0> (2)				
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0	ARPT<7:0> ⁽²⁾										

REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ALRMEN: Alarm Enable bit^(1,2)
 - 1 = Alarm is enabled
 - 0 = Alarm is disabled

bit 14 CHIME: Chime Enable bit⁽²⁾

- 1 = Chime is enabled ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse. When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 ALRMSYNC: Alarm Sync bit⁽³⁾

- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 AMASK<3:0>: Alarm Mask Configuration bits⁽²⁾

- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved; do not use
- 1011 = Reserved; do not use
- 11xx = Reserved; do not use
- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
31:24	—	—	HR10)<1:0>	HR01<3:0>					
00.40	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
23:16	—		MIN10<2:0>			MIN01	<3:0>			
45.0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15:8	—		SEC10<2:0>		SEC01<3:0>					
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
7:0	—	—	—	—	_	_	_	—		
	•	•								
l egend.										

REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

bit 29-28 HR10<1:0>: Binary Coded Decimal value of hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9 bit 23 **Unimplemented:** Read as '0'

bit 22-20 MIN10<2:0>: Binary Coded Decimal value of minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9 bit 15 **Unimplemented:** Read as '0'

bit 14-12 SEC10<2:0>: Binary Coded Decimal value of seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 Unimplemented: Read as '0'

22.0 **10-BIT ANALOG-TO-DIGITAL** CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- · Up to 1 Msps conversion speed

FIGURE 22-1:

- Up to 13 analog input pins
- External voltage reference input pins
- · One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- · 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- · Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. Figure 22-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.



5: This selection is only used with CTMU capacitive and time measurement.

ADC1 MODULE BLOCK DIAGRAM

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 22-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	_	—	—	—
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ADRC	—	—			SAMC<4:0>(1)		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
7:0				ADCS<	7:0> ⁽²⁾			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ADRC: ADC Conversion Clock Source bit
 - 1 = Clock derived from FRC
 - 0 = Clock derived from Peripheral Bus Clock (PBCLK)
- bit 14-13 Unimplemented: Read as '0'
- - 00000001 =TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD 00000000 =TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD
- **Note 1:** This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
 - 2: This bit is not used if the ADRC (AD1CON3<15>) bit = 1.

REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED) bit 24 EDG1STAT: Edge1 Status bit Indicates the status of Edge1 and can be written to control edge source 1 = Edge1 has occurred 0 = Edge1 has not occurred EDG2MOD: Edge2 Edge Sampling Select bit bit 23 1 = Input is edge-sensitive 0 = Input is level-sensitive bit 22 EDG2POL: Edge 2 Polarity Select bit 1 = Edge2 programmed for a positive edge response 0 = Edge2 programmed for a negative edge response bit 21-18 EDG2SEL<3:0>: Edge 2 Source Select bits 1111 = C3OUT pin is selected 1110 = C2OUT pin is selected 1101 = C1OUT pin is selected 1100 = PBCLK clock is selected 1011 = IC3 Capture Event is selected 1010 = IC2 Capture Event is selected 1001 = IC1 Capture Event is selected 1000 = CTED13 pin is selected 0111 = CTED12 pin is selected 0110 = CTED11 pin is selected 0101 = CTED10 pin is selected 0100 = CTED9 pin is selected 0011 = CTED1 pin is selected 0010 = CTED2 pin is selected 0001 = OC1 Compare Event is selected 0000 = Timer1 Event is selected bit 17-16 Unimplemented: Read as '0' bit 15 **ON:** ON Enable bit 1 = Module is enabled 0 = Module is disabled bit 14 Unimplemented: Read as '0' bit 13 CTMUSIDL: Stop in Idle Mode bit 1 = Discontinue module operation when the device enters Idle mode 0 = Continue module operation when the device enters Idle mode TGEN: Time Generation Enable bit⁽¹⁾ bit 12 1 = Enables edge delay generation 0 = Disables edge delay generation bit 11 EDGEN: Edge Enable bit 1 = Edges are not blocked 0 = Edges are blocked

- **Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 30-41) in Section 30.0 "Electrical Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

26.0 POWER-SAVING FEATURES

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 10. "Power-
	Saving Features" (DS60001130), which
	is available from the Documentation >
	Reference Manual section of the
	Microchip PIC32 web site
	(www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX1XX/2XX 28/36/44-pin Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

26.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- Sosc Run mode: the CPU is clocked from the Sosc clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

26.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- Posc Idle mode: the system clock is derived from the Posc. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- Sosc Idle mode: the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.

- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

26.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

26.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See Section 26.3.3 "Peripheral Bus Scaling Method" for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)					
		$\begin{array}{ll} Operating \ temperature & -40^{\circ}C \leq TA \leq +85^{\circ}C \ for \ Industrial \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \ for \ V\text{-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
	VIL	Input Low Voltage					
DI10		I/O Pins with PMP	Vss	—	0.15 Vdd	V	
		I/O Pins	Vss	—	0.2 Vdd	V	
DI18		SDAx, SCLx	Vss	_	0.3 Vdd	V	SMBus disabled (Note 4)
DI19		SDAx, SCLx	Vss	_	0.8	V	SMBus enabled (Note 4)
	VIH	Input High Voltage					
DI20		I/O Pins not 5V-tolerant ⁽⁵⁾	0.65 VDD	_	Vdd	V	(Note 4,6)
		I/O Pins 5V-tolerant with PMP ⁽⁵⁾	0.25 VDD + 0.8V	_	5.5	V	(Note 4,6)
		I/O Pins 5V-tolerant ⁽⁵⁾	0.65 VDD	—	5.5	V	
DI28		SDAx, SCLx	0.65 VDD	_	5.5	V	SMBus disabled (Note 4,6)
DI29		SDAx, SCLx	2.1	_	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 (Note 4,6)
DI30	ICNPU	Change Notification Pull-up Current	—	—	-50	μA	VDD = 3.3V, VPIN = VSS (Note 3,6)
DI31	ICNPD	Change Notification Pull-down Current ⁽⁴⁾	—	—	-50	μA	VDD = 3.3V, VPIN = VDD
	lı∟	Input Leakage Current (Note 3)					
DI50		I/O Ports	_	—	<u>+</u> 1	μA	Vss \leq VPIN \leq VDD, Pin at high-impedance
DI51		Analog Input Pins	_	_	<u>+</u> 1	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance
DI55		MCLR(2)	_	—	<u>+</u> 1	μA	$VSS \leq VPIN \leq VDD$
DI56		OSC1	_	_	<u>+</u> 1	μA	VSS \leq VPIN \leq VDD, XT and HS modes

TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: See the "Pin Diagrams" section for the 5V-tolerant pins.
- 6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the userselectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

31.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX 28/36/44-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 30.0** "Electrical Characteristics", with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "M", which denotes 50 MHz operation. For example, parameter DC29a in **Section 30.0** "**Electrical Characteristics**", is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/36/44-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	40°C to +85°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss (Note 3)	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 2.3V$ (Note 3)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 2.3V (Note 3)	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of Vss pin(s)	
Maximum current into VDD pin(s) (Note 2)	
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	
Maximum current sourced by all ports (Note 2)	200 mA

Note 1: Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
- 3: See the "Pin Diagrams" section for the 5V tolerant pins.

TABLE 31-5: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Op (unless othe Operating ter	perating Co erwise state mperature	nditions: 2.3 ed) -40°C ≤ TA ≤	√ to 3.6\ +85°C fc	/ or Industrial
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
MOS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4		50 50	MHz MHz	EC (Note 2) ECPLL (Note 1)

Note 1: PLL input requirements: 4 MHz \leq FPLLIN \leq 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 31-6:SPIX MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—	—	ns	_
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2	_	_	ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

TABLE 31-7: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—	_	ns	—
MSP11	TscH	SCKx Output High Time (Note 1,2)	Tsck/2	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	1	MILLIMETER	S	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section	Update Description			
4.0 "Memory Organization"	Added Memory Maps for the new devices (see Figure 4-3 and Figure 4-4).			
	Removed the BMXCHEDMA bit from the Bus Matrix Register map (see Table 4-1).			
	Added the REFOTRIM register, added the DIVSWEN bit to the REFOCON registers, added Note 4 to the ULOCK and SOSCEN bits and added the PBDIVRDY bit in the OSCCON register in the in the System Control Register map (see Table 4-16).			
	Removed the ALTI2C1 and ALTI2C2 bits from the DEVCFG3 register and added Note 1 to the UPLLEN and UPLLIDIV<2:0> bits of the DEVCFG2 register in the Device Configuration Word Summary (see Table 4-17).			
	Updated Note 1 in the Device and Revision ID Summary (see Table 4-18).			
	Added Note 2 to the PORTA Register map (see Table 4-19).			
	Added the ANSB6 and ANSB12 bits to the ANSELB register in the PORTB Register map (see Table 4-20).			
	Added Notes 2 and 3 to the PORTC Register map (see Table 4-21).			
	Updated all register names in the Peripheral Pin Select Register map (see Table 4-23).			
	Added values in support of new devices (16 KB RAM and 32 KB RAM) in the Data RAM Size register (see Register 4-5).			
	Added values in support of new devices (64 KB Flash and 128 KB Flash) in the Data RAM Size register (see Register 4-5).			
8.0 "Oscillator Configuration"	Added Note 5 to the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1).			
	Added the PBDIVRDY bit and Note 2 to the Oscillator Control register (see Register 8-1).			
	Added the DIVSWEN bit and Note 3 to the Reference Oscillator Control register (see Register 8-3).			
	Added the REFOTRIM register (see Register 8-4).			
21.0 "10-bit Analog-to-Digital	Updated the ADC1 Module Block Diagram (see Figure 21-1).			
Converter (ADC)"	Updated the Notes in the ADC Input Select register (see Register 21-4).			
24.0 "Charge Time Measurement	Updated the CTMU Block Diagram (see Figure 24-1).			
	Added Note 3 to the CTMU Control register (see Register 24-1)			
26.0 "Special Features"	Added Note 1 and the PGEC4/PGED4 pin pair to the ICESEL<1:0> bits in DEVCFG0: Device Configuration Word 0 (see Register 26-1).			
	Removed the ALTI2C1 and ALTI2C2 bits from the Device Configuration Word 3 register (see Register 26-4).			
	Removed 26.3.3 "Power-up Requirements".			
	Added Note 3 to the Connections for the On-Chip Regulator diagram (see Figure 26-2).			
	Updated the Block Diagram of Programming, Debugging and Trace Ports diagram (see Figure 26-3).			

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