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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 40MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-VFTLA Exposed Pad |
| Supplier Device Package | 36-VTLA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f064c-v-tl |

**TABLE 8: PIN NAMES FOR 36-PIN USB DEVICES**

**36-PIN VTLA (TOP VIEW)(1,2,3,5)**

**PIC32MX210F016C**
**PIC32MX220F032C**
**PIC32MX230F064C**
**PIC32MX250F128C**

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| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 | 19 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 | 20 | RPC9/CTED7/RC9 |
| 3 | PGED4(4)/AN6/RPC0/RC0 | 21 | VSS |
| 4 | PGEC4(4)/AN7/RPC1/RC1 | 22 | VCAP |
| 5 | VDD | 23 | VDD |
| 6 | VSS | 24 | PGED2/RPB10/D+/CTED11/RB10 |
| 7 | OSC1/CLKI/RPA2/RA2 | 25 | PGEC2/RPB11/D-/RB11 |
| 8 | OSC2/CLKO/RPA3/PMA0/RA3 | 26 | VUSB3V3 |
| 9 | SOSCI/RPB4/RB4 | 27 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 10 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 28 | CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14 |
| 11 | AN12/RPC3/RC3 | 29 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 12 | VSS | 30 | AVSS |
| 13 | VDD | 31 | AVDD |
| 14 | VDD | 32 | $\overline{\text{MCLR}}$ |
| 15 | TMS/RPB5/USBID/RB5 | 33 | PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 |
| 16 | VBUS | 34 | PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 |
| 17 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 35 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 |
| 18 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 36 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

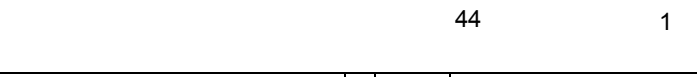
**4:** This pin function is not available on PIC32MX210F016C and PIC32MX120F032C devices.

**5:** Shaded pins are 5V tolerant.

**TABLE 9: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES**

**44-PIN QFN (TOP VIEW)(1,2,3,5)**

**PIC32MX110F016D**
**PIC32MX120F032D**
**PIC32MX130F064D**
**PIC32MX130F256D**
**PIC32MX150F128D**
**PIC32MX170F256D**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | RPB9/SDA1/CTED4/PMD3/RB9 | 23 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2 |
| 2 | RPC6/PMA1/RC6 | 24 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 |
| 3 | RPC7/PMA0/RC7 | 25 | AN6/RPC0/RC0 |
| 4 | RPC8/PMA5/RC8 | 26 | AN7/RPC1/RC1 |
| 5 | RPC9/CTED7/PMA6/RC9 | 27 | AN8/RPC2/PMA2/RC2 |
| 6 | VSS | 28 | VDD |
| 7 | VCAP | 29 | VSS |
| 8 | PGED2/RPB10/CTED11/PMD2/RB10 | 30 | OSC1/CLKI/RPA2/RA2 |
| 9 | PGEC2/RPB11/PMD1/RB11 | 31 | OSC2/CLKO/RPA3/RA3 |
| 10 | AN12/PMD0/RB12 | 32 | TDO/RPA8/PMA8/RA8 |
| 11 | AN11/RPB13/CTPLS/PMRD/RB13 | 33 | SOSCI/RPB4/RB4 |
| 12 | PGED4(4)/TMS/PMA10/RA10 | 34 | SOSCO/RPA4/T1CK/CTED9/RA4 |
| 13 | PGEC4(4)/TCK/CTED8/PMA7/RA7 | 35 | TDI/RPA9/PMA9/RA9 |
| 14 | CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14 | 36 | RPC3/RC3 |
| 15 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 | 37 | RPC4/PMA4/RC4 |
| 16 | AVSS | 38 | RPC5/PMA3/RC5 |
| 17 | AVDD | 39 | VSS |
| 18 | $\overline{\text{MCLR}}$ | 40 | VDD |
| 19 | VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0 | 41 | PGED3/RPB5/PMD7/RB5 |
| 20 | VREF-/CVREF-/AN1/RPA1/CTED2/RA1 | 42 | PGEC3/RPB6/PMD6/RB6 |
| 21 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0 | 43 | RPB7/CTED3/PMD5/INT0/RB7 |
| 22 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1 | 44 | RPB8/SCL1/CTED10/PMD4/RB8 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.
**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.
**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
**4:** This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.
**5:** Shaded pins are 5V tolerant.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number[1] | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| SDA1 | 15 | 18 | 19 | 1 | I/O | ST | Synchronous serial data input/output for I2C1 |
| SCL2 | 4 | 7 | 2 | 24 | I/O | ST | Synchronous serial clock input/output for I2C2 |
| SDA2 | 3 | 6 | 1 | 23 | I/O | ST | Synchronous serial data input/output for I2C2 |
| TMS | 19[2]<br>11[3] | 22[2]<br>14[3] | 25[2]<br>15[3] | 12 | I | ST | JTAG Test mode select pin |
| TCK | 14 | 17 | 18 | 13 | I | ST | JTAG test clock input pin |
| TDI | 13 | 16 | 17 | 35 | O | — | JTAG test data input pin |
| TDO | 15 | 18 | 19 | 32 | O | — | JTAG test data output pin |
| RTCC | 4 | 7 | 2 | 24 | O | ST | Real-Time Clock alarm output |
| CVREF- | 28 | 3 | 34 | 20 | I | Analog | Comparator Voltage Reference (low) |
| CVREF+ | 27 | 2 | 33 | 19 | I | Analog | Comparator Voltage Reference (high) |
| CVREFOUT | 22 | 25 | 28 | 14 | O | Analog | Comparator Voltage Reference output |
| C1INA | 4 | 7 | 2 | 24 | I | Analog | Comparator Inputs |
| C1INB | 3 | 6 | 1 | 23 | I | Analog | |
| C1INC | 2 | 5 | 36 | 22 | I | Analog | |
| C1IND | 1 | 4 | 35 | 21 | I | Analog | |
| C2INA | 2 | 5 | 36 | 22 | I | Analog | |
| C2INB | 1 | 4 | 35 | 21 | I | Analog | |
| C2INC | 4 | 7 | 2 | 24 | I | Analog | |
| C2IND | 3 | 6 | 1 | 23 | I | Analog | |
| C3INA | 23 | 26 | 29 | 15 | I | Analog | |
| C3INB | 22 | 25 | 28 | 14 | I | Analog | |
| C3INC | 27 | 2 | 33 | 19 | I | Analog | |
| C3IND | 1 | 4 | 35 | 21 | I | Analog | |
| C1OUT | PPS | PPS | PPS | PPS | O | — | Comparator Outputs |
| C2OUT | PPS | PPS | PPS | PPS | O | — | |
| C3OUT | PPS | PPS | PPS | PPS | O | — | |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

**Note 1:** Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number[1] | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| USBID | 11[3] | 14[3] | 15[3] | 41[3] | I | ST | USB OTG ID detect |
| CTED1 | 27 | 2 | 33 | 19 | I | ST | CTMU External Edge Input |
| CTED2 | 28 | 3 | 34 | 20 | I | ST | |
| CTED3 | 13 | 16 | 17 | 43 | I | ST | |
| CTED4 | 15 | 18 | 19 | 1 | I | ST | |
| CTED5 | 22 | 25 | 28 | 14 | I | ST | |
| CTED6 | 23 | 26 | 29 | 15 | I | ST | |
| CTED7 | — | — | 20 | 5 | I | ST | |
| CTED8 | — | — | — | 13 | I | ST | |
| CTED9 | 9 | 12 | 10 | 34 | I | ST | |
| CTED10 | 14 | 17 | 18 | 44 | I | ST | |
| CTED11 | 18 | 21 | 24 | 8 | I | ST | |
| CTED12 | 2 | 5 | 36 | 22 | I | ST | |
| CTED13 | 3 | 6 | 1 | 23 | I | ST | |
| CTPLS | 21 | 24 | 27 | 11 | O | — | CTMU Pulse Output |
| PGED1 | 1 | 4 | 35 | 21 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 1 |
| PGEC1 | 2 | 5 | 36 | 22 | I | ST | Clock input pin for Programming/Debugging Communication Channel 1 |
| PGED2 | 18 | 21 | 24 | 8 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 2 |
| PGEC2 | 19 | 22 | 25 | 9 | I | ST | Clock input pin for Programming/Debugging Communication Channel 2 |
| PGED3 | 11[2] | 14[2] | 15[2] | 41[2] | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 3 |
| | 27[3] | 2[3] | 33[3] | 19[3] | | | |
| PGEC3 | 12[2] | 15[2] | 16[2] | 42[2] | I | ST | Clock input pin for Programming/ Debugging Communication Channel 3 |
| | 28[3] | 3[3] | 34[3] | 20[3] | | | |
| PGED4 | — | — | 3 | 12 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 4 |
| PGEC4 | — | — | 4 | 13 | I | ST | Clock input pin for Programming/ Debugging Communication Channel 4 |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

**Note 1:** Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

### 4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.

**REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **BMXDRMSZ<31:0>:** Data RAM Memory (DRM) Size bits
Static value that indicates the size of the Data RAM in bytes:
0x00001000 = Device has 4 KB RAM
0x00002000 = Device has 8 KB RAM
0x00004000 = Device has 16 KB RAM
0x00008000 = Device has 32 KB RAM
0x00010000 = Device has 64 KB RAM

**REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | BMXPUPBA<19:16> | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
| | BMXPUPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXPUPBA<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-20 **Unimplemented:** Read as '0'

bit 19-11 **BMXPUPBA<19:11>:** Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>:** Read-Only bits
This value is always '0', which forces 2 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.
**2:** The value in this register must be less than or equal to BMXPFMSZ.

**REGISTER 9-5: DCRCDATA: DMA CRC DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return '0' on any read.

**REGISTER 9-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

**REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)**

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
- 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
- 0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
- 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
- 0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
- 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
- 0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
- 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
- 0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
- 1 = A channel address error has been detected (either the source or the destination address is invalid)
- 0 = No interrupt is pending

**REGISTER 10-3: U1OTGSTAT: USB OTG STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | R-0 | U-0 | R-0 | R-0 | U-0 | R-0 |
| | ID | — | LSTATE | — | SESVD | SESEND | — | VBUSVD |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit
- 1 = No cable is attached or a "type B" cable has been inserted into the USB receptacle
- 0 = A "type A" OTG cable has been inserted into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit
- 1 = USB line state (SE0 (U1CON<6>) bit and JSTATE (U1CON<7>)) bit has been stable for previous 1 ms
- 0 = USB line state (SE0 and JSTATE) has not been stable for previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A or B device
- 0 = VBUS voltage is below Session Valid on the A or B device

bit 2 **SESEND:** B-Device Session End Indicator bit
- 1 = VBUS voltage is below Session Valid on the B device
- 0 = VBUS voltage is above Session Valid on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A device
- 0 = VBUS voltage is below Session Valid on the A device

**REGISTER 10-20: U1CNFG1: USB CONFIGURATION 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
| | UTEYE | UOEMON | — | USBSIDL | — | — | — | UASUSPND |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit
1 = Eye-Pattern Test is enabled
0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB $\overline{OE}$ Monitor Enable bit
1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving
0 = OE signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit
1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 10-5.
0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock.

**REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDL | TWDIS | TWIP | — | — | — |
| 7:0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
| | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Timer is enabled
- 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
- 1 = Writes to Timer1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:
- 1 = Asynchronous write to the Timer1 register in progress
- 0 = Asynchronous write to Timer1 register is complete

In Synchronous Timer mode:
This bit is read as '0'.

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value

**Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 14-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1,2) | — | — | — | — | — | — | — |
| 7:0 | U-0 | R-y | R-y | R-y | R-y | R-y | R/W-0 | R/W-0 |
| | — | SWDTPS<4:0> | | | | | WDTWINEN | WDTCLR |

| Legend: | y = Values set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit(1,2)
- 1 = Enables the WDT if it is not enabled by the device configuration
- 0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit
- 1 = Enable windowed Watchdog Timer
- 0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit
- 1 = Writing a '1' will clear the WDT
- 0 = Software cannot force this bit to a '0'

**Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.

**2:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 18-2: I2CxSTAT: I$^2$C STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| 7:0 | R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |

| Legend: | HS = Set in hardware | HSC = Hardware set/cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | C = Clearable bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I$^2$C master, applicable to master transmit operation)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I$^2$C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I$^2$C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I$^2$C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

**NOTES:**

**REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | — | — | — | — | — | — | — | ADM_EN |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADDR<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-1 |
| | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/W-0 | R-0 |
| | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ADM_EN:** Automatic Address Detect Mode Enable bit
- 1 = Automatic Address Detect mode is enabled
- 0 = Automatic Address Detect mode is disabled

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

When the ADM_EN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits
- 11 = Reserved, do not use
- 10 = Interrupt is generated and asserted while the transmit buffer is empty
- 01 = Interrupt is generated and asserted when all characters have been transmitted
- 00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):
- 1 = IrDA encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** Receiver Enable bit
- 1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module. UxRX pin is controlled by port.

bit 11 **UTXBRK:** Transmit Break bit
- 1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Break transmission is disabled or completed

bit 10 **UTXEN:** Transmit Enable bit
- 1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1).
- 0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset. UxTX pin is controlled by port.

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
- 1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

## 22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

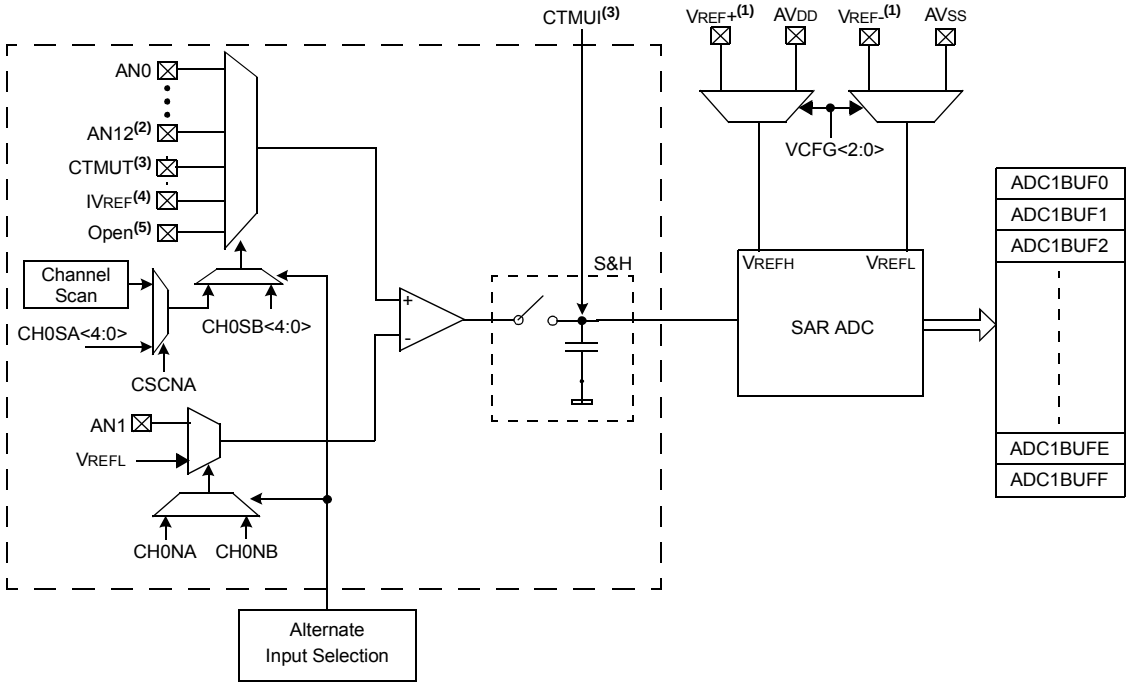
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 13 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. Figure 22-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

**FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM**




**Note 1:** VREF+ and VREF- inputs can be multiplexed with other analog inputs.

**2:** AN8 is only available on 44-pin devices. AN6, AN7, and AN12 are not available on 28-pin devices.

**3:** Connected to the CTMU module. See **Section 25.0 "Charge Time Measurement Unit (CTMU)"** for more information.

**4:** Internal precision voltage reference (1.2V).

**5:** This selection is only used with CTMU capacitive and time measurement.

## 27.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129), which are available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family devices include the following features intended to maximize application flexibility, reliability and minimize cost through elimination of external components.

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

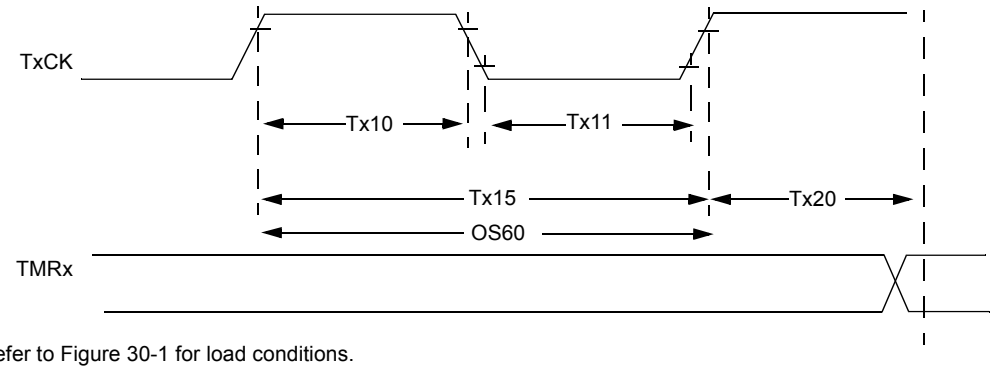
### 27.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- CFGCON: Configuration Control Register

In addition, the DEVID register (Register 27-6) provides device and revision information.

**FIGURE 30-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS**

| **AC CHARACTERISTICS(1)** | | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| TA10 | TTXH | TxCK High Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | — | ns | Must also meet parameter TA15 |
| | | | Asynchronous, with prescaler | 10 | — | — | ns | — |
| TA11 | TTXL | TxCK Low Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | — | ns | Must also meet parameter TA15 |
| | | | Asynchronous, with prescaler | 10 | — | — | ns | — |
| TA15 | TTXP | TxCK Input Period | Synchronous, with prescaler | [(Greater of 25 ns or 2 TPB)/N] + 30 ns | — | — | ns | VDD > 2.7V |
| | | | | [(Greater of 25 ns or 2 TPB)/N] + 50 ns | — | — | ns | VDD < 2.7V |
| | | | Asynchronous, with prescaler | 20 | — | — | ns | VDD > 2.7V **(Note 3)** |
| | | | | 50 | — | — | ns | VDD < 2.7V **(Note 3)** |
| OS60 | FT1 | SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting the TCS (T1CON<1>) bit) | | 32 | — | 100 | kHz | — |
| TA20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | — | 1 | TPB | — |

**Note 1:** Timer1 is a Type A timer.

**2:** This parameter is characterized, but not tested in manufacturing.

**3:** N = Prescale Value (1, 8, 64, 256).

**FIGURE 30-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS**

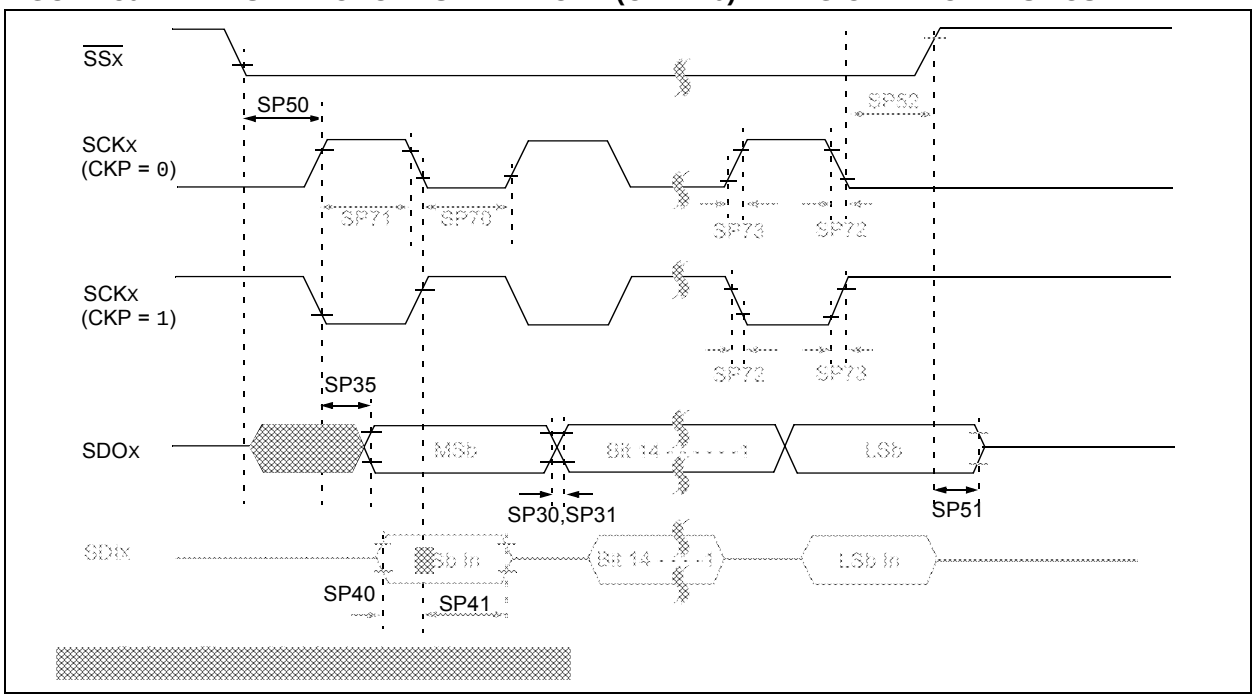



**TABLE 30-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See parameter DO32 |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input | 175 | — | — | ns | — |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 3)** | 5 | — | 25 | ns | — |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ after SCKx Edge | Tsck + 20 | — | — | ns | — |

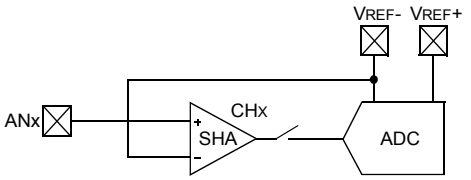
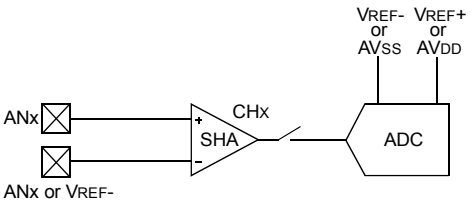
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 30-35: 10-BIT CONVERSION RATE PARAMETERS**

| AC CHARACTERISTICS(2) | | | Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **ADC Speed** | **TAD Min.** | **Sampling Time Min.** | **RS Max.** | **VDD** | **ADC Channels Configuration** |
| 1 Msps to 400 ksps(1) | 65 ns | 132 ns | 500Ω | 3.0V to 3.6V |  |
| Up to 400 ksps | 200 ns | 200 ns | 5.0 kΩ | 2.5V to 3.6V |  |

**Note 1:** External VREF- and VREF+ pins must be used for correct operation.

**2:** These parameters are characterized, but not tested in manufacturing.

**3:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.