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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f064ct-v-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 9: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

44-PIN QFN (TOP VIEW)^(1,2,3,5)

PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	Vdd
7	VCAP	29	Vss
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVDD	39	Vss
18	MCLR	40	Vdd
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

44

1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

5: Shaded pins are 5V tolerant.

Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note:	To access the following documents, refer
	to the Documentation > Reference
	Manuals section of the Microchip PIC32
	website: http://www.microchip.com/pic32

- Section 1. "Introduction" (DS60001127)
- Section 2. "CPU" (DS60001113)
- Section 3. "Memory Organization" (DS60001115)
- Section 5. "Flash Program Memory" (DS60001121)
- Section 6. "Oscillator Configuration" (DS60001112)
- Section 7. "Resets" (DS60001118)
- Section 8. "Interrupt Controller" (DS60001108)
- Section 9. "Watchdog Timer and Power-up Timer" (DS60001114)
- Section 10. "Power-Saving Features" (DS60001130)
- Section 12. "I/O Ports" (DS60001120)
- Section 13. "Parallel Master Port (PMP)" (DS60001128)
- Section 14. "Timers" (DS60001105)
- Section 15. "Input Capture" (DS60001122)
- Section 16. "Output Compare" (DS60001111)
- Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104)
- Section 19. "Comparator" (DS60001110)
- Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109)
- Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107)
- Section 23. "Serial Peripheral Interface (SPI)" (DS60001106)
- Section 24. "Inter-Integrated Circuit (I²C)" (DS60001116)
- Section 27. "USB On-The-Go (OTG)" (DS60001126)
- Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125)
- Section 31. "Direct Memory Access (DMA) Controller" (DS60001117)
- Section 32. "Configuration" (DS60001124)
- Section 33. "Programming and Diagnostics" (DS60001129)
- Section 37. "Charge Time Measurement Unit (CTMU)" (DS60001167)

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

Exception	Description
Reset	Assertion MCLR or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Вр	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

TABLE 3-3: MIPS32[®] M4K[®] PROCESSOR CORE EXCEPTION TYPES

3.3 Power Management

The MIPS M4K processor core offers many power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see Section 26.0 "Power-Saving Features".

3.4 EJTAG Debug Support

The MIPS M4K processor core provides an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

- bit 18-16 **PLLMULT<2:0>:** Phase-Locked Loop (PLL) Multiplier bits
 - 111 = Clock is multiplied by 24
 - 110 = Clock is multiplied by 21
 - 101 = Clock is multiplied by 20
 - 100 = Clock is multiplied by 19
 - 011 = Clock is multiplied by 18
 - 010 = Clock is multiplied by 17
 - 001 = Clock is multiplied by 16
 - 000 = Clock is multiplied by 15
- bit 15 Unimplemented: Read as '0'
- bit 14-12 COSC<2:0>: Current Oscillator Selection bits
 - 111 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (OSCCON<26:24>)
 - 110 = Internal Fast RC (FRC) Oscillator divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (Posc) (XT, HS or EC)
 - 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast RC (FRC) Oscillator
- bit 11 Unimplemented: Read as '0'
- bit 10-8 NOSC<2:0>: New Oscillator Selection bits
 - 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC Oscillator (FRC) divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (XT, HS or EC)
 - 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

bit 7 CLKLOCK: Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):

- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):

Clock and PLL selections are never locked and may be modified.

- bit 6 ULOCK: USB PLL Lock Status bit⁽¹⁾
 - 1 = The USB PLL module is in lock or USB PLL module start-up timer is satisfied
 - 0 =The USB PLL module is out of lock or USB PLL module start-up timer is in progress or the USB PLL is disabled
- bit 5 SLOCK: PLL Lock Status bit
 - 1 = The PLL module is in lock or PLL module start-up timer is satisfied
 - 0 = The PLL module is out of lock, the PLL start-up timer is running, or the PLL is disabled
- bit 4 SLPEN: Sleep Mode Enable bit
 - 1 = The device will enter Sleep mode when a WAIT instruction is executed
 - 0 = The device will enter Idle mode when a WAIT instruction is executed
- **Note 1:** This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	_		—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:10	—	—	—	—	—	—	—	—	
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	
15:8	0N ⁽¹⁾	—	_	SUSPEND	DMABUSY	—	—	—	
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
7:0	_	_	_	_	_	_	_	_	

REGISTER 9-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ON: DMA On bit⁽¹⁾
 - 1 = DMA module is enabled
 - 0 = DMA module is disabled
- bit 14-13 **Unimplemented:** Read as '0'
- bit 12 SUSPEND: DMA Suspend bit
 - 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
 - 0 = DMA operates normally

bit 11 DMABUSY: DMA Module Busy bit

- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data
- bit 10-0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-3: U1OTGSTAT: USB OTG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
51.24	—	—	—	—	—	—		—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	-	—	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15:8	—	—	_	_	_	_		_	
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0	
7:0	ID	_	LSTATE	_	SESVD	SESEND		VBUSVD	

Legend:

Logonal							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-8 Unimplemented: Read as '0'

- bit 7 ID: ID Pin State Indicator bit
 - 1 = No cable is attached or a "type B" cable has been inserted into the USB receptacle
 - 0 = A "type A" OTG cable has been inserted into the USB receptacle
- bit 6 Unimplemented: Read as '0'
- bit 5 LSTATE: Line State Stable Indicator bit
 - 1 = USB line state (SE0 (U1CON<6>) bit and JSTATE (U1CON<7>)) bit has been stable for previous 1 ms 0 = USB line state (SE0 and JSTATE) has not been stable for previous 1 ms

bit 4 Unimplemented: Read as '0'

- bit 3 SESVD: Session Valid Indicator bit
 - 1 = VBUS voltage is above Session Valid on the A or B device
 - 0 = VBUS voltage is below Session Valid on the A or B device
- bit 2 SESEND: B-Device Session End Indicator bit
 - 1 = VBUS voltage is below Session Valid on the B device
 - 0 = VBUS voltage is above Session Valid on the B device

bit 1 Unimplemented: Read as '0'

- bit 0 VBUSVD: A-Device VBUS Valid Indicator bit
 - 1 = VBUS voltage is above Session Valid on the A device
 - 0 = VBUS voltage is below Session Valid on the A device

Bit Range	Bit 31/23/15/7	Bit Bit 31/23/15/7 30/22/14/6		Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	—	—		—	—	—	_	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—		—	—	—	_	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—		—	—	—	_	—
	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R-0	R/WC-0, HS
7:0	STALLE		RESIMEIE(2)		TRNIE(3)	SOFIE		URSTIF ⁽⁵⁾
	UTALLI			IDELII		0011		DETACHIF ⁽⁶⁾

REGISTER 10-6: U1IR: USB INTERRUPT REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit					
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-8 Unimplemented: Read as '0'

bit 7		STALLIF: STALL Handshake Interrupt bit
	-	1 = In Host mode a STALL handshake was received during the handshake phase of the transaction
	I	In Device mode a STALL handshake was transmitted during the handshake phase of the transaction
	(0 = STALL handshake has not been sent
bit 6		ATTACHIF: Peripheral Attach Interrupt bit ⁽¹⁾
	-	1 = Peripheral attachment was detected by the USB module
	(0 = Peripheral attachment was not detected
bit 5		RESUMEIF: Resume Interrupt bit ⁽²⁾
	-	$1 = K$ -State is observed on the D+ or D- pin for 2.5 μ s
	(0 = K-State is not observed
bit 4	I	IDLEIF: Idle Detect Interrupt bit
	-	1 = Idle condition detected (constant Idle state of 3 ms or more)
L:1 0	-	U = NO IDE CONDITION DELECTED
DIT 3		IRNIF: Token Processing Complete Interrupt Dit ^{ery}
	-	$\Gamma = \Gamma$ recessing of current token not complete.
hit 2	Ċ	SOFIE: SOF Taken Interrunt hit
		1 = SOE token received by the peripheral or the SOE threshold reached by the host
	(0 = SOF token was not received nor threshold reached
bit 1	I	UERRIF: USB Error Condition Interrupt bit ⁽⁴⁾
		1 = Unmasked error condition has occurred
	(0 = Unmasked error condition has not occurred
bit 0	l	URSTIF: USB Reset Interrupt bit (Device mode) ⁽⁵⁾
	-	1 = Valid USB Reset has occurred
	(0 = No USB Reset has occurred
		DETACHIF: USB Detach Interrupt bit (Host mode) ⁽⁶⁾
	-	1 = Peripheral detachment was detected by the USB module
	(0 = Peripheral detachment was not detected
Note	1:	This bit is valid only if the HOSTEN bit is set (see Register 10-11), there is no activity on the USB for
		2.5 μ s, and the current bus state is not SE0.
	2:	When not in Suspend mode, this interrupt should be disabled.
	3:	Clearing this bit will cause the STAT FIFO to advance.
	4:	Only error conditions enabled through the U1FIF register will set this bit
	5:	
	6.	Host mode
	υ.	nost mode.

REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
 - 1 = Reset all Even/Odd buffer pointers to the EVEN Buffer Descriptor banks
 - 0 = Even/Odd buffer pointers are not Reset
- bit 0 USBEN: USB Module Enable bit⁽⁴⁾
 - 1 = USB module and supporting circuitry is enabled
 - 0 = USB module and supporting circuitry is disabled

SOFEN: SOF Enable bit⁽⁵⁾

- 1 = SOF token is sent every 1 ms
- 0 = SOF token is disabled
- **Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
 - 2: All host control logic is reset any time that the value of this bit is toggled.
 - 3: Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
 - 4: Device mode.
 - 5: Host mode.

11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digitalonly peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin.

Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



12.2 Timer1 Control Registers

TABLE 12-1: TIMER1 REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Name ⁽¹⁾ Bit Range								В	its								6
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000 740		31:16	_	—	—	—	-	—	—	—	-	—	—	-	—	-	-	—	0000
0000	TICON	15:0	ON	_	SIDL	TWDIS	TWIP	—	_	—	TGATE	_	TCKP	S<1:0>	—	TSYNC	TCS	_	0000
0610		31:16	_	_	—	—	—	—	_	—	—	_	_	—	—	—	—	_	0000
0610		15:0								TMR1	<15:0>								0000
0620	DD1	31:16	_	_	_	_	_	_	_	_	_	_		_	_	_	_	_	0000
	PR1	15:0								PR1<	<15:0>								FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 3 Unimplemented: Read as '0'
 bit 2 TSYNC: Timer External Clock Input Synchronization Selection bit When TCS = 1: 1 = External clock input is synchronized 0 = External clock input is not synchronized When TCS = 0: This bit is ignored.
 bit 1 TCS: Timer Clock Source Select bit 1 = External clock from TxCKI pin
 - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
31:24	—	— HR10<1:0>			HR01<3:0>						
00.40	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
23:10	—	MIN10<2:0>				MIN01<3:0>					
45.0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
15:8	—		SEC10<2:0>		SEC01<3:0>						
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
7:0	—	—	—	—	_	_	_	_			
		•									
l egend.											

REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

bit 29-28 HR10<1:0>: Binary Coded Decimal value of hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9 bit 23 **Unimplemented:** Read as '0'

bit 22-20 MIN10<2:0>: Binary Coded Decimal value of minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9 bit 15 **Unimplemented:** Read as '0'

bit 14-12 SEC10<2:0>: Binary Coded Decimal value of seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 Unimplemented: Read as '0'

25.1 CTMU Control Registers

TABLE 25-1: CTMU REGISTER MAP

ess			Bits											6					
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
A 200		31:16	EDG1MOD	EDG1POL		EDG15	SEL<3:0>		EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL		EDG28	SEL<3:0>		—	—	0000
A200		15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG			ITRIM	<5:0>			IRNG	i<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- · MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

DC CHARACTERISTICS			Standa (unless Operati	rd Operatii s otherwise ing tempera	n g Condi stated) ture -40 -40	tions:)°C ≤ T)°C ≤ T	ions: 2.3V to 3.6V °C \leq TA \leq +85°C for Industrial °C \leq TA \leq +105°C for V-temp			
Param. No.	^{n.} Symbol Characteristics			Typical ⁽¹⁾	Max.	Units	Conditions			
		Program Flash Memory ⁽³⁾								
D130	Eр	Cell Endurance	20,000	—	—	E/W	_			
D131	Vpr	VDD for Read	2.3	—	3.6	V	—			
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—			
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated			
D135	IDDP	Supply Current during Programming	_	10	—	mA	_			
	Tww	Word Write Cycle Time	—	411	—	es	See Note 4			
D136	Trw	Row Write Cycle Time	—	6675	—	Cycl	See Note 2,4			
D137	Тре	Page Erase Cycle Time	—	20011	—	с С	See Note 4			
	TCE	Chip Erase Cycle Time	—	80180		ц Ц	See Note 4			

TABLE 30-12: DC CHARACTERISTICS: PROGRAM MEMORY

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on FRC accuracy (See Table 30-19) and FRC tuning values (See Register 8-2).

TABLE 30-14: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard (unless of Operating	Operatin therwise tempera	ng Conditions e stated) ture $-40^{\circ}C \le$ $-40^{\circ}C \le$	TA ≤ +8 TA ≤ +8 TA ≤ +1	to 3.6V 35°C for Industrial 105°C for V-temp			
Param. No.	Symbol	Characteristics	Min. Typ. Max. Units Comments							
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	_		10	μs	See Note 1			
D313	D313 DACREFH	CVREF Input Voltage	AVss	—	AVDD	V	CVRSRC with CVRSS = 0			
		Reference Range	VREF-	—	VREF+	V	CVRSRC with CVRSS = 1			
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size			
			0.25 x DACREFH	_	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size			
D315	DACRES	Resolution	—	—	DACREFH/24	-	CVRCON <cvrr> = 1</cvrr>			
			_	—	DACREFH/32	_	CVRCON <cvrr> = 0</cvrr>			
D316	DACACC	Absolute Accuracy ⁽²⁾		_	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>			
			—	_	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>			

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 30-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			Standa (unles Operat	ard Operat s otherwis ing temper	ing Cor se stated ature	nditions d) -40°C ≤ -40°C ≤	: 2.3V to 3.6V TA \leq +85°C for Industrial TA \leq +105°C for V-temp		
Param. No.	Symbol	Characteristics	Min.	Min. Typical Max. Units			Comments		
D321	Cefc	External Filter Capacitor Value	8	10	_	μF	Capacitor must be low series resistance (1 ohm). Typical voltage on the VCAP pin is 1.8V.		



FIGURE 30-13: SPIX MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

TABLE 30-31: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHA	ARACTERIS	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time (Note 3)	Tsck/2		_	ns	_
SP71	TscH	SCKx Input High Time (Note 3)	Tsck/2	—	-	ns	—
SP72	TscF	SCKx Input Fall Time	—	5	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	5	10	ns	_
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	—	_	_	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	—	—	_	ns	See parameter DO31
SP35	TscH2doV,	SDOx Data Output Valid after	_	—	20	ns	VDD > 2.7V
	TscL2DoV	SCKx Edge	—	—	30	ns	VDD < 2.7V
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	_	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—		ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input	175			ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 3: The minimum clock period for SCKx is 50 ns.
- **4:** Assumes 50 pF load on all SPIx pins.

TABLE 30-39: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	ram. No. Symbol Characteristics ⁽¹⁾			Тур.	Max.	Units	Conditions	
PM11	Twr	PMWR Pulse Width	_	1 Трв	_	_	_	
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	_	2 Трв	_	_	_	
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 Трв	—	—	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 30-40: OTG ELECTRICAL SPECIFICATIONS

АС СНА	AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. Max. Units Condition					
USB313	VUSB3V3	USB Voltage	3.0	_	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation	
USB315	VILUSB	Input Low Voltage for USB Buffer	_	—	0.8	V	—	
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	_	V	—	
USB318	VDIFS	Differential Input Sensitivity	—	_	0.2	V	The difference between D+ and D- must exceed this value while VCM is met	
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—	
USB320	Zout	Driver Output Impedance	28.0	—	44.0	Ω	—	
USB321	Vol	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3	
USB322	Vон	Voltage Output High	2.8		3.6	V	1.425 k Ω load connected to ground	



NOTES:

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units	MILLIMETERS			
Dimensior	Limits	MIN	NOM	MAX	
Number of Pins	Ν		36		
Number of Pins per Side	ND		10		
Number of Pins per Side	NE		8		
Pitch	е		0.50 BSC		
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.025	-	0.075	
Overall Width	E		5.00 BSC		
Exposed Pad Width	E2	3.60	3.75	3.90	
Overall Length	D		5.00 BSC		
Exposed Pad Length	D2	3.60	3.75	3.90	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.20	0.25	0.30	
Contact-to-Exposed Pad	K	0.20	-	_	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2