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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f064d-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

bit 3	CF: Clock Fail Detect bit
	1 = FSCM has detected a clock failure
	0 = No clock failure has been detected
bit 2	UFRCEN: USB FRC Clock Enable bit <sup>(1)</sup>
	<ul> <li>1 = Enable the FRC as the clock source for the USB clock source</li> <li>0 = Use the Primary Oscillator or USB PLL as the USB clock source</li> </ul>
bit 1	SOSCEN: Secondary Oscillator (Sosc) Enable bit
	1 = Enable the Secondary Oscillator
	0 = Disable the Secondary Oscillator
bit 0	OSWEN: Oscillator Switch Enable bit
	<ul> <li>1 = Initiate an oscillator switch to selection specified by NOSC&lt;2:0&gt; bits</li> <li>0 = Oscillator switch is complete</li> </ul>
Note 1:	This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

## PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTE	:K 9-0: D					KUL KEGIS	IER							
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0						
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0						
31.24	—	—	—	_	—	—	—	—						
22:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1						
23.10	CHAIRQ<7:0> <sup>(1)</sup>													
15.0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1						
15:8	CHSIRQ<7:0> <sup>(1)</sup>													
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0						
7.0	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN									

#### CISTER 0-8. CIETED

Legend:	S = Settable bit						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

## bit 31-24 Unimplemented: Read as '0'

bit

bit

bit

bit

bit

bit

31-24	Unimplemented. Read as 0
23-16	CHAIRQ<7:0>: Channel Transfer Abort IRQ bits <sup>(1)</sup>
	11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
	•
	•
	00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag 00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag
15-8	CHSIRQ<7:0>: Channel Transfer Start IRQ bits <sup>(1)</sup>
	11111111 = Interrupt 255 will initiate a DMA transfer
	•
	•
	•
	00000001 = Interrupt 0 will initiate a DMA transfer
7	CEORCE: DMA Forced Transfer bit
1	
	<ul> <li>1 = A DMA transfer is forced to begin when this bit is written to a '1'</li> <li>0 = This bit always reads '0'</li> </ul>
6	CABORT: DMA Abort Transfer bit
	1 = A DMA transfer is aborted when this bit is written to a '1'
	0 = This bit always reads '0'
5	PATEN: Channel Pattern Match Abort Enable bit
	1 = Abort transfer and clear CHEN on pattern match
	0 = Pattern match is disabled
4	SIRQEN: Channel Start IRQ Enable bit
	1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

- - 0 = Interrupt number CHSIRQ is ignored and does not start a transfer
- bit 3 AIRQEN: Channel Abort IRQ Enable bit
  - 1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
  - 0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer
- bit 2-0 Unimplemented: Read as '0'
- Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

## PIC32MX1XX/2XX 28/36/44-PIN FAMILY

#### REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)

- bit 1 CRC5EF: CRC5 Host Error Flag bit<sup>(4)</sup>
  - 1 = Token packet rejected due to CRC5 error
  - 0 = Token packet accepted
  - EOFEF: EOF Error Flag bit<sup>(3,5)</sup>
  - 1 = An EOF error condition was detected
  - 0 = No EOF error condition was detected
- bit 0 PIDEF: PID Check Failure Flag bit
  - 1 = PID check failed
  - 0 = PID check passed
- **Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
  - **2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
  - **3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
  - 4: Device mode.
  - 5: Host mode.

## 11.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 12. "I/O Ports" (DS60001120), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

General purpose I/O pins are the simplest of peripherals. They allow the PIC<sup>®</sup> MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions. These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Key features of this module include:

- · Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.



#### TABLE 11-4: PORTB REGISTER MAP

ess										Bits									
Virtual Addr (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6100	ANSEL B	31:16	_	—	—	—	-	-	_	—	-	-	—	_	_	—	—	_	0000
0100	,	15:0	ANSB15	ANSB14	ANSB13	ANSB12 <sup>(2)</sup>	_		—	—	_	_	—	—	ANSB3	ANSB2	ANSB1	ANSB0	E00F
6110	TRISB	31:16	_	_	_	—	—	_	—	—	—		—	_	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12(2)	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6(2)	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6120	PORTB	31:16	_		_		_	—	_	_	_		_						0000
		15:0	RB15	RB14	RB13	RB12(2)	RB11	RB10	RB9	RB8	RB7	RC6(2)	RB5	RB4	RB3	RB2	RB1	RB0	XXXX
6130	LATB	31:16		-	-		-	-	—	-			-	-	—	—	-	—	0000
		15:0	LAIB15	LAIB14	LAIB13	LAIB12(2)	LAI B11	LAIB10	LATB9	LAI B8	LAIB7	LAIB6(2)	LAI B5	LAI B4	LATB3	LATB2	LAIB1	LAIBO	XXXX
6140	ODCB	31:16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB1	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCR0	0000
6150	CNPUB	31:16																	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12-	CNPUBIT	CNPUBIU	CNPUB9	CNPUB8	CNPUB/	CNPUB6-	CNP0B5	CNPUB4	CNP0B3	CNP0B2	CNPUBI	CNPUBU	0000
6160	CNPDB	31:10																	0000
		15.0	CNPDB15	CINPUB14	CNPDB13	CNPDB12	CNPDBT	CNPDBIU	CNPDB9	CNPDBo	CNPDB/	CNPDB0	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDBI	CNPDBU	0000
6170	CNCONB	15.0			SIDI														0000
		31.16																	0000
6180	CNENB	15.0	CNIEB15	CNIEB14	CNIEB13	CNIEB11(2)	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6(2)	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
		31:16	_	_	_	_	_	_				_							0000
6190	CNSTATB		CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	
		15:0	STATB15	STATB14	STATB13	STATB12(2)	STATB11	STATB10	STATB9	STATB8	STATB7	STATB6 <sup>(2)</sup>	STATB5	STATB4	STATB3	STATB2	STATB1	STATB0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: This bit is not available on PIC32MX2XX devices. The reset value for the TRISB register when this bit is not available is 0x0000EFBF.

#### REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 3 Unimplemented: Read as '0'
  bit 2 TSYNC: Timer External Clock Input Synchronization Selection bit When TCS = 1: 1 = External clock input is synchronized 0 = External clock input is not synchronized When TCS = 0: This bit is ignored.
  bit 1 TCS: Timer Clock Source Select bit 1 = External clock from TxCKI pin
  - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## 16.1 Output Compare Control Registers

### TABLE 16-1: OUTPUT COMPARE 1-OUTPUT COMPARE 5 REGISTER MAP

ess										В	its								
Virtual Addr (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3000	00100	31:16	—	—	—	—	—	—	—	_	—	—	—	—	—		—	_	0000
0000	001001	15:0	ON _ SIDL OC32 OCFLT OCTSEL OCM<2:0>														0000		
3010	OC1R	31:16 15:0	OC1R<31:0>															xxxx	
3020	OC1RS	31:16 15:0	OC1RS<31:0>															XXXX	
0000	00000	31:16	—	_	_	_	_	_		_	—	—	_	_	_	_	—	—	0000
3200	UC2CON	15:0	ON	_	SIDL	_	_	_	_	_	_	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
2210	0028	31:16		0028-21:05														XXXX	
3210	UCZR	15:0		UC2R<31:0>														xxxx	
3220	00288	31:16		00205-21:05														XXXX	
3220	00283	15:0		UU2KS<31:0>													XXXX		
3400	003000	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_		—		0000
3400	003001	15:0	ON	_	SIDL	_	_	_	_	_	-	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3410	OC3R	31:16 15:0								OC3R	<31:0>								XXXX XXXX
2420	00200	31:16								00000	221.05								XXXX
3420	00383	15:0								UCSRC	5-51.0-								XXXX
3600		31:16	—	_	_	_	_	_	_	_	—	—	_	—	—	_	—	_	0000
3000	004001	15:0	ON	_	SIDL	_	_	_	_	_	-	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3610	OC4R	31:16								OC4R	<31.0>								XXXX
3010	0041	15:0								0041	-01.02								xxxx
3620	OC4PS	31:16									221.05								xxxx
3020	00410	15:0								00400	0-01.0-								xxxx
3800		31:16	-	_	—	_	_	_	_	_	-	_	—	—	—		—		0000
3000	000001	15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3810	OC5R	31:16								00.5R	<31.0>								xxxx
3010	0000	15:0								OUJK	-01.02								xxxx
3820	OC5RS	31:16																	xxxx
3020	00010	15 <sup>.</sup> 0								00000	-01.02								xxxx

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Legend: x = unknown value on Reset; -- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

## REGISTER 18-2: I2CxSTAT: I<sup>2</sup>C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	-	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	_	—	—
45.0	R-0, HSC R-0, HSC		U-0	U-0 U-0		R/C-0, HS	R-0, HSC	R-0, HSC
15:8	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
7.0	R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
7:0	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF

Legend:	HS = Set in hardware	HSC = Hardware set/cleared						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'						
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit					

#### bit 31-16 Unimplemented: Read as '0'

bit 15 ACKSTAT: Acknowledge Status bit (when operating as I<sup>2</sup>C master, applicable to master transmit operation) 1 = Acknowledge was not received from slave 0 = Acknowledge was received from slave Hardware set or clear at end of slave Acknowledge. bit 14 **TRSTAT:** Transmit Status bit (when operating as I<sup>2</sup>C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK) 0 = Master transmit is not in progress Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge. bit 13-11 Unimplemented: Read as '0' bit 10 BCL: Master Bus Collision Detect bit 1 = A bus collision has been detected during a master operation 0 = No collisionHardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module. bit 9 GCSTAT: General Call Status bit 1 = General call address was received 0 = General call address was not received Hardware set when address matches general call address. Hardware clear at Stop detection. bit 8 ADD10: 10-bit Address Status bit 1 = 10-bit address was matched 0 = 10-bit address was not matched Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

#### bit 7 IWCOL: Write Collision Detect bit

1 = An attempt to write the I2CxTRN register failed because the I <sup>2</sup> C module is busy
0 = No collision

Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

#### bit 6 I2COV: Receive Overflow Flag bit

1 = A byte was received while the I2CxRCV register is still holding the previous byte 0 = No overflow

Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

#### bit 5 **D\_A:** Data/Address bit (when operating as I<sup>2</sup>C slave)

- 1 = Indicates that the last byte received was data
- 0 = Indicates that the last byte received was device address

Hardware clear at device address match. Hardware set by reception of slave byte.

## 24.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- · Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

A block diagram of the module is shown in Figure 24-1.



## 24.1 Comparator Voltage Reference Control Register

ess	Register Name <sup>(1)</sup>	Bit Range		Bits															
Virtual Addr (BF80_#)			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
0000	CVRCON	31:16	_	—	—	_	_	—	_	_	_	—	-	_	-	—	—	_	0000
9000	CVRCON	15:0	ON	_		_	_	_	_	_	_	CVROE	CVRR	CVRSS		CVR<	3:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

## 25.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 37. "Charge Time Measurement Unit (CTMU)" (DS60001167), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.



- Up to 13 channels available for capacitive or time measurement input
- · On-chip precision current source
- 16-edge input trigger sources
- · Selection of edge or level-sensitive inputs
- · Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- · High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- · Control of current source during auto-sampling
- · Four current source ranges
- · Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 25-1.



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The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- · On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

### 26.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

- Note 1: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a Posc of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.
  - 2: Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from Posc to LPRC just prior to entering Sleep in order to save power. No oscillator startup delay would be applied when exiting Idle. However, when switching back to Posc, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

#### 26.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P	
31:24	—	—	—	—	— — FWDTWINSZ<				
00.40	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P	
23:10	FWDTEN	WINDIS	—	WDTPS<4:0>					
45.0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P	
15:8	FCKSM	/<1:0>	FPBDI	IV<1:0> — OSCIOFNC POSCMOD<1:				OD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P	
	IESO	—	FSOSCEN	— — FNOSC<2:0>					

#### REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Legend: r = Reserved bit		P = Programmable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

#### bit 31-26 Reserved: Write '1'

bit 25-24 FWDTWINSZ<1:0>: Watchdog Timer Window Size bits

- 11 = Window size is 25%
- 10 = Window size is 37.5%
- 01 = Window size is 50%
- 00 = Window size is 75%

#### bit 23 FWDTEN: Watchdog Timer Enable bit

- 1 = Watchdog Timer is enabled and cannot be disabled by software
- 0 = Watchdog Timer is not enabled; it can be enabled in software

#### bit 22 WINDIS: Watchdog Timer Window Enable bit

- 1 = Watchdog Timer is in non-Window mode
- 0 = Watchdog Timer is in Window mode

#### bit 21 Reserved: Write '1'

#### bit 20-16 WDTPS<4:0>: Watchdog Timer Postscale Select bits

0
10100 <b>= 1:1048576</b>
10011 <b>= 1:524288</b>
10010 <b>= 1:262144</b>
10001 <b>= 1:131072</b>
10000 <b>= 1:65536</b>
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 <b>= 1:2048</b>
01010 = 1:1024
01001 = 1:512
01000 <b>= 1:256</b>
00111 <b>= 1:128</b>
00110 = 1:64
00101 <b>= 1:32</b>
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

**Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

## 29.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers (MCU) and dsPIC<sup>®</sup> digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB<sup>®</sup> X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM<sup>™</sup> Assembler
  - MPLINK<sup>™</sup> Object Linker/ MPLIB<sup>™</sup> Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

### 29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows<sup>®</sup>, Linux and Mac OS<sup>®</sup> X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- · Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- · Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window
- Project-Based Workspaces:
- Multiple projects
- Multiple tools
- · Multiple configurations
- · Simultaneous debugging sessions

File History and Bug Tracking:

- · Local file history feature
- Built-in support for Bugzilla issue tracker

### 29.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM<sup>™</sup> and dsPICDEM<sup>™</sup> demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ<sup>®</sup> security ICs, CAN, IrDA<sup>®</sup>, PowerSmart battery management, SEEVAL<sup>®</sup> evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

## 29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent<sup>®</sup> and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika<sup>®</sup>

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D300	VIOFF	Input Offset Voltage	-	±7.5	±25	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	_	Vdd	V	AVDD = VDD, AVss = Vss (Note 2)
D302	CMRR	Common Mode Rejection Ratio	55	—	_	dB	Max VICM = (VDD - 1)V (Note 2)
D303A	TRESP	Large Signal Response Time	—	150	400	ns	AVDD = VDD, AVSS = VSS (Note 1,2)
D303B	TSRESP	Small Signal Response Time	-	1	_	μs	This is defined as an input step of 50 mV with 15 mV of overdrive (Note 2)
D304	ON2ov	Comparator Enabled to Output Valid	-		10	μS	Comparator module is configured before setting the comparator ON bit (Note 2)
D305	IVREF	Internal Voltage Reference	1.14	1.2	1.26	V	—
D312	TSET	Internal Comparator Voltage DRC Reference Setting time			10	μs	(Note 3)

#### TABLE 30-13: COMPARATOR SPECIFICATIONS

**Note 1:** Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from Vss to VDD.

**2:** These parameters are characterized but not tested.

**3:** Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

**4:** The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

#### TABLE 31-5: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Op (unless othe Operating ter	perating Co erwise state mperature	nditions: 2.3 ed) -40°C ≤ TA ≤	<b>√ to 3.6\</b> +85°C fc	/ or Industrial
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
MOS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4		50 50	MHz MHz	EC <b>(Note 2)</b> ECPLL <b>(Note 1)</b>

Note 1: PLL input requirements: 4 MHz  $\leq$  FPLLIN  $\leq$  5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

**2:** This parameter is characterized, but not tested in manufacturing.

### TABLE 31-6:SPIX MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—	—	ns	_
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2	_	_	ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

#### TABLE 31-7: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard (unless of Operating	<b>I Operatir</b> otherwise g temperat	ng Condit stated) ture -40	°C ≤ TA	<b>3V to 3.6V</b> ≤ +85°C for Industrial
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Тур.	Max.	Units	Conditions
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—	_	ns	—
MSP11	TscH	SCKx Output High Time (Note 1,2)	Tsck/2	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

## 32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 32-1: I/O OUTPUT VOLTAGE HIGH (VOH)





# 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	Limits	MIN	NOM	MAX		
Contact Pitch	Contact Pitch E		0.65 BSC			
Optional Center Pad Width	W2			4.25		
Optional Center Pad Length	T2			4.25		
Contact Pad Spacing	C1		5.70			
Contact Pad Spacing	C2		5.70			
Contact Pad Width (X28)	X1			0.37		
Contact Pad Length (X28)	Y1			1.00		
Distance Between Pads	G	0.20				

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

## **Revision F (February 2014)**

This revision includes the addition of the following devices:

In addition, this revision includes the following major changes as described in Table A-5, as well as minor updates to text and formatting, which were incorporated throughout the document.

- PIC32MX170F256B PIC32MX270F256B
- PIC32MX170F256D
   PIC32MX270F256D

#### TABLE A-5: MAJOR SECTION UPDATES

Section	Update Description
32-bit Microcontrollers (up to 256	Added new devices to the family features (see Table 1 and Table 2).
KB Flash and 64 KB SRAM) with	Updated pin diagrams to include new devices (see "Pin Diagrams").
Audio and Graphics Interfaces, USB, and Advanced Analog	
1.0 "Device Overview"	Added Note 3 reference to the following pin names: VBUS, VUSB3V3, VBUSON,
	D+, D-, and USBID.
2.0 "Guidelines for Getting	Replaced Figure 2-1: Recommended Minimum Connection.
Started with 32-bit MCUs"	Updated Figure 2-2: MCLR Pin Connections.
	Added 2.9 "Sosc Design Recommendation".
4.0 "Memory Organization"	Added memory tables for devices with 64 KB RAM (see Table 4-4 through Table 4-5).
	Changed the Virtual Addresses for all registers and updated the PWP bits in the DEVCFG: Device Configuration Word Summary (see Table 4-17).
	Updated the ODCA, ODCB, and ODCC port registers (see Table 4-19, Table 4-20, and Table 4-21).
	The RTCTIME, RTCDATE, ALRMTIME, and ALRMDATE registers were updated (see Table 4-25).
	Added Data Ram Size value for 64 KB RAM devices (see Register 4-5).
	Added Program Flash Size value for 256 KB Flash devices (see Register 4-5).
12.0 "Timer1"	The Timer1 block diagram was updated to include the 16-bit data bus (see Figure 12-1).
13.0 "Timer2/3, Timer4/5"	The Timer2-Timer5 block diagram (16-bit) was updated to include the 16-bit data bus (see Figure 13-1).
	The Timer2/3, Timer4/5 block diagram (32-bit) was updated to include the 32- bit data bus (see Figure 13-1).
19.0 "Parallel Master Port (PMP)"	The CSF<1:0> bit value definitions for '00' and '01' were updated (see Register 19-1).
	Bit 14 in the Parallel Port Address register (PMADDR) was updated (see Register 19-3).
20.0 "Real-Time Clock and	The following registers were updated:
Calendar (RTCC)"	RTCTIME (see Register 20-3)
	RTCDATE (see Register 20-4)
	ALRMTIME (see Register 20-5)
	ALRMDATE (see Register 20-6)
26.0 "Special Features"	Updated the PWP bits (see Register 26-1).
29.0 "Electrical Characteristics"	Added parameters DO50 and DO50a to the Capacitive Loading Requirements
	Added Note 5 to the IDD DC Characteristics (see Table 29-5)
	Added Note 4 to the JIDI E DC Characteristics (see Table 29-6).
	Added Note 5 to the IPD DC Characteristics (see Table 29-7).
	Updated the conditions for parameters USB321 (VOL) and USB322 (VOH) in the OTG Electrical Specifications (see Table 29-38).
Product Identification System	Added 40 MHz speed information.