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Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f064d-v-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 13: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

44-PIN VTLA (TOP VIEW)^(1,2,3,5)

PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	VDD
7	VCAP	29	Vss
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVdd	39	Vss
18	MCLR	40	VDD
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

44

1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

5: Shaded pins are 5V tolerant.



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 μF to 47 μF . This capacitor should be located as close to the device as possible.

2.3 Capacitor on Internal Voltage Regulator (VCAP)

2.3.1 INTERNAL REGULATOR MODE

A low-ESR (3 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **30.0 "Electrical Characteristics"** for additional information on CEFC specifications.

2.4 Master Clear (MCLR) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions:

- Device Reset
- Device programming and debugging

Pulling The $\overline{\text{MCLR}}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{\text{MCLR}}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.



EXAMPLE OF MCLR PIN CONNECTIONS



3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

NOTES:

5.1 Flash Controller Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

ess		Ċ,		Bits															
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E400		31:16		—	—	—	—		—	—	—	—	—	_	—	—			0000
1400		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	_	_	_	_	_	_			NVMO	P<3:0>		0000
E410		31:16									/~21.0>								0000
1410		15:0									S1.02								0000
E420		31:16									D-21.05								0000
F420	NVINADUR' /	15:0								INVIVIADD	K~31.0~								0000
E420		31:16		000										0000					
F430	NVINDATA	15:0		0000															
E440		31:16										0000							
F440	NVIVISRCADDR	15:0													0000				

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
	NVMKEY<31:24>										
00.40	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
23:10	NVMKEY<23:16>										
45.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
15:8	NVMKEY<15:8>										
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
				NVMK	EY<7:0>						

REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMKEY<31:0>: Unlock Register bits

These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	NVMADDR<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:10	NVMADDR<23:16>										
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	NVMADDR<15:8>										
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
				NVMA	DR<7:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMADDR<31:0>: Flash Address bits

Bulk/Chip/PFM Erase: Address is ignored. Page Erase: Address identifies the page to erase. Row Program: Address identifies the row to program. Word Program: Address identifies the word to program.

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

(1)	IRQ	Vector		Interru	pt Bit Location		Persistent
Interrupt Source ⁽¹⁾	#	#	Flag	Enable	Priority	Sub-priority	Interrupt
		Highes	st Natural O	rder Priority	,		
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1E – SPI1 Fault	36	31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1TX – SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—		—	—			—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	_	—		_	_			_		
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15:8	—	—	-	—	—		-	—		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0				BDTPTR	H<23:16>					

REGISTER 10-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **BDTPTRH<23:16>:** Buffer Descriptor Table Base Address bits This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	_	—	_	—	—	_	—	—		
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15.0	—	—	—	—	—	—	—	—		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				BDTPTR	U<31:24>					

REGISTER 10-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **BDTPTRU<31:24>:** Buffer Descriptor Table Base Address bits This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

12.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (Sosc) for Real-Time Clock (RTC) applications.

FIGURE 12-1: TIMER1 BLOCK DIAGRAM

The following modes are supported:

- · Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

12.1 Additional Supported Features

- · Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)

Figure 12-1 illustrates a general block diagram of Timer1.



REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

- bit 3 T32: 32-Bit Timer Mode Select bit⁽²⁾
 - 1 = Odd numbered and even numbered timers form a 32-bit timer
 - 0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2 Unimplemented: Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit⁽³⁾
 - 1 = External clock from TxCK pin
 - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
 - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

NOTES:

REGISTI	ER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)								
bit 17	SPIFE: Frame Sync Pulse Edge Select bit (Framed SPI mode only)								
	1 = Frame synchronization pulse coincides with the first bit clock								
bit 16	ENHBITE: Enhanced Buffer Enable bit ⁽²⁾								
Sit 10	1 = Enhanced Buffer mode is enabled								
	0 = Enhanced Buffer mode is disabled								
bit 15	ON: SPI Peripheral On bit ⁽¹⁾								
	1 = SPI Peripheral is enabled								
hit 14	Unimplemented: Read as '0'								
bit 13	SIDL: Stop in Idle Mode bit								
	1 = Discontinue module operation when the device enters Idle mode								
	0 = Continue module operation when the device enters Idle mode								
bit 12	DISSDO: Disable SDOx pin bit								
	1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register $0 = SDOx pin is controlled by the module$								
bit 11-10	MODE<32.16>: 32/16-Bit Communication Select bits								
	When AUDEN = 1:								
	MODE32 MODE16 Communication								
	1 1 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame								
	1 0 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame								
	0 0 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame								
	When AUDEN = 0:								
	MODE32 MODE16 Communication								
	1 x 32-bit								
	0 0 8-bit								
bit 9	SMP: SPI Data Input Sample Phase bit								
	Master mode (MSTEN = 1):								
	 Input data sampled at end of data output time Input data sampled at middle of data output time 								
	Slave mode (MSTEN = 0):								
	SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.								
	To write a '1' to this bit, the MSTEN value = 1 must first be written.								
bit 8	CKE: SPI Clock Edge Select bit ⁽³⁾								
	1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit) 0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)								
bit 7	SSEN: Slave Select Enable (Slave mode) bit								
bit i	$1 = \overline{SSx}$ pin used for Slave mode								
	$0 = \overline{SSx}$ pin not used for Slave mode, pin controlled by port function.								
bit 6	CKP: Clock Polarity Select bit ⁽⁴⁾								
	1 = 1 dle state for clock is a high level; active state is a low level 0 = 1 dle state for clock is a low level; active state is a high level								
Note 1:	When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in								
	the SYSCLK cycle immediately following the instruction that clears the module's ON bit.								
2:	This bit can only be written when the ON bit = 0.								
3:	I his bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).								
4:	When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value								
	of CKP.								

2

REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 5 MSTEN: Master Mode Enable bit
 - 1 = Master mode
 - 0 = Slave mode
- bit 4 DISSDI: Disable SDI bit
 - 1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
 - 0 = SDI pin is controlled by the SPI module
- bit 3-2 STXISEL<1:0>: SPI Transmit Buffer Empty Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
 - 10 = Interrupt is generated when the buffer is empty by one-half or more
 - 01 = Interrupt is generated when the buffer is completely empty
 - 00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
- bit 1-0 SRXISEL<1:0>: SPI Receive Buffer Full Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is full
 - 10 = Interrupt is generated when the buffer is full by one-half or more
 - 01 = Interrupt is generated when the buffer is not empty
 - 00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit can only be written when the ON bit = 0.
 - 3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - 4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	-	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	_	—
15.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7.0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7.0	AUDEN ⁽¹⁾	—	—	—	AUDMONO ^(1,2)	—	AUDMOD)<1:0> ^(1,2)

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 SPISGNEXT: Sign Extend Read Data from the RX FIFO bit
 - 1 = Data from RX FIFO is sign extended
 - 0 = Data from RX FIFO is not sign extended
- bit 14-13 Unimplemented: Read as '0'
- bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
 - 1 = Frame Error overflow generates error events
 - 0 = Frame Error does not generate error events
- bit 11 SPIROVEN: Enable Interrupt Events via SPIROV bit
 - 1 = Receive overflow generates error events
 - 0 = Receive overflow does not generate error events
- bit 10 SPITUREN: Enable Interrupt Events via SPITUR bit
 - 1 = Transmit underrun generates error events
 - 0 = Transmit underrun does not generate error events
- bit 9 IGNROV: Ignore Receive Overflow bit (for Audio Data Transmissions)
 - 1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
 0 = A ROV is a critical error that stops SPI operation
- bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
 - 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
 - 0 = A TUR is a critical error that stops SPI operation
- bit 7 AUDEN: Enable Audio CODEC Support bit⁽¹⁾
- 1 = Audio protocol enabled
 - 0 = Audio protocol disabled
- bit 6-5 Unimplemented: Read as '0'
- bit 3 AUDMONO: Transmit Audio Data Format bit^(1,2)
 - 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
 - 0 = Audio data is stereo
- bit 2 Unimplemented: Read as '0'
- bit 1-0 AUDMOD<1:0>: Audio Protocol Mode bit^(1,2)
 - 11 = PCM/DSP mode
 - 10 = Right-Justified mode
 - 01 = Left-Justified mode
 - $00 = I^2S \mod$
- **Note 1:** This bit can only be written when the ON bit = 0.
 - **2:** This bit is only valid for AUDEN = 1.

19.1 UART Control Registers

TABLE 19-1: UART1 AND UART2 REGISTER MAP

ess										Bi	ts								
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6000		31:16			—	—	—			—		_					—		0000
0000	OTWODE	15:0	ON	_	SIDL	IREN	RTSMD	-	UEN	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSE	L<1:0>	STSEL	0000
6010	111STA(1)	31:16	-	—	—	—	—	-	—	ADM_EN				ADDF	R<7:0>				0000
0010	UIUIA	15:0	UTXISE	EL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISI	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6020		31:16	-	—	—	—	—	-	—	_	_	—	-	-	—	—	—	—	0000
0020	UTIXILO	15:0	-	—	—	—	—	-	—				Tra	insmit Regi	ster				0000
6030		31:16		_	—	_	_		_	_		_			_	_	_	_	0000
0000	UIIVILO	15:0	-	—	—	—	—	-	—				Re	ceive Regis	ster				0000
6040		31:16	-	—	—	—	—	-	—	_	_	—	-	-	—	—	—	—	0000
0040	OTBICO	15:0							Bau	d Rate Gen	erator Pres	caler					-		0000
6200	112MODE(1)	31:16	-	—	—	—	—	-	—	_	_	—	-	-	—	—	—	—	0000
0200	02INIODE.	15:0	ON	—	SIDL	IREN	RTSMD	_	UEN	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSE	L<1:0>	STSEL	0000
6210	112STA(1)	31:16	_	—				_	—	ADM_EN				ADDF	R<7:0>		-		0000
0210	02017	15:0	UTXISE	EL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISI	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6220	LI2TXREG	31:16	_	—	—			_	—	—	_	—	—		—	—	—	—	0000
0220	15:0		_		_	_	_	_	—				Tra	insmit Regi	ster				0000
6230		31:16	-	—	—	—	—	-	—	_	_	—	-	-	—	—	—	—	0000
0230	OZIVAREO	15:0	_		_	_	_	_	—				Re	ceive Regis	ster				0000
6240	U2BRG(1)	31:16	_	—	—			—	—	—	_	—	—	_	—	—		—	0000
52-70	OZDINO.	15:0							Bau	d Rate Gen	erator Pres	caler							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
15:8		VCFG<2:0>		OFFCAL	—	CSCNA	—	—
7.0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	BUFS	—		SMP	1<3:0>		BUFM	ALTS

REGISTER 22-2: AD1CON2: ADC CONTROL REGISTER 2

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-13 VCFG<2:0>: Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	AVss
001	External VREF+ pin	AVss
010	AVdd	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVss

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the sample and hold amplifier are connected to VREFL

0 = Disable Offset Calibration mode

The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 Unimplemented: Read as '0'

- bit 10 **CSCNA:** Input Scan Select bit
 - 1 = Scan inputs
 - 0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1.

1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7

0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 Unimplemented: Read as '0'

bit 5-2 SMPI<3:0>: Sample/Convert Sequences Per Interrupt Selection bits

```
1111 = Interrupts at the completion of conversion for each 16<sup>th</sup> sample/convert sequence
```

```
1110 = Interrupts at the completion of conversion for each 15<sup>th</sup> sample/convert sequence
```

- .
- •

0001 = Interrupts at the completion of conversion for each 2^{nd} sample/convert sequence 0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 BUFM: ADC Result Buffer Mode Select bit

- 1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
 - 0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 ALTS: Alternate Input Sample Mode Select bit

- 1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
- 0 = Always use Sample A input multiplexer settings

PIC32MX1XX/2XX 28/36/44-PIN FAMILY





TABLE 30-34: ADC MODULE SPECIFICATIONS

	AC CHAF	ACTERISTICS	$\begin{array}{ll} \mbox{Standard Operating Conditions (see Note 5): 2.5V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions		
ADC Ac	curacy – N	leasurements with Inter	nal VREF+/V	REF-					
AD20d	Nr	Resolution		10 data bits	6	bits	(Note 3)		
AD21d	INL	Integral Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)		
AD22d	DNL	Differential Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Notes 2,3)		
AD23d	Gerr	Gain Error	> -4	_	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)		
AD24d	Eoff	Offset Error	> -2	_	< 2	Lsb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)		
AD25d	—	Monotonicity	—	—	—		Guaranteed		
Dynami	c Performa	ance	·				·		
AD32b	SINAD	Signal to Noise and Distortion	55	58.5		dB	(Notes 3,4)		
AD34b	ENOB	Effective Number of bits	9.0	9.5		bits	(Notes 3,4)		

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimensior	n Limits	MIN	NOM	MAX
Number of Pins	Ν		28	
Pitch	е		.100 BSC	
Top to Seating Plane	Α	-	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	с	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	MILLIMETERS			
Dimensior	Limits	MIN	NOM	MAX
Number of Pins	Ν		36	
Number of Pins per Side	ND		10	
Number of Pins per Side	NE		8	
Pitch	е		0.50 BSC	
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	_

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Optional Center Pad Width	W2			6.80	
Optional Center Pad Length	T2			6.80	
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Width (X44)	X1			0.35	
Contact Pad Length (X44)	Y1			0.80	
Distance Between Pads	G	0.25			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A