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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f064dt-i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

		Pin Nu	mber <sup>(1)</sup>				
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
OC1	PPS	PPS	PPS	PPS	0	_	Output Compare Output 1
OC2	PPS	PPS	PPS	PPS	0	—	Output Compare Output 2
OC3	PPS	PPS	PPS	PPS	0	—	Output Compare Output 3
OC4	PPS	PPS	PPS	PPS	0	—	Output Compare Output 4
OC5	PPS	PPS	PPS	PPS	0	—	Output Compare Output 5
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault B Input
INT0	13	16	17	43	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4
RA0	27	2	33	19	I/O	ST	PORTA is a bidirectional I/O port
RA1	28	3	34	20	I/O	ST	1
RA2	6	9	7	30	I/O	ST	1
RA3	7	10	8	31	I/O	ST	1
RA4	9	12	10	34	I/O	ST	1
RA7	_	_	_	13	I/O	ST	1
RA8	_	_	_	32	I/O	ST	
RA9	_	_	_	35	I/O	ST	1
RA10	_	_	_	12	I/O	ST	
RB0	1	4	35	21	I/O	ST	PORTB is a bidirectional I/O port
RB1	2	5	36	22	I/O	ST	7
RB2	3	6	1	23	I/O	ST	7
RB3	4	7	2	24	I/O	ST	
RB4	8	11	9	33	I/O	ST	
RB5	11	14	15	41	I/O	ST	
RB6	12 <sup>(2)</sup>	15 <b>(2)</b>	16 <b>(2)</b>	42 <sup>(2)</sup>	I/O	ST	
RB7	13	16	17	43	I/O	ST	
RB8	14	17	18	44	I/O	ST	
RB9	15	18	19	1	I/O	ST	
RB10	18	21	24	8	I/O	ST	
RB11	19	22	25	9	I/O	ST	
RB12	20 <sup>(2)</sup>	23 <sup>(2)</sup>	26 <sup>(2)</sup>	10 <sup>(2)</sup>	I/O	ST	1
RB13	21	24	27	11	I/O	ST	1
RB14	22	25	28	14	I/O	ST	1
RB15	23	26	29	15	I/O	ST	
Legend:	CMOS = CN	MOS compa	atible input	or output		Analog =	Analog input P = Power
	SI = Schmi	tt Irigger in	put with CN	VIOS levels		O = Outp	out I = Input
Note 1.			lod for rofo	ronco only	See the	"Pin Diag	$m_{\text{rem}} = N/A$

#### DINOUT I/O DESCRIPTIONS (CONTINUED)

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	_	—	—		—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	—	—	_	—	—	—	—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0			
15:8	BMXDKPBA<15:8>										
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
7:0				BMXDK	PBA<7:0>						

#### REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

### Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 BMXDKPBA<9:0>: Read-Only bits This value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

## 8.0 OSCILLATOR CONFIGURATION

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 6. "Oscillator
	Configuration" (DS60001112), which is
	available from the Documentation >
	Reference Manual section of the
	Microchip PIC32 web site
	(www.microchip.com/pic32).

The PIC32MX1XX/2XX 28/36/44-pin Family oscillator system has the following modules and features:

- Four external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

A block diagram of the oscillator system is provided in Figure 8-1.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	—	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHSSIZ<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0				CHSSIZ	<7:0>						

#### REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

# Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSSIZ<15:0>: Channel Source Size bits

1111111111111111 = 65,535 byte source size

#### **REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	—	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	—	—	—	—	—	—	—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
10.0	CHDSIZ<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0				CHDSIZ	<u>/</u> <7:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

IABL		PEI			1 SELEC		PUIRE	GISTER		CONTR									
SS										В	its								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FB4C	RPB8R	31:16	—	—	—	-	—	—	—	—	—	—	_	—	_	—	—	—	0000
		15:0		_									_			RPB8	<3:0>		0000
FB50	RPB9R	31:16		_	_	_	_	_			_	_			_			—	0000
		15:0	—	_	—	_	_	_	_	_	_	_	_	_		RPB9	<3:0>		0000
FB54	RPB10R	31:16	—	—	-	-	—	—	_	—	—	—	_	—	—	—	—	—	0000
	-	15:0	_	_	—		_	—	_	_	_	_	_	_		RPB10	)<3:0>		0000
FB58	RPB11R	31:16	_	_	—		_	—	_	_	_	_	_	_	_	—	_	_	0000
		15:0		_	_		—	—					_	_		RPB1 <sup>-</sup>	1<3:0>		0000
FB60	RPB13R	31:16		—	—	—	—	—	—	—	—	—	—	—	—				0000
		15:0		—	—	—	—	—	—	—	—	—	—	—		RPB1	3<3:0>		0000
FB64	RPB14R	31:16		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0		—	—	—	—	—	—	—	—	—	—	—		RPB14	4<3:0>		0000
FB68	RPB15R	31:16	—	—	—	—	-		—	—				—	—		—	—	0000
	1. 5101	15:0	—	—	—	—	-		—	—				—		RPB1	5<3:0>		0000
FB6C	RPCOR(3)	31:16	—	—	—	-	—	—	—	—	—	—	—	—	—	—	—	—	0000
. 200		15:0	—	—	—	-	—	—	—	—	—	—	—	—		RPC0	<3:0>		0000
EB70	RPC1R(3)	31:16	_	—	—	—	_	_	_	_	—	—	_	—	_	—	_	—	0000
1 870	NI OIIX	15:0	_	—	—	—	_	_	_	_	—	—	_	—		RPC1	<3:0>		0000
FB74		31:16	_	—	—	—	_	_	_	_	—	—	_	—	_	—	_	—	0000
1014		15:0	_	—	—	—	_	_	_	_	—	—	_	—		RPC2	<3:0>		0000
EB78		31:16		—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	0000
1 0/0		15:0		—	—	—	—	—	—	—	—	—	—	—		RPC3	<3:0>		0000
FB7C		31:16		—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	0000
1 B/C		15:0	_	—	—	—	—	—	—	—	—	—	—	—		RPC4	<3:0>		0000
EDOO		31:16	-	—	—	—	—	—	—	—	—	—	—	—	-	—	_	-	0000
1 000	NF GOINT	15:0	_	—	—	—	—	—	—	—	—	—	—	—		RPC5	<3:0>		0000
ED94		31:16	—	—	—	—	—	—	_	—	—	—	—	—	—	—	—	—	0000
гро4	NFUUR	15:0	—	—	—	—	—	—	_	—	—	—	—	—		RPC6	<3:0>		0000
ED80		31:16	—	—	—	—	—	—	_	—	—	—	—	—	—	—	—	—	0000
F 000	KFU/KU	15:0	_	_	_	_	_	_		_	_	_	_	_		RPC7	<3:0>		0000

#### OT AUTOUT DEALATED MAD

x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

This register is only available on 44-pin devices. Note 1:

2: 3:

This register is only available on PIC32MX1XX devices. This register is only available on 36-pin and 44-pin devices.

#### 12.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (Sosc) for Real-Time Clock (RTC) applications.

FIGURE 12-1: TIMER1 BLOCK DIAGRAM

The following modes are supported:

- · Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

#### 12.1 Additional Supported Features

- · Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)

Figure 12-1 illustrates a general block diagram of Timer1.



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>					
00.40	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0			
23.10	MCLKSEL <sup>(2)</sup>	—	—	-	—	—	SPIFE	ENHBUF <sup>(2)</sup>			
15.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
10.0	ON <sup>(1)</sup>	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE <sup>(3)</sup>			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0	SSEN	CKP <sup>(4)</sup>	MSTEN	DISSDI	STXISE	L<1:0> SRXISE		EL<1:0>			

#### REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 FRMEN: Framed SPI Support bit

- 1 = Framed SPI support is enabled (SSx pin used as FSYNC input/output)
   0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on <u>SSx</u> pin bit (Framed SPI mode only)
  - 1 = Frame sync pulse input (Slave mode)
  - 0 = Frame sync pulse output (Master mode)
- bit 29 FRMPOL: Frame Sync Polarity bit (Framed SPI mode only)
  - 1 = Frame pulse is active-high
  - 0 = Frame pulse is active-low
- bit 28 MSSEN: Master Mode Slave Select Enable bit
  - 1 = Slave select SPI support enabled. The SS pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
  - 0 = Slave select SPI support is disabled.
- bit 27 FRMSYPW: Frame Sync Pulse Width bit
  - $\ensuremath{\mathtt{1}}$  = Frame sync pulse is one character wide
  - 0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in FRAMED\_SYNC mode.
  - 111 = Reserved; do not use
  - 110 = Reserved; do not use
  - 101 = Generate a frame sync pulse on every 32 data characters
  - 100 = Generate a frame sync pulse on every 16 data characters
  - 011 = Generate a frame sync pulse on every 8 data characters
  - 010 = Generate a frame sync pulse on every 4 data characters
  - 001 = Generate a frame sync pulse on every 2 data characters
  - 000 = Generate a frame sync pulse on every data character
- bit 23 MCLKSEL: Master Clock Enable bit<sup>(2)</sup>
  - 1 = REFCLK is used by the Baud Rate Generator
  - 0 = PBCLK is used by the Baud Rate Generator
- bit 22-18 Unimplemented: Read as '0'
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: This bit can only be written when the ON bit = 0.
  - **3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
  - 4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

#### REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	-	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	_	—
15.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7.0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7:0	AUDEN <sup>(1)</sup>	_	_	—	AUDMONO <sup>(1,2)</sup>	—	AUDMOD	)<1:0> <sup>(1,2)</sup>

#### Legend:

R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-16 Unimplemented: Read as '0'

- bit 15 SPISGNEXT: Sign Extend Read Data from the RX FIFO bit
  - 1 = Data from RX FIFO is sign extended
  - 0 = Data from RX FIFO is not sign extended
- bit 14-13 Unimplemented: Read as '0'
- bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
  - 1 = Frame Error overflow generates error events
  - 0 = Frame Error does not generate error events
- bit 11 SPIROVEN: Enable Interrupt Events via SPIROV bit
  - 1 = Receive overflow generates error events
    - 0 = Receive overflow does not generate error events
- bit 10 SPITUREN: Enable Interrupt Events via SPITUR bit
  - 1 = Transmit underrun generates error events
  - 0 = Transmit underrun does not generate error events
- bit 9 IGNROV: Ignore Receive Overflow bit (for Audio Data Transmissions)
  - 1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
     0 = A ROV is a critical error that stops SPI operation
- bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
  - 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
  - 0 = A TUR is a critical error that stops SPI operation
- bit 7 AUDEN: Enable Audio CODEC Support bit<sup>(1)</sup>
- 1 = Audio protocol enabled
  - 0 = Audio protocol disabled
- bit 6-5 Unimplemented: Read as '0'
- bit 3 AUDMONO: Transmit Audio Data Format bit<sup>(1,2)</sup>
  - 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
  - 0 = Audio data is stereo
- bit 2 Unimplemented: Read as '0'
- bit 1-0 AUDMOD<1:0>: Audio Protocol Mode bit<sup>(1,2)</sup>
  - 11 = PCM/DSP mode
  - 10 = Right-Justified mode
  - 01 = Left-Justified mode
  - $00 = I^2S \mod$
- **Note 1:** This bit can only be written when the ON bit = 0.
  - 2: This bit is only valid for AUDEN = 1.

## **REGISTER 18-2:** I2CxSTAT: I<sup>2</sup>C STATUS REGISTER (CONTINUED)

bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware set or clear when Start, Repeated Start or Stop detected.
bit 3	S: Start bit
	<ul> <li>1 = Indicates that a Start (or Repeated Start) bit has been detected last</li> <li>0 = Start bit was not detected last</li> </ul>
	Hardware set or clear when Start, Repeated Start or Stop detected.
bit 2	<b>R_W:</b> Read/Write Information bit (when operating as I <sup>2</sup> C slave)
	1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave
	Hardware set or clear after reception of I <sup>2</sup> C device address byte.
bit 1	RBF: Receive Buffer Full Status bit
	1 = Receive complete, I2CxRCV is full
	0 = Receive not complete, I2CxRCV is empty
	Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit
	1 = Transmit in progress, I2CxTRN is full

0 = Transmit complete, I2CxTRN is empty

Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

NOTES:

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
51.24	EDG1MOD	EDG1POL		EDG1S	SEL<3:0>		EDG2STAT	EDG1STAT
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
23.10	EDG2MOD	EDG2POL		EDG2S	—	—		
15.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	ON	—	CTMUSIDL	TGEN <sup>(1)</sup>	EDGEN	EDGSEQEN	IDISSEN <sup>(2)</sup>	CTTRIG
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0			ITRIM	1<5:0>			IRNG	<1:0>

#### REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER

#### Legend:

Logonan			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 31 EDG1MOD: Edge1 Edge Sampling Select bit
  - 1 = Input is edge-sensitive
  - 0 = Input is level-sensitive
- bit 30 EDG1POL: Edge 1 Polarity Select bit
  - 1 = Edge1 programmed for a positive edge response
  - 0 = Edge1 programmed for a negative edge response
- bit 29-26 EDG1SEL<3:0>: Edge 1 Source Select bits
  - 1111 = C3OUT pin is selected
    - 1110 = C2OUT pin is selected
    - 1101 = C1OUT pin is selected
    - 1100 = IC3 Capture Event is selected
    - 1011 = IC2 Capture Event is selected
    - 1010 = IC1 Capture Event is selected
    - 1001 = CTED8 pin is selected
    - 1000 = CTED7 pin is selected
    - 0111 = CTED6 pin is selected
    - 0110 = CTED5 pin is selected
    - 0101 = CTED4 pin is selected
    - 0100 = CTED3 pin is selected
    - 0011 = CTED1 pin is selected
    - 0010 = CTED2 pin is selected
    - 0001 = OC1 Compare Event is selected 0000 = Timer1 Event is selected

#### bit 25 EDG2STAT: Edge2 Status bit

Indicates the status of Edge2 and can be written to control edge source

- 1 = Edge2 has occurred
- 0 = Edge2 has not occurred
- Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
  - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
  - 3: Refer to the CTMU Current Source Specifications (Table 30-41) in Section 30.0 "Electrical Characteristics" for current values.
  - 4: This bit setting is not available for the CTMU temperature diode.

						0			
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.04	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1	
31:24	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—		—	_	
22.16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	
23.10	—	—	—	—	—	—	—	-	
15.0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P	
15.0	USERID<15:8>								
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P	
7.0				USERID<	7:0>				

#### REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 FVBUSONIO: USB VBUSON Selection bit

- 1 = VBUSON pin is controlled by the USB module 0 = VBUSON pin is controlled by the port function
- bit 30 **FUSBIDIO:** USB USBID Selection bit 1 = USBID pin is controlled by the USB module 0 = USBID pin is controlled by the port function
- bit 29 IOL1WAY: Peripheral Pin Select Configuration bit
  - 1 = Allow only one reconfiguration
  - 0 = Allow multiple reconfigurations
- bit 28 PMDI1WAY: Peripheral Module Disable Configuration bit
  - 1 = Allow only one reconfiguration
  - 0 = Allow multiple reconfigurations
- bit 27-16 Reserved: Write '1'
- bit 15-0 USERID<15:0>: User ID bits

This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit Bit 27/19/11/3 26/18/*		Bit 25/17/9/1	Bit 24/16/8/0
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	—	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	_	—	—	—	—	—	_	—
45.0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
15:8	—	—	IOLOCK <sup>(1)</sup>	PMDLOCK <sup>(1)</sup>	—	—		_
7.0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-1	R/W-1
7:0	—	_	_	_	JTAGEN	_		TDOEN

#### **REGISTER 27-5: CFGCON: CONFIGURATION CONTROL REGISTER**

#### Legend:

Logonan			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-14 Unimplemented: Read as '0'

- bit 13 IOLOCK: Peripheral Pin Select Lock bit<sup>(1)</sup>
  - 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
  - 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.
- bit 12 PMDLOCK: Peripheral Module Disable bit<sup>(1)</sup>
  - 1 = Peripheral module is locked. Writes to PMD registers is not allowed.
  - 0 = Peripheral module is not locked. Writes to PMD registers is allowed.

#### bit 11-4 Unimplemented: Read as '0'

- bit 3 JTAGEN: JTAG Port Enable bit
  - 1 = Enable the JTAG port
    - 0 = Disable the JTAG port
- bit 2-1 Unimplemented: Read as '1'
- bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG bit
  - 1 = 2-wire JTAG protocol uses TDO
  - 0 = 2-wire JTAG protocol does not use TDO
- Note 1: To change this bit, the unlock sequence must be performed. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp					
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DO10	Vol	Output Low Voltage	_	_	0.4	V	$\text{Iol} \leq 10 \text{ mA}, \text{ Vdd} = 3.3 \text{V}$
		Output High Voltage	1.5 <sup>(1)</sup>	_	_		IOH $\ge$ -14 mA, VDD = 3.3V
020	Мон	I/O Pins	2.0 <sup>(1)</sup>	—	—	V	IOH $\ge$ -12 mA, VDD = 3.3V
0020	VOH		2.4	_	_	v	Ioh $\geq$ -10 mA, Vdd = 3.3V
			3.0(1)	_	_		$IOH \ge -7 \text{ mA}, \text{ VDD} = 3.3 \text{V}$

#### TABLE 30-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized, but not tested.

#### TABLE 30-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp					
Param. No.	Symbol	Characteristics	Min. <sup>(1)</sup> Typical Max. Units Conditions				Conditions
BO10	VBOR	BOR Event on VDD transition high-to-low <sup>(2)</sup>	2.0		2.3	V	_

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Conditions				
		Program Flash Memory <sup>(3)</sup>						
D130	Eр	Cell Endurance	20,000	—	—	E/W	_	
D131	Vpr	VDD for Read	2.3	—	3.6	V	—	
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated	
D135	IDDP	Supply Current during Programming	_	10	—	mA	—	
	Tww	Word Write Cycle Time	—	411	—	es	See Note 4	
D136	Trw	Row Write Cycle Time	—	6675	—	Cycl	See Note 2,4	
D137	Тре	Page Erase Cycle Time	—	20011	—	с С	See Note 4	
	TCE	Chip Erase Cycle Time	—	80180		ц Ц	See Note 4	

#### TABLE 30-12: DC CHARACTERISTICS: PROGRAM MEMORY

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on FRC accuracy (See Table 30-19) and FRC tuning values (See Register 8-2).

#### TABLE 30-14: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard (unless of Operating	Operatin therwise tempera	ng Conditions e stated) ture $-40^{\circ}C \le$ $-40^{\circ}C \le$	<b>TA ≤ +8</b> TA ≤ +8 TA ≤ +1	<b>o 3.6V</b> 5°C for Industrial 05°C for V-temp
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	_		10	μs	See Note 1
D313	DACREFH	CVREF Input Voltage	AVss	—	AVDD	V	CVRSRC with CVRSS = 0
		Reference Range	VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24	-	CVRCON <cvrr> = 1</cvrr>
			_	—	DACREFH/32	_	CVRCON <cvrr> = 0</cvrr>
D316	DACACC	Absolute Accuracy <sup>(2)</sup>		_	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>
			—	_	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>

**Note 1:** Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

**2:** These parameters are characterized but not tested.

#### TABLE 30-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	nbol Characteristics		Typical	Max.	Units	Comments
D321	Cefc	External Filter Capacitor Value	8	10	_	μF	Capacitor must be low series resistance (1 ohm). Typical voltage on the VCAP pin is 1.8V.

#### TABLE 30-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics <sup>(1)</sup>			Min.	Max.	Units	Conditions	
TB10	ТтхН	TxCK High Time	Synchronous, with prescaler		[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8,
TB11	ΤτxL	TxCK Low Time	Synchronous, with ime prescaler		[(12.5 ns or 1 ТРВ)/N] + 25 ns	_	ns	Must also meet parameter TB15	16, 32, 64, 256)
TB15	B15 TTXP T		TxCK Synchronous, Input prescaler		[(Greater of [(25 ns or 2 Трв)/N] + 30 ns	_	ns	VDD > 2.7V	
		Period			[(Greater of [(25 ns or 2 Трв)/N] + 50 ns	_	ns	VDD < 2.7V	
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment			—	1	Трв	_	-

Note 1: These parameters are characterized, but not tested in manufacturing.

#### FIGURE 30-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



#### TABLE 30-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param. No.	Symbol	Characteristics <sup>(1)</sup>		Min.	Max.	Units	Conditions	
IC10	TCCL	ICx Input	t Low Time	[(12.5 ns or 1 ТРв)/N] + 25 ns	-	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	ТссН	ICx Input High Time		[(12.5 ns or 1 ТРВ)/N] + 25 ns	_	ns	Must also meet parameter IC15.	
IC15	TCCP	ICx Input Period		[(25 ns or 2 Трв)/N] + 50 ns	_	ns	_	

Note '	1:	These	parameters a	are charac	terized, bu	it not f	tested in	manufacturing	
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NOTES:

#### **Revision D (February 2012)**

All occurrences of VUSB were changed to: VUSB3V3. In addition, text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-3.

#### TABLE A-3: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 128	Corrected a part number error in all pin diagrams.
KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Updated the DMA Channels (Programmable/Dedicated) column in the PIC32MX1XX General Purpose Family Features (see Table 1).
1.0 "Device Overview"	Added the TQFP and VTLA packages to the 44-pin column heading and updated the pin numbers for the SCL1, SCL2, SDA1, and SDA2 pins in the Pinout I/O Descriptions (see Table 1-1).
7.0 "Interrupt Controller"	Updated the Note that follows the features.
	Updated the Interrupt Controller Block Diagram (see Figure 7-1).
29.0 "Electrical Characteristics"	Updated the Maximum values for parameters DC20-DC24, and the Minimum value for parameter DC21 in the Operating Current (IDD) DC Characteristics (see Table 29-5).
	Updated all Minimum and Maximum values for the Idle Current (IIDLE) DC Characteristics (see Table 29-6).
	Updated the Maximum values for parameters DC40k, DC40l, DC40n, and DC40m in the Power-down Current (IPD) DC Characteristics (see Table 29-7).
	Changed the minimum clock period for SCKx from 40 ns to 50 ns in Note 3 of the SPIx Master and Slave Mode Timing Requirements (see Table 29-26 through Table 29-29).
30.0 "DC and AC Device Characteristics Graphs"	Updated the Typical IIDLE Current @ VDD = 3.3V graph (see Figure 30-5).