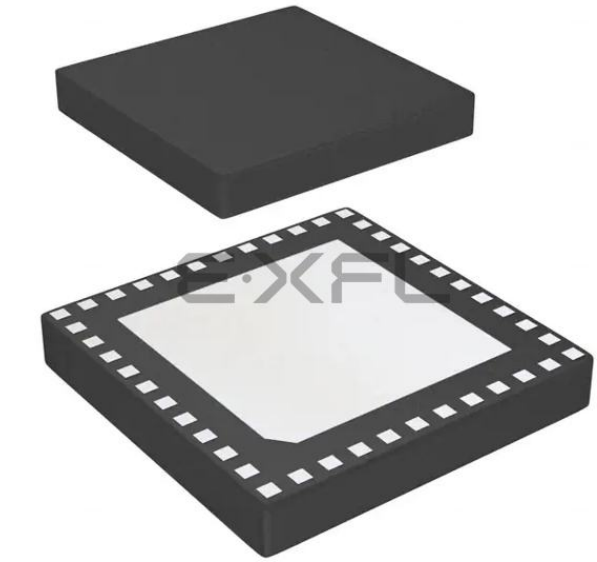

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 40MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 13x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VFTLA Exposed Pad |
| Supplier Device Package | 44-VTLA (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f064dt-v-tl |

**TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES**

**28-PIN QFN (TOP VIEW)(1,2,3,4)**

**PIC32MX210F016B**
**PIC32MX220F032B**
**PIC32MX230F064B**
**PIC32MX230F256B**
**PIC32MX250F128B**
**PIC32MX270F256B**

28 1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 | 15 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 | 16 | VSS |
| 3 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 | 17 | VCAP |
| 4 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 | 18 | PGED2/RPB10/D+/CTED11/RB10 |
| 5 | VSS | 19 | PGEC2/RPB11/D-/RB11 |
| 6 | OSC1/CLKI/RPA2/RA2 | 20 | VUSB3V3 |
| 7 | OSC2/CLKO/RPA3/PMA0/RA3 | 21 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 8 | SOSCI/RPB4/RB4 | 22 | CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14 |
| 9 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 23 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 10 | VDD | 24 | AVSS |
| 11 | TMS/RPB5/USBID/RB5 | 25 | AVDD |
| 12 | VBUS | 26 | $\overline{\text{MCLR}}$ |
| 13 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 27 | PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 |
| 14 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 28 | PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** Shaded pins are 5V tolerant.

## 3.0 CPU

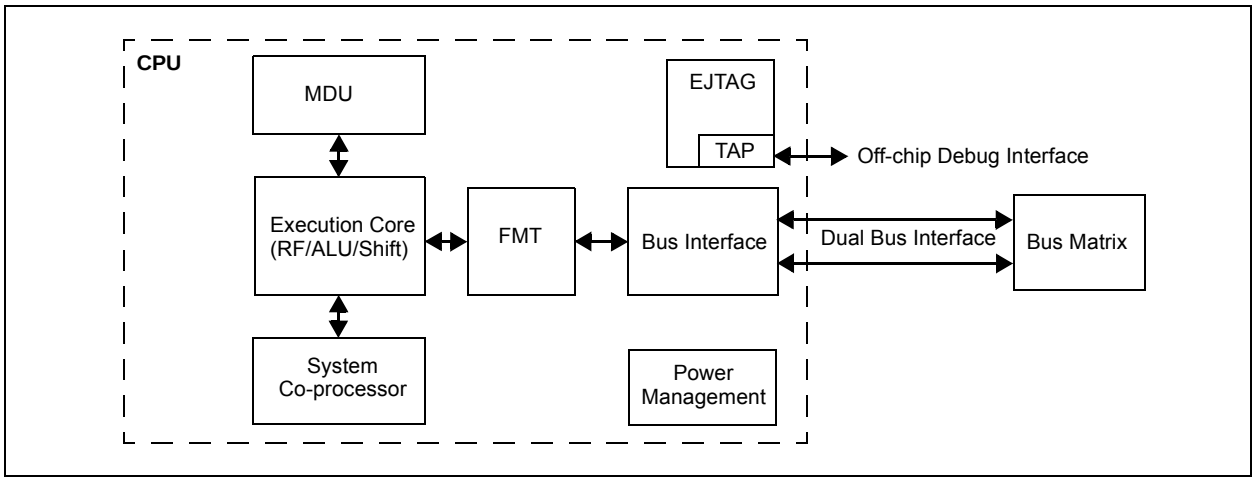
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS60001113), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). Resources for the MIPS32® M4K® Processor Core are available at: www.imgtec.com.

The MIPS32® M4K® Processor Core is the heart of the PIC32MX1XX/2XX family processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the destinations.

### 3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2)
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - Bit field manipulation instructions
- MIPS16e® code compression
  - 16-bit encoding of 32-bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - `SAVE` and `RESTORE` macro instructions for setting up and tearing down stack frames within subroutines
  - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- Simple dual bus interface
  - Independent 32-bit address and data buses
  - Transactions can be aborted to improve interrupt latency
- Autonomous multiply/divide unit
  - Maximum issue rate of one 32x16 multiply per clock
  - Maximum issue rate of one 32x32 multiply every other clock
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (*rs*) sign extension-dependent)
- Power control
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG debug and instruction trace
  - Support for single stepping
  - Virtual instruction and data address/value
  - Breakpoints

**FIGURE 3-1: MIPS32® M4K® PROCESSOR CORE BLOCK DIAGRAM**



## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

### 4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.

## 7.1 Interrupt Control Registers

**TABLE 7-2: INTERRUPT REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | FCEIF | RTCCIF | FSCMIF | AD1IF | OC5IF | IC5IF | IC5EIF | T5IF | INT4IF | OC4IF | IC4IF | IC4EIF | T4IF | INT3IF | OC3IF | IC3IF | 0000 |
| | | 15:0 | IC3EIF | T3IF | INT2IF | OC2IF | IC2IF | IC2EIF | T2IF | INT1IF | OC1IF | IC1IF | IC1EIF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | DMA3IF | DMA2IF | DMA1IF | DMA0IF | CTMUIF | I2C2MIF | I2C2SIF | I2C2BIF | U2TXIF | U2RXIF | U2EIF | SPI2TXIF | SPI2RXIF | SPI2EIF | PMPEIF | PMPIF | 0000 |
| | | 15:0 | CNCIF | CNBIF | CNAIF | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF | U1RXIF | U1EIF | SPI1TXIF | SPI1RXIF | SPI1EIF | USBIF(2) | CMP3IF | CMP2IF | CMP1IF | 0000 |
| 1060 | IEC0 | 31:16 | FCEIE | RTCCIE | FSCMIE | AD1IE | OC5IE | IC5IE | IC5EIE | T5IE | INT4IE | OC4IE | IC4IE | IC4EIE | T4IE | INT3IE | OC3IE | IC3IE | 0000 |
| | | 15:0 | IC3EIE | T3IE | INT2IE | OC2IE | IC2IE | IC2EIE | T2IE | INT1IE | OC1IE | IC1IE | IC1EIE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | DMA3IE | DMA2IE | DMA1IE | DMA0IE | CTMUIE | I2C2MIE | I2C2SIE | I2C2BIE | U2TXIE | U2RXIE | U2EIE | SPI2TXIE | SPI2RXIE | SPI2EIE | PMPEIE | PMPIE | 0000 |
| | | 15:0 | CNCIE | CNBIE | CNAIE | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE | U1RXIE | U1EIE | SPI1TXIE | SPI1RXIE | SPI1EIE | USBIE(2) | CMP3IE | CMP2IE | CMP1IE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX1XX devices.

**3:** This register does not have associated CLR, SET, INV registers.

**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)**

bit 9-8 **IS01<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP00<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS00<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

| **Note:** | This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions. |
|---|---|

**TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3170 | DCH1SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3180 | DCH1DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3190 | DCH1SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31A0 | DCH1DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31B0 | DCH1CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31C0 | DCH1CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31D0 | DCH1DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 31E0 | DCH2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 31F0 | DCH2ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 3200 | DCH2INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3210 | DCH2SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3220 | DCH2DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3230 | DCH2SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3240 | DCH2DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3250 | DCH2SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3260 | DCH2DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3270 | DCH2CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

**REGISTER 9-1: DMACON: DMA CONTROLLER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | — | SUSPEND | DMABUSY | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit(1)
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 9-5: DCRCDATA: DMA CRC DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return '0' on any read.

**REGISTER 9-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

**REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)**

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
- 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
- 0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
- 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
- 0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
- 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
- 0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
- 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
- 0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
- 1 = A channel address error has been detected (either the source or the destination address is invalid)
- 0 = No interrupt is pending

**NOTES:**

## 15.0 INPUT CAPTURE

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
  - Capture timer value on every rising and falling edge of input at ICx pin
  - Capture timer value on every edge (rising and falling)
  - Capture timer value on every edge (rising and falling), specified edge first.
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

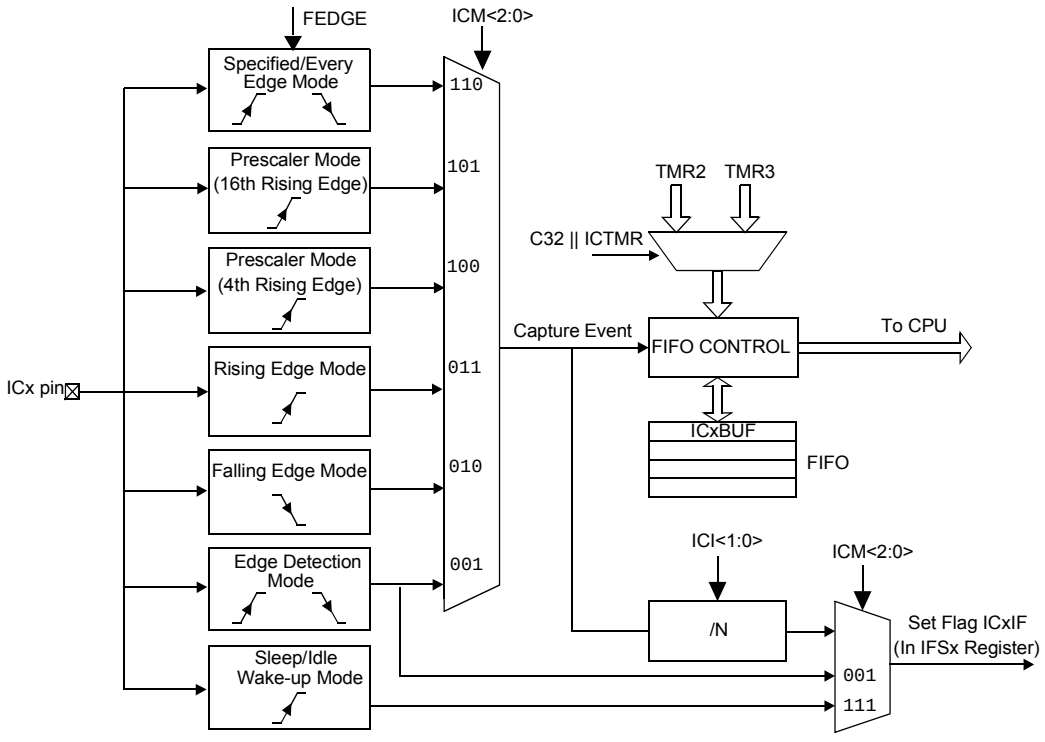
Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- Input capture can also be used to provide additional sources of external interrupts

Figure 15-1 illustrates a general block diagram of the Input Capture module.

**FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM**




**Note:** An 'x' in a signal, register or bit name denotes the number of the capture channel.

**REGISTER 18-2: I2CxSTAT: I$^2$C STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| 7:0 | R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |

| Legend: | HS = Set in hardware | HSC = Hardware set/cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | C = Clearable bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I$^2$C master, applicable to master transmit operation)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I$^2$C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I$^2$C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I$^2$C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

## 20.0 PARALLEL MASTER PORT (PMP)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

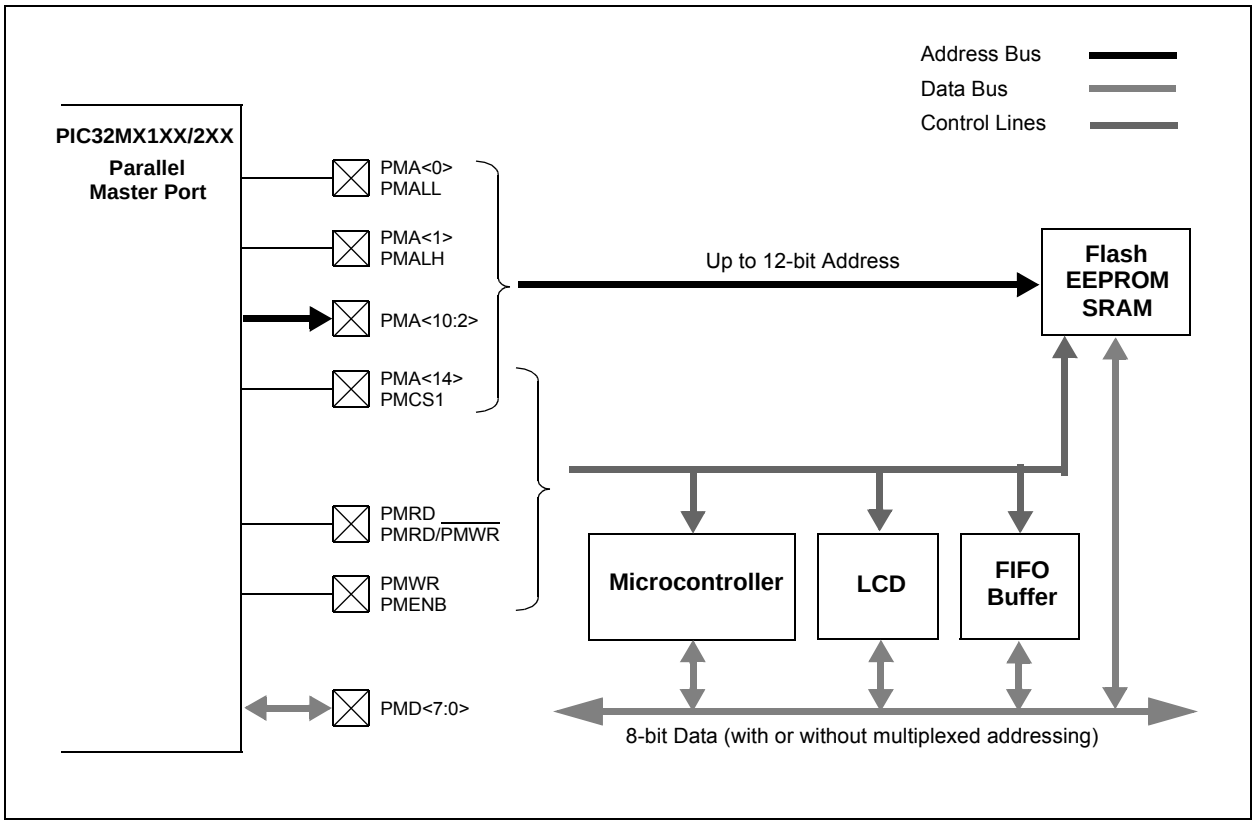
The PMP is a parallel 8-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- Fully multiplexed address/data mode
- Demultiplexed or partially multiplexed address/data mode
  - up to 11 address lines with single Chip Select
  - up to 12 address lines without Chip Select
- One Chip Select line
- Programmable strobe options
  - Individual read and write strobes or;
  - Read/$\overline{\text{write}}$ strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Legacy parallel slave port support
- Enhanced parallel slave support
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Selectable input voltage levels

Figure 20-1 illustrates the PMP module block diagram.

**FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES**



**REGISTER 27-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)**

bit 18-10 **PWP<8:0>:** Program Flash Write-Protect bits(3)

Prevents selected program Flash memory pages from being modified during code execution.
111111111 = Disabled
111111110 = Memory below 0x0400 address is write-protected
111111101 = Memory below 0x0800 address is write-protected
111111100 = Memory below 0x0C00 address is write-protected
111111011 = Memory below 0x1000 (4K) address is write-protected
111111010 = Memory below 0x1400 address is write-protected
111111001 = Memory below 0x1800 address is write-protected
111111000 = Memory below 0x1C00 address is write-protected
111110111 = Memory below 0x2000 (8K) address is write-protected
111110110 = Memory below 0x2400 address is write-protected
111110101 = Memory below 0x2800 address is write-protected
111110100 = Memory below 0x2C00 address is write-protected
111110011 = Memory below 0x3000 address is write-protected
111110010 = Memory below 0x3400 address is write-protected
111110001 = Memory below 0x3800 address is write-protected
111110000 = Memory below 0x3C00 address is write-protected
111101111 = Memory below 0x4000 (16K) address is write-protected
.
.
.
110111111 = Memory below 0x10000 (64K) address is write-protected
.
.
.
101111111 = Memory below 0x20000 (128K) address is write-protected
.
.
.
011111111 = Memory below 0x40000 (256K) address is write-protected
.
.
.
000000000 = All possible memory is write-protected

bit 9-5 **Reserved:** Write '1'

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits(2)

11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = PGEC4/PGED4 pair is used(2)

bit 2 **JTAGEN:** JTAG Enable bit(1)

1 = JTAG is enabled
0 = JTAG is disabled

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)

1x = Debugger is disabled
0x = Debugger is enabled

**Note 1:** This bit sets the value for the JTAGEN bit in the CFGCON register.

**2:** The PGEC4/PGED4 pin pair is not available on all devices. Refer to the **"Pin Diagrams"** section for availability.

**3:** The PWP<8:7> bits are only available on devices with 256 KB Flash.

**TABLE 30-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **Parameter No.** | **Typical(3)** | **Max.** | **Units** | **Conditions** | |
| **Operating Current (IDD) (Notes 1, 2, 5)** | | | | | |
| DC20 | 2 | 3 | mA | 4 MHz **(Note 4)** | |
| DC21 | 7 | 10.5 | mA | 10 MHz | |
| DC22 | 10 | 15 | mA | 20 MHz **(Note 4)** | |
| DC23 | 15 | 23 | mA | 30 MHz **(Note 4)** | |
| DC24 | 20 | 30 | mA | 40 MHz | |
| DC25 | 100 | 150 | µA | +25ºC, 3.3V | LPRC (31 kHz) **(Note 4)** |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** This parameter is characterized, but not tested in manufacturing.

**5:** IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

**TABLE 30-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| DO10 | VOL | **Output Low Voltage**<br>I/O Pins | — | — | 0.4 | V | IOL ≤ 10 mA, VDD = 3.3V |
| DO20 | VOH | **Output High Voltage**<br>I/O Pins | 1.5(1) | — | — | V | IOH ≥ -14 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -12 mA, VDD = 3.3V |
| | | | 2.4 | — | — | | IOH ≥ -10 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -7 mA, VDD = 3.3V |

**Note 1:** Parameters are characterized, but not tested.

**TABLE 30-11: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.(1)** | **Typical** | **Max.** | **Units** | **Conditions** |
| BO10 | VBOR | BOR Event on VDD transition high-to-low(2) | 2.0 | — | 2.3 | V | — |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

**TABLE 30-12: DC CHARACTERISTICS: PROGRAM MEMORY**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | | **Program Flash Memory(3)** | | | | | |
| D130 | EP | Cell Endurance | 20,000 | — | — | E/W | — |
| D131 | VPR | VDD for Read | 2.3 | — | 3.6 | V | — |
| D132 | VPEW | VDD for Erase or Write | 2.3 | — | 3.6 | V | — |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | Provided no other specifications are violated |
| D135 | IDDP | Supply Current during Programming | — | 10 | — | mA | — |
| | TWW | Word Write Cycle Time | — | 411 | — | FRC Cycles | See **Note 4** |
| D136 | TRW | Row Write Cycle Time | — | 6675 | — | | See **Note 2,4** |
| D137 | TPE | Page Erase Cycle Time | — | 20011 | — | | See **Note 4** |
| | TCE | Chip Erase Cycle Time | — | 80180 | — | | See **Note 4** |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

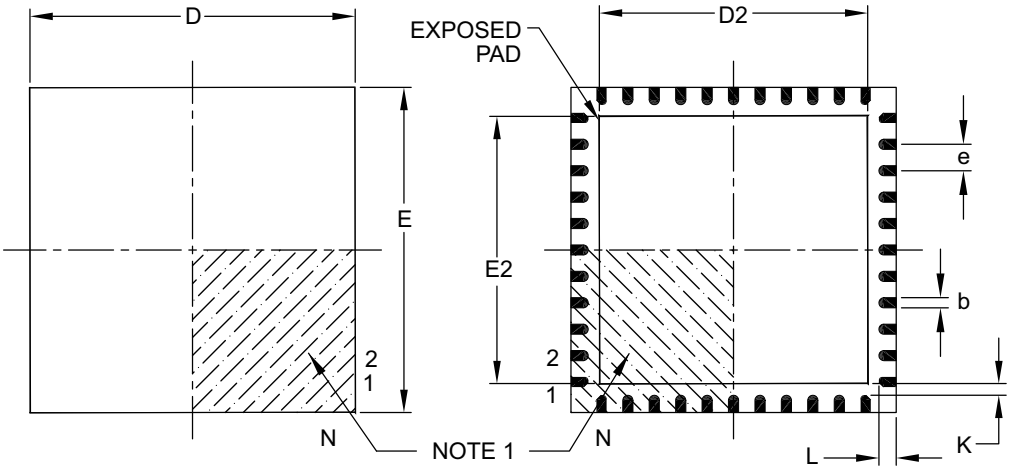
**2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

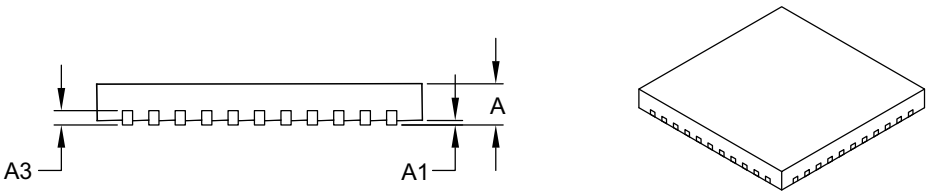
**4:** This parameter depends on FRC accuracy (See Table 30-19) and FRC tuning values (See Register 8-2).

### 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW** **BOTTOM VIEW**




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 44 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 8.00 BSC | |
| Exposed Pad Width | E2 | 6.30 | 6.45 | 6.80 |
| Overall Length | D | | 8.00 BSC | |
| Exposed Pad Length | D2 | 6.30 | 6.45 | 6.80 |
| Contact Width | b | 0.25 | 0.30 | 0.38 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

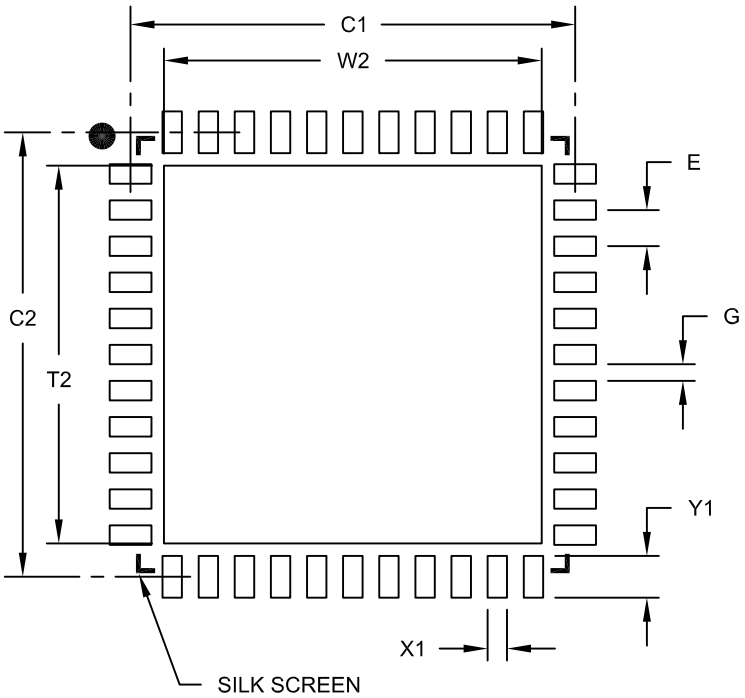
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

### 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 6.80 |
| Optional Center Pad Length | T2 | | | 6.80 |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Width (X44) | X1 | | | 0.35 |
| Contact Pad Length (X44) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

# APPENDIX A: REVISION HISTORY

## Revision A (May 2011)

This is the initial released version of this document.

## Revision B (October 2011)

The following two global changes are included in this revision:

- All packaging references to VLAP have been changed to VTLA throughout the document
- All references to VCORE have been removed
- All occurrences of the ASCL1, ASCL2, ASDA1, and ASDA2 pins have been removed
- V-temp temperature range (-40ºC to +105ºC) was added to all electrical specification tables

This revision includes the addition of the following devices:

- PIC32MX130F064B
- PIC32MX130F064C
- PIC32MX130F064D
- PIC32MX150F128B
- PIC32MX150F128C
- PIC32MX150F128D
- PIC32MX230F064B
- PIC32MX230F064C
- PIC32MX230F064D
- PIC32MX250F128B
- PIC32MX250F128C
- PIC32MX250F128D

Text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-1.

**TABLE A-1: MAJOR SECTION UPDATES**

| Section | Update Description |
|---|---|
| **"**32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog**"** | Split the existing Features table into two: PIC32MX1XX General Purpose Family Features (Table 1) and PIC32MX2XX USB Family Features (Table 2).<br>Added the SPDIP package reference (see Table 1, Table 2, and **"Pin Diagrams"**).<br>Added the new devices to the applicable pin diagrams.<br>Changed PGED2 to PGED1 on pin 35 of the 36-pin VTLA diagram for PIC32MX220F032C, PIC32MX220F016C, PIC32MX230F064C, and PIC32MX250F128C devices. |
| **1.0 "Device Overview"** | Added the SPDIP package reference and updated the pin number for AN12 for 44-pin QFN devices in the Pinout I/O Descriptions (see Table 1-1).<br>Added the PGEC4/PGED4 pin pair and updated the C1INA-C1IND and C2INA-C2IND pin numbers for 28-pin SSOP/SPDIP/SOIC devices in the Pinout I/O Descriptions (see Table 1-1). |
| **2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"** | Updated the Recommended Minimum Connection diagram (see Figure 2-1). |