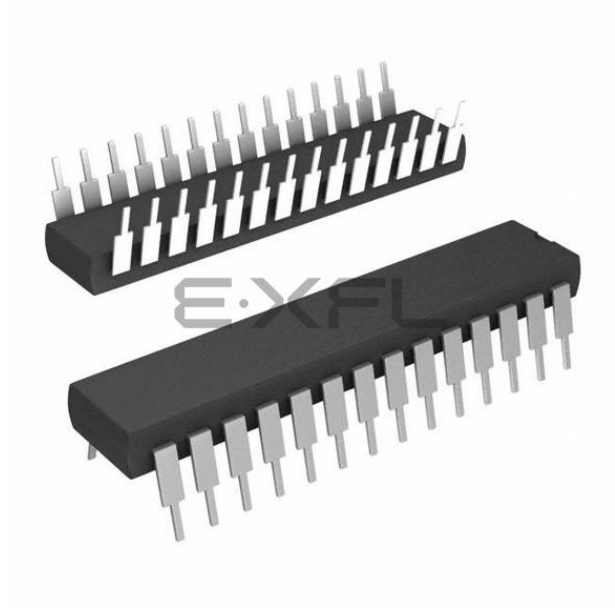
Microchip Technology - PIC32MX230F256B-I/SP Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256b-i-sp

TABLE 2: PIC32MX2XX 28/36/44-PIN USB FAMILY FEATURES

Device	Pins	Program Memory (KB)(1)	Data Memory (KB)	Remappable Peripherals					Analog Comparators	USB On-The-Go (OTG)	I^2C	PMP	DMA Channels (Programmable/Dedicated)	CTMU	10-bit 1 Msps ADC (Channels)	RTCC	I/O Pins	JTAG	Packages
				Remappable Pins	Timers(2)/Capture/Compare	UART	SPI/I^2S	External Interrupts(3)											
PIC32MX210F016B	28	16+3	4	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX210F016C	36	16+3	4	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	25	Y	VTLA
PIC32MX210F016D	44	16+3	4	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX220F032B	28	32+3	8	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX220F032C	36	32+3	8	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX220F032D	44	32+3	8	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX230F064B	28	64+3	16	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX230F064C	36	64+3	16	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX230F064D	44	64+3	16	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX250F128B	28	128+3	32	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX250F128C	36	128+3	32	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX250F128D	44	128+3	32	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX230F256B	28	256+3	16	20	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX230F256D	44	256+3	16	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX270F256B	28	256+3	64	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX270F256D	44	256+3	64	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX270F256DB(4)	44	256+3	64	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN

Note 1: This device features 3 KB of boot Flash memory.

2: Four out of five timers are remappable.

3: Four out of five external interrupts are remappable.

4: This PIC32 device is targeted to specific audio software packages that are tracked for licensing royalty purposes. All peripherals and electrical characteristics are identical to their corresponding base part numbers.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
AN0	27	2	33	19	I	Analog	Analog input channels.
AN1	28	3	34	20	I	Analog	
AN2	1	4	35	21	I	Analog	
AN3	2	5	36	22	I	Analog	
AN4	3	6	1	23	I	Analog	
AN5	4	7	2	24	I	Analog	
AN6	—	—	3	25	I	Analog	
AN7	—	—	4	26	I	Analog	
AN8	—	—	—	27	I	Analog	
AN9	23	26	29	15	I	Analog	
AN10	22	25	28	14	I	Analog	
AN11	21	24	27	11	I	Analog	
AN12	20(2)	23(2)	26(2) 11(3)	10(2) 36(3)	I	Analog	
CLKI	6	9	7	30	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	7	10	8	31	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	6	9	7	30	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	7	10	8	31	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	8	11	9	33	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	9	12	10	34	O	—	32.768 kHz low-power oscillator crystal output.
REFCLKI	PPS	PPS	PPS	PPS	I	ST	Reference Input Clock
REFCLKO	PPS	PPS	PPS	PPS	O	—	Reference Output Clock
IC1	PPS	PPS	PPS	PPS	I	ST	Capture Inputs 1-5
IC2	PPS	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
SDA1	15	18	19	1	I/O	ST	Synchronous serial data input/output for I2C1
SCL2	4	7	2	24	I/O	ST	Synchronous serial clock input/output for I2C2
SDA2	3	6	1	23	I/O	ST	Synchronous serial data input/output for I2C2
TMS	19[2] 11[3]	22[2] 14[3]	25[2] 15[3]	12	I	ST	JTAG Test mode select pin
TCK	14	17	18	13	I	ST	JTAG test clock input pin
TDI	13	16	17	35	O	—	JTAG test data input pin
TDO	15	18	19	32	O	—	JTAG test data output pin
RTCC	4	7	2	24	O	ST	Real-Time Clock alarm output
CVREF-	28	3	34	20	I	Analog	Comparator Voltage Reference (low)
CVREF+	27	2	33	19	I	Analog	Comparator Voltage Reference (high)
CVREFOUT	22	25	28	14	O	Analog	Comparator Voltage Reference output
C1INA	4	7	2	24	I	Analog	Comparator Inputs
C1INB	3	6	1	23	I	Analog	
C1INC	2	5	36	22	I	Analog	
C1IND	1	4	35	21	I	Analog	
C2INA	2	5	36	22	I	Analog	
C2INB	1	4	35	21	I	Analog	
C2INC	4	7	2	24	I	Analog	
C2IND	3	6	1	23	I	Analog	
C3INA	23	26	29	15	I	Analog	
C3INB	22	25	28	14	I	Analog	
C3INC	27	2	33	19	I	Analog	
C3IND	1	4	35	21	I	Analog	
C1OUT	PPS	PPS	PPS	PPS	O	—	Comparator Outputs
C2OUT	PPS	PPS	PPS	PPS	O	—	
C3OUT	PPS	PPS	PPS	PPS	O	—	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		—	—	27	O	—	Parallel Master Port address (Demultiplexed Master modes)
PMA3		—	—	38	O	—	
PMA4		—	—	37	O	—	
PMA5		—	—	4	O	—	
PMA6		—	—	5	O	—	
PMA7		—	—	13	O	—	
PMA8		—	—	32	O	—	
PMA9		—	—	35	O	—	
PMA10		—	—	12	O	—	
PMCS1	23	26	29	15	O	—	Parallel Master Port Chip Select 1 strobe
PMD0	20(2)	23(2)	26(2)	10(2)	I/O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes)
	1(3)	4(3)	35(3)	21(3)			
PMD1	19(2)	22(2)	25(2)	9(2)	I/O	TTL/ST	
	2(3)	5(3)	36(3)	22(3)			
PMD2	18(2)	21(2)	24(2)	8(2)	I/O	TTL/ST	
	3(3)	6(3)	1(3)	23(3)			
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12(2)	15(2)	16(2)	42(2)	I/O	TTL/ST	
	28(3)	3(3)	34(3)	20(3)			
PMD7	11(2)	14(2)	15(2)	41(2)	I/O	TTL/ST	
	27(3)	2(3)	33(3)	19(3)			
PMRD	21	24	27	11	O	—	Parallel Master Port read strobe
PMWR	22(2)	25(2)	28(2)	14(2)	O	—	Parallel Master Port write strobe
	4(3)	7(3)	2(3)	24(3)			
VBUS	12(3)	15(3)	16(3)	42(3)	I	Analog	USB bus power monitor
VUSB3V3	20(3)	23(3)	26(3)	10(3)	P	—	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22(3)	25(3)	28(3)	14(3)	O	—	USB Host and OTG bus power control output
D+	18(3)	21(3)	24(3)	8(3)	I/O	Analog	USB D+
D-	19(3)	22(3)	25(3)	9(3)	I/O	Analog	USB D-

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

REGISTER 9-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	RDWR	DMACH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **RDWR:** Read/Write Status bit
1 = Last DMA bus access was a read
0 = Last DMA bus access was a write

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel.

REGISTER 9-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access.

REGISTER 9-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow a "terminate on match".

All other modes:
Unused.

REGISTER 10-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

REGISTER 10-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit
When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit
1 = External clock from TxCKI pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 4 **Unimplemented:** Read as '0'

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	MONTH10	MONTH01<3:0>			
15:8	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	DAY10<1:0>		DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	—	—	—	—	—	WDAY01<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MONTH10:** Binary Coded Decimal value of months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAY10<1:0>:** Binary Coded Decimal value of days bits, 10s place digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY01<2:0>:** Binary Coded Decimal value of weekdays bits; contains a value from 0 to 6

22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

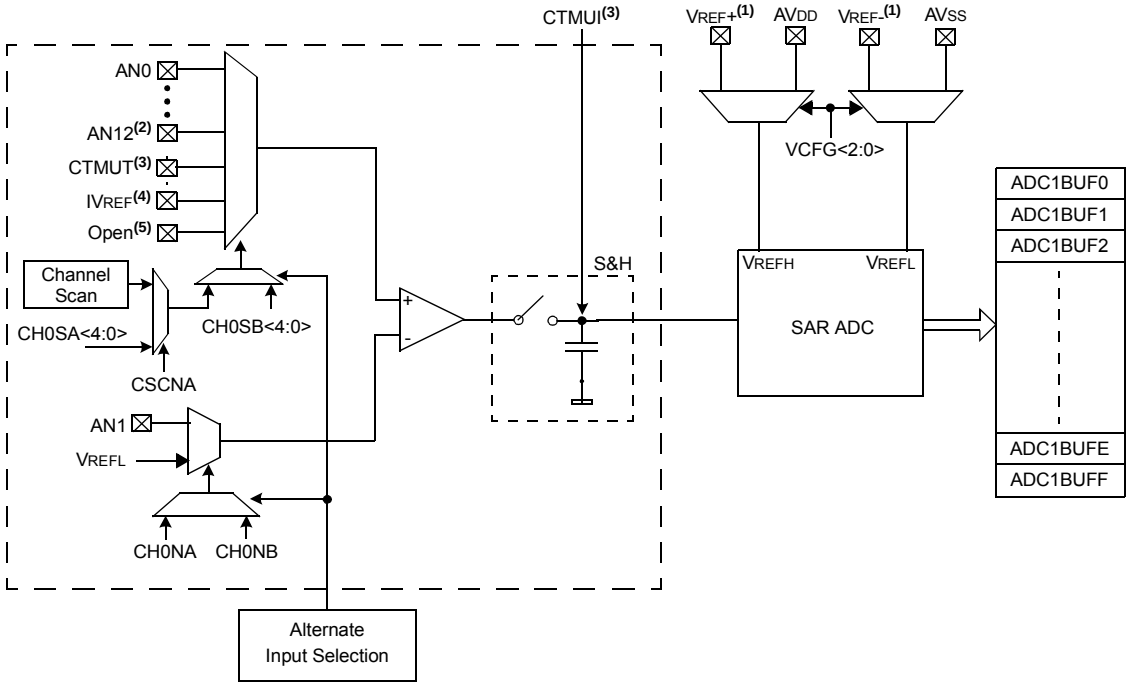
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 13 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. Figure 22-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM



Note 1: VREF+ and VREF- inputs can be multiplexed with other analog inputs.

2: AN8 is only available on 44-pin devices. AN6, AN7, and AN12 are not available on 28-pin devices.

3: Connected to the CTMU module. See **Section 25.0 "Charge Time Measurement Unit (CTMU)"** for more information.

4: Internal precision voltage reference (1.2V).

5: This selection is only used with CTMU capacitive and time measurement.

TABLE 22-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9120	ADC1BUFB	31:16	ADC Result Word B (ADC1BUFB<31:0>)																0000
		15:0																	0000
9130	ADC1BUFC	31:16	ADC Result Word C (ADC1BUFC<31:0>)																0000
		15:0																	0000
9140	ADC1BUFD	31:16	ADC Result Word D (ADC1BUFD<31:0>)																0000
		15:0																	0000
9150	ADC1BUFE	31:16	ADC Result Word E (ADC1BUFE<31:0>)																0000
		15:0																	0000
9160	ADC1BUFF	31:16	ADC Result Word F (ADC1BUFF<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for details.

NOTES:

TABLE 26-2: PERIPHERAL MODULE DISABLE REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F240	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CVRMD	—	—	—	CTMUMD	—	—	—	—	—	—	—	AD1MD	0000
F250	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD	0000
F260	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
F270	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	T5MD	T4MD	T3MD	T2MD	T1MD	0000
F280	PMD5	31:16	—	—	—	—	—	—	—	USB1MD	—	—	—	—	—	—	I2C1MD	I2C1MD	0000
		15:0	—	—	—	—	—	—	SPI2MD	SPI1MD	—	—	—	—	—	—	U2MD	U1MD	0000
F290	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PMPMD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	RTCCMD	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

REGISTER 27-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	—	—	—	—	—	FPLLODIV<2:0>		
15:8	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	UPLLEN(1)	—	—	—	—	UPLLIDIV<2:0>(1)		
7:0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
	—	FPLLMUL<2:0>			—	FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** Default PLL Output Divisor bits
- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit(1)
- 1 = Disable and bypass USB PLL
- 0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLIDIV<2:0>:** USB PLL Input Divider bits(1)
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits
- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

Note 1: This bit is only available on PIC32MX2XX devices.

TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O Pins with PMP	VSS	—	0.15 VDD	V	
		I/O Pins	VSS	—	0.2 VDD	V	
DI18		SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	VSS	—	0.8	V	SMBus enabled **(Note 4)**
	VIH	**Input High Voltage**					
DI20		I/O Pins not 5V-tolerant(5)	0.65 VDD	—	VDD	V	**(Note 4,6)**
		I/O Pins 5V-tolerant with PMP(5)	0.25 VDD + 0.8V	—	5.5	V	**(Note 4,6)**
		I/O Pins 5V-tolerant(5)	0.65 VDD	—	5.5	V	
DI28		SDAx, SCLx	0.65 VDD	—	5.5	V	SMBus disabled **(Note 4,6)**
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)**
DI30	ICNPU	**Change Notification Pull-up Current**	—	—	-50	µA	VDD = 3.3V, VPIN = VSS **(Note 3,6)**
DI31	ICNPD	**Change Notification Pull-down Current(4)**	—	—	-50	µA	VDD = 3.3V, VPIN = VDD
	IIL	**Input Leakage Current (Note 3)**					
DI50		I/O Ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{\text{MCLR}}$(2)	—	—	±1	µA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the **"Pin Diagrams"** section for the 5V-tolerant pins.

6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

TABLE 30-13: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±7.5	±25	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS **(Note 2)**
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max VICM = (VDD - 1)V **(Note 2)**
D303A	TRESP	Large Signal Response Time	—	150	400	ns	AVDD = VDD, AVSS = VSS **(Note 1,2)**
D303B	TSRESP	Small Signal Response Time	—	1	—	μs	This is defined as an input step of 50 mV with 15 mV of overdrive **(Note 2)**
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	μs	Comparator module is configured before setting the comparator ON bit **(Note 2)**
D305	IVREF	Internal Voltage Reference	1.14	1.2	1.26	V	—
D312	TSET	Internal Comparator Voltage DRC Reference Setting time	—	—	10	μs	**(Note 3)**

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

2: These parameters are characterized but not tested.

3: Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

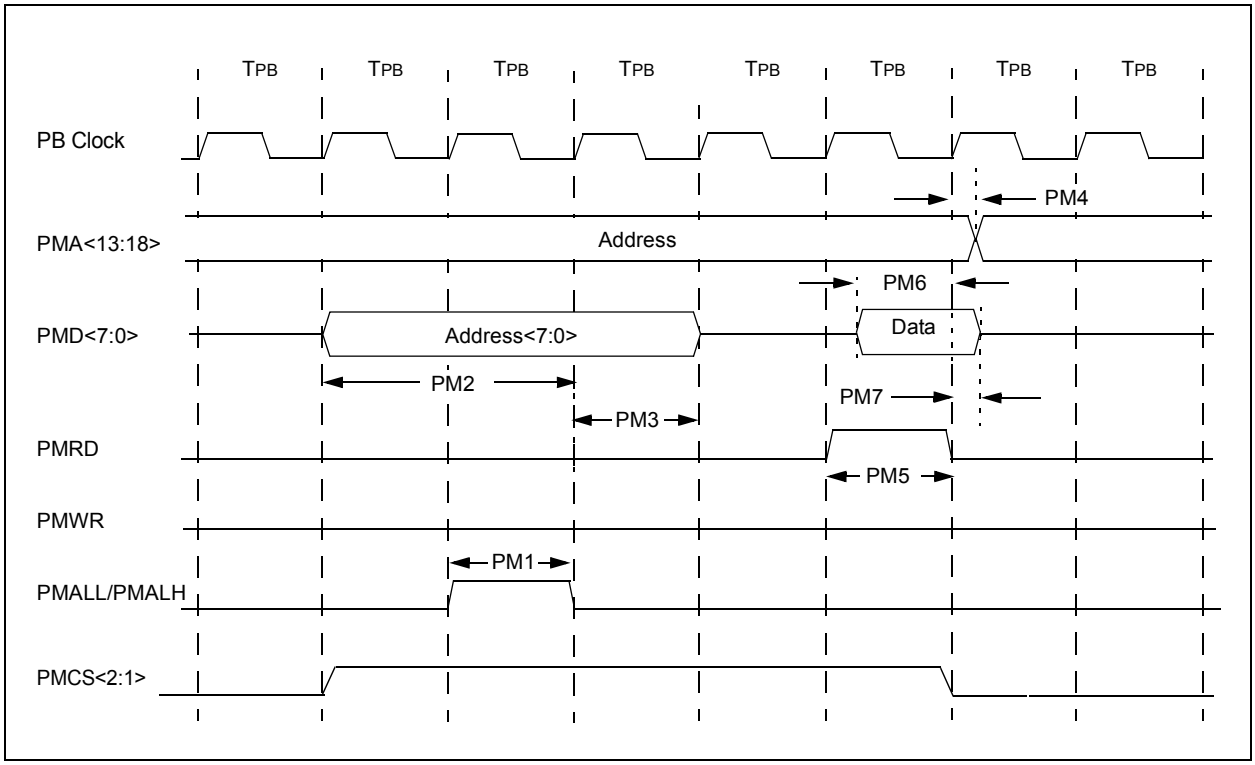
4: The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 30-37: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param.No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtI	$\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid	—	—	60	ns	—
PS4	TrdH2dtI	$\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{CS}$ Active Time	TPB + 40	—	—	ns	—
PS6	TWR	$\overline{WR}$ Active Time	TPB + 25	—	—	ns	—
PS7	TRD	$\overline{RD}$ Active Time	TPB + 25	—	—	ns	—

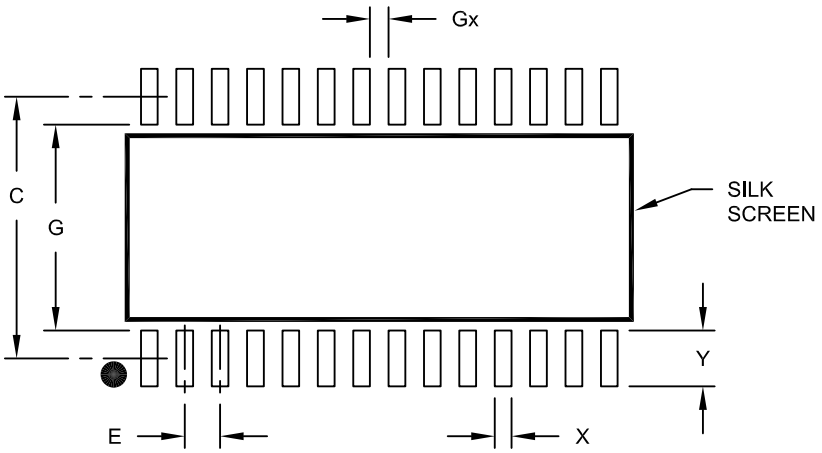
Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 30-21: PARALLEL MASTER PORT READ TIMING DIAGRAM



28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

Revision D (February 2012)

All occurrences of VUSB were changed to: VUSB3V3. In addition, text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-3: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog**"**	Corrected a part number error in all pin diagrams. Updated the DMA Channels (Programmable/Dedicated) column in the PIC32MX1XX General Purpose Family Features (see Table 1).
1.0 "Device Overview"	Added the TQFP and VTLA packages to the 44-pin column heading and updated the pin numbers for the SCL1, SCL2, SDA1, and SDA2 pins in the Pinout I/O Descriptions (see Table 1-1).
7.0 "Interrupt Controller"	Updated the Note that follows the features. Updated the Interrupt Controller Block Diagram (see Figure 7-1).
29.0 "Electrical Characteristics"	Updated the Maximum values for parameters DC20-DC24, and the Minimum value for parameter DC21 in the Operating Current (IDD) DC Characteristics (see Table 29-5). Updated all Minimum and Maximum values for the Idle Current (IIDLE) DC Characteristics (see Table 29-6). Updated the Maximum values for parameters DC40k, DC40l, DC40n, and DC40m in the Power-down Current (IPD) DC Characteristics (see Table 29-7). Changed the minimum clock period for SCKx from 40 ns to 50 ns in Note 3 of the SPIx Master and Slave Mode Timing Requirements (see Table 29-26 through Table 29-29).
30.0 "DC and AC Device Characteristics Graphs"	Updated the Typical IIDLE Current @ VDD = 3.3V graph (see Figure 30-5).