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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256b-i-ss

TABLE 7: PIN NAMES FOR 36-PIN GENERAL PURPOSE DEVICES

36-PIN VTLA (TOP VIEW)(1,2,3,5)

PIC32MX110F016C
PIC32MX120F032C
PIC32MX130F064C
PIC32MX150F128C

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1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	19	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	20	RPC9/CTED7/RC9
3	PGED4(4)/AN6/RPC0/RC0	21	VSS
4	PGEC4(4)/AN7/RPC1/RC1	22	VCAP
5	VDD	23	VDD
6	VSS	24	PGED2/RPB10/CTED11/PMD2/RB10
7	OSC1/CLKI/RPA2/RA2	25	PGEC2/TMS/RPB11/PMD1/RB11
8	OSC2/CLKO/RPA3/PMA0/RA3	26	AN12/PMD0/RB12
9	SOSCI/RPB4/RB4	27	AN11/RPB13/CTPLS/PMRD/RB13
10	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	28	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
11	RPC3/RC3	29	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
12	VSS	30	AVSS
13	VDD	31	AVDD
14	VDD	32	$\overline{\text{MCLR}}$
15	PGED3/RPB5/PMD7/RB5	33	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0
16	PGEC3/RPB6/PMD6/RB6	34	VREF-/CVREF-/AN1/RPA1/CTED2/RA1
17	TDI/RPB7/CTED3/PMD5/INT0/RB7	35	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0
18	TCK/RPB8/SCL1/CTED10/PMD4/RB8	36	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.
2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.
3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
4: This pin function is not available on PIC32MX110F016C and PIC32MX120F032C devices.
5: Shaded pins are 5V tolerant.

TABLE 11: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

44-PIN TQFP (TOP VIEW)(1,2,3,5)

PIC32MX110F016D
PIC32MX120F032D
PIC32MX130F064D
PIC32MX130F256D
PIC32MX150F128D
PIC32MX170F256D

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Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	VSS	28	VDD
7	VCAP	29	VSS
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4(4)/TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4(4)/TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVSS	38	RPC5/PMA3/RC5
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

5: Shaded pins are 5V tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
USBID	11[3]	14[3]	15[3]	41[3]	I	ST	USB OTG ID detect
CTED1	27	2	33	19	I	ST	CTMU External Edge Input
CTED2	28	3	34	20	I	ST	
CTED3	13	16	17	43	I	ST	
CTED4	15	18	19	1	I	ST	
CTED5	22	25	28	14	I	ST	
CTED6	23	26	29	15	I	ST	
CTED7	—	—	20	5	I	ST	
CTED8	—	—	—	13	I	ST	
CTED9	9	12	10	34	I	ST	
CTED10	14	17	18	44	I	ST	
CTED11	18	21	24	8	I	ST	
CTED12	2	5	36	22	I	ST	
CTED13	3	6	1	23	I	ST	
CTPLS	21	24	27	11	O	—	CTMU Pulse Output
PGED1	1	4	35	21	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	2	5	36	22	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	18	21	24	8	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	19	22	25	9	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
PGED3	11[2]	14[2]	15[2]	41[2]	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3
	27[3]	2[3]	33[3]	19[3]			
PGEC3	12[2]	15[2]	16[2]	42[2]	I	ST	Clock input pin for Programming/ Debugging Communication Channel 3
	28[3]	3[3]	34[3]	20[3]			
PGED4	—	—	3	12	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 4
PGEC4	—	—	4	13	I	ST	Clock input pin for Programming/ Debugging Communication Channel 4

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

REGISTER 10-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE(1) / EOFEE(2)	PIDEE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

Note 1: Device mode.
2: Host mode.

Note: For an interrupt to propagate the USBIF register, the UERRIE (U1IE<1>) bit must be set.

REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Reset all Even/Odd buffer pointers to the EVEN Buffer Descriptor banks
0 = Even/Odd buffer pointers are not Reset

bit 0 **USBEN:** USB Module Enable bit(4)
1 = USB module and supporting circuitry is enabled
0 = USB module and supporting circuitry is disabled

SOFEN: SOF Enable bit(5)
1 = SOF token is sent every 1 ms
0 = SOF token is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).

2: All host control logic is reset any time that the value of this bit is toggled.

3: Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.

4: Device mode.

5: Host mode.

REGISTER 10-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit
1 = Next token command to be executed at Low-Speed
0 = Next token command to be executed at Full-Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 10-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FB8C	RPC8R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC8<3:0>				0000
FB90	RPC9R(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC9<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is only available on 44-pin devices.
2: This register is only available on PIC32MX1XX devices.
3: This register is only available on 36-pin and 44-pin devices.

REGISTER 14-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON(1,2)	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	—	SWDTPS<4:0>					WDTWINEN	WDTCLR

Legend:	y = Values set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit(1,2)
- 1 = Enables the WDT if it is not enabled by the device configuration
- 0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit
- 1 = Enable windowed Watchdog Timer
- 0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit
- 1 = Writing a '1' will clear the WDT
- 0 = Software cannot force this bit to a '0'

Note 1: A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.

2: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Set in hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR:** SPI Frame Error status bit
1 = Frame error detected
0 = No Frame error detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.

bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved; do not use
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

22.1 ADC Control Registers

TABLE 22-1: ADC REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	AD1CON1(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE	0000
9010	AD1CON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG<2:0>			OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000
9020	AD1CON3(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>								0000
9040	AD1CHS(1)	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9050	AD1CSSL(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16	ADC Result Word 0 (ADC1BUF0<31:0>)																0000
		15:0																	0000
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)																0000
		15:0																	0000
9090	ADC1BUF2	31:16	ADC Result Word 2 (ADC1BUF2<31:0>)																0000
		15:0																	0000
90A0	ADC1BUF3	31:16	ADC Result Word 3 (ADC1BUF3<31:0>)																0000
		15:0																	0000
90B0	ADC1BUF4	31:16	ADC Result Word 4 (ADC1BUF4<31:0>)																0000
		15:0																	0000
90C0	ADC1BUF5	31:16	ADC Result Word 5 (ADC1BUF5<31:0>)																0000
		15:0																	0000
90D0	ADC1BUF6	31:16	ADC Result Word 6 (ADC1BUF6<31:0>)																0000
		15:0																	0000
90E0	ADC1BUF7	31:16	ADC Result Word 7 (ADC1BUF7<31:0>)																0000
		15:0																	0000
90F0	ADC1BUF8	31:16	ADC Result Word 8 (ADC1BUF8<31:0>)																0000
		15:0																	0000
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)																0000
		15:0																	0000
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for details.

25.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

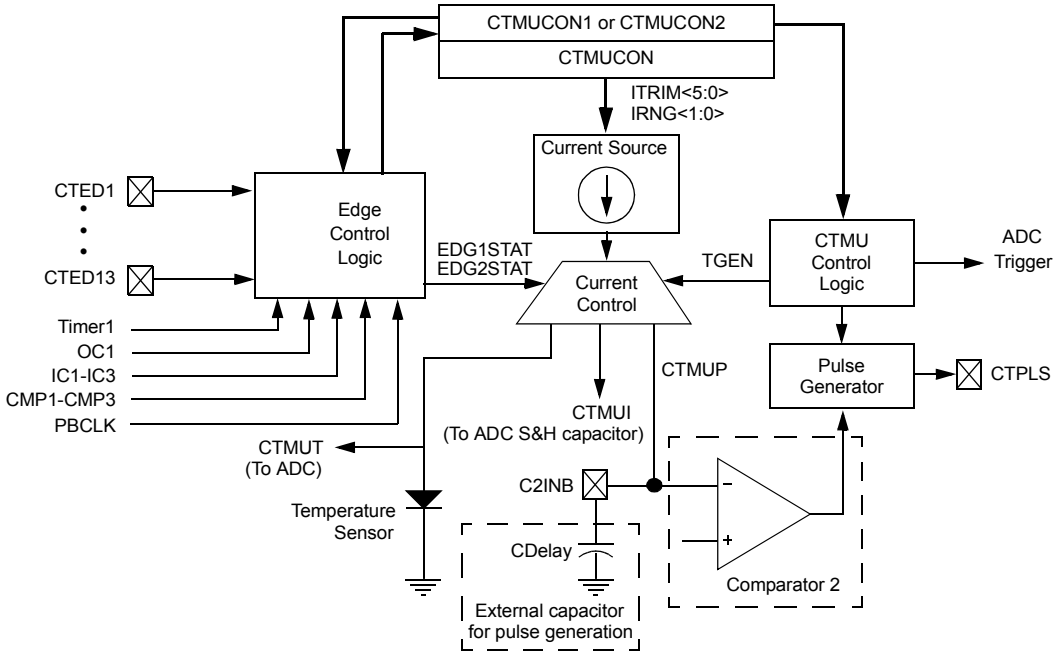
The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Up to 13 channels available for capacitive or time measurement input
- On-chip precision current source
- 16-edge input trigger sources
- Selection of edge or level-sensitive inputs
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- Control of current source during auto-sampling
- Four current source ranges
- Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 25-1.

FIGURE 25-1: CTMU BLOCK DIAGRAM



Current Control Selection	TGEN	EDG1STAT, EDG2STAT
CTMUT	0	EDG1STAT = EDG2STAT
CTMUI	0	EDG1STAT ≠ EDG2STAT
CTMUP	1	EDG1STAT ≠ EDG2STAT
No Connect	1	EDG1STAT = EDG2STAT

26.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX1XX/2XX 28/36/44-pin Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

26.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- SOSC Run mode: the CPU is clocked from the SOSC clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

26.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- POSC Idle mode: the system clock is derived from the POSC. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- SOSC Idle mode: the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

26.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

26.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See **Section 26.3.3 "Peripheral Bus Scaling Method"** for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

REGISTER 27-5: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	—	—	IOLOCK(1)	PMDLOCK(1)	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-1	R/W-1
	—	—	—	—	JTAGEN	—	—	TDOEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit(1)
- 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
- 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.

bit 12 **PMDLOCK:** Peripheral Module Disable bit(1)
- 1 = Peripheral module is locked. Writes to PMD registers is not allowed.
- 0 = Peripheral module is not locked. Writes to PMD registers is allowed.

bit 11-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Port Enable bit
- 1 = Enable the JTAG port
- 0 = Disable the JTAG port

bit 2-1 **Unimplemented:** Read as '1'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG bit
- 1 = 2-wire JTAG protocol uses TDO
- 0 = 2-wire JTAG protocol does not use TDO

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

TABLE 30-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp		
Param. No.	**Typical(2)**	**Max.**	**Units**	**Conditions**	
Power-Down Current (I_{PD}) (Notes 1, 5)					
DC40k	44	70	μA	-40°C	Base Power-Down Current
DC40l	44	70	μA	+25°C	
DC40n	168	259	μA	+85°C	
DC40m	335	536	μA	+105ºC	
Module Differential Current					
DC41e	5	20	μA	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
DC42e	23	50	μA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
DC43d	1000	1100	μA	3.6V	ADC: ΔI_{ADC} **(Notes 3,4)**

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

5: I_{PD} electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

TABLE 30-34: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	AVDD	V	**(Note 1)**
Reference Inputs							
AD05 AD05a	VREFH	Reference Voltage High	AVSS + 2.0 2.5	— —	AVDD 3.6	V V	**(Note 1)** VREFH = AVDD **(Note 3)**
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	**(Note 1)**
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	**(Note 3)**
AD08 AD08a	IREF	Current Drain	— —	250 —	400 3	µA µA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15	—	Leakage Current	—	±0.001	±0.610	µA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 kΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5k	Ω	**(Note 1)**
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V **(Note 2)**
AD23c	GERR	Gain Error	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	EOFF	Offset Error	> -1	—	< 1	Lsb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

31.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX 28/36/44-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 30.0 "Electrical Characteristics"**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "M", which denotes 50 MHz operation. For example, parameter DC29a in **Section 30.0 "Electrical Characteristics"**, is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/36/44-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on D+ or D- pin with respect to V_{USB3V3} ..... -0.3V to (V_{USB3V3} + 0.3V)
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +5.5V
Maximum current out of V_{SS} pin(s) ..... 300 mA
Maximum current into V_{DD} pin(s) **(Note 2)** ..... 300 mA
Maximum output current sunk by any I/O pin ..... 15 mA
Maximum output current sourced by any I/O pin ..... 15 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports **(Note 2)** ..... 200 mA

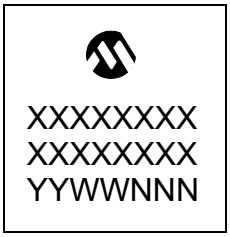
Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: See the **"Pin Diagrams"** section for the 5V tolerant pins.

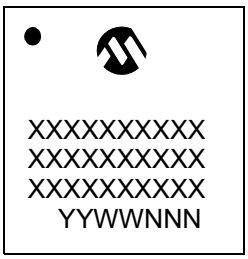
33.1 Package Marking Information (Continued)

36-Lead VTLA



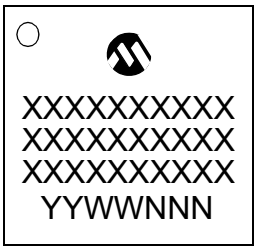
Example

44-Lead VTLA



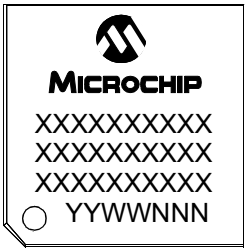
Example

44-Lead QFN

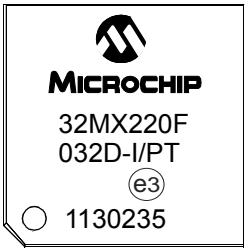


Example

44-Lead TQFP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

Revision G (April 2015)

This revision includes the addition of the following devices:

- PIC32MX130F256B
- PIC32MX230F256B
- PIC32MX130F256D
- PIC32MX230F256D

The title of the document was updated to avoid confusion with the PIC32MX1XX/2XX/5XX 64/100-pin Family data sheet.

All peripheral SFR maps have been relocated from the Memory chapter to their respective peripheral chapters.

In addition, this revision includes the following major changes as described in Table A-6, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-6: MAJOR SECTION UPDATES

Section	Update Description
32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog	Added new devices to the family features (see Table 1 and Table 2). Updated pin diagrams to include new devices (see Pin Diagrams).
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Updated these sections: **2.2 "Decoupling Capacitors"**, **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**, **2.4 "Master Clear (MCLR) Pin"**, **2.8.1 "Crystal Oscillator Design Consideration"**
4.0 "Memory Organization"	Added Memory Map for new devices (see Figure 4-6).
14.0 "Watchdog Timer (WDT)"	New chapter created from content previously located in the Special Features chapter.
30.0 "Electrical Characteristics"	Removed parameter D312 (TSET) from the Comparator Specifications (see Table 30-12). Added the Comparator Voltage Reference Specifications (see Table 30-13). Updated Table 30-12.

Revision H (July 2015)

This revision includes the following major changes as described in Table A-7, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-7: MAJOR SECTION UPDATES

Section	Update Description
2.0 "Guidelines for Getting Started with 32-bit MCUs"	**Section 2.9 "Sosc Design Recommendation"** was removed.
8.0 "Oscillator Configuration"	The Primary Oscillator (POSC) logic in the Oscillator diagram was updated (see Figure 8-1).
30.0 "Electrical Characteristics"	The Power-Down Current (IPD) DC Characteristics parameter DC40k was updated (see Table 30-7). **Table 30-9: "DC Characteristics: I/O Pin Input Injection current Specifications"** was added.