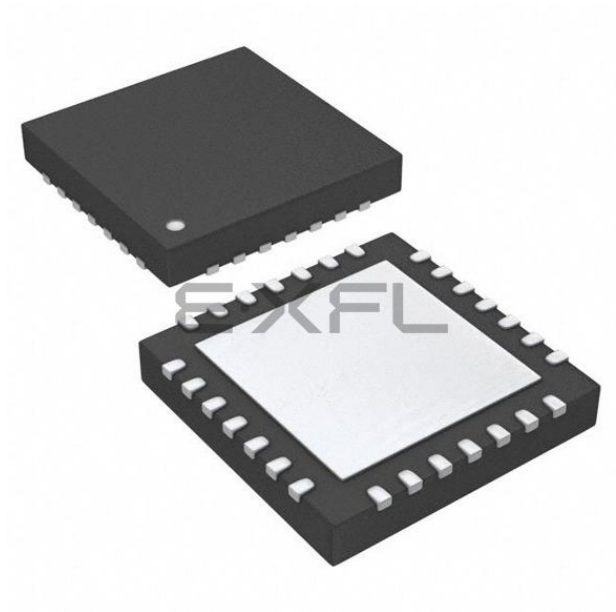
# Microchip Technology - PIC32MX230F256BT-50I/ML Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 19 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 9x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256bt-50i-ml |

**TABLE 14: PIN NAMES FOR 44-PIN USB DEVICES**

**44-PIN VTLA (TOP VIEW)(1,2,3,5)**

**PIC32MX210F016D**
**PIC32MX220F032D**
**PIC32MX230F064D**
**PIC32MX230F256D**
**PIC32MX250F128D**
**PIC32MX270F256D**

44 1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | RPB9/SDA1/CTED4/PMD3/RB9 | 23 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 |
| 2 | RPC6/PMA1/RC6 | 24 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 |
| 3 | RPC7/PMA0/RC7 | 25 | AN6/RPC0/RC0 |
| 4 | RPC8/PMA5/RC8 | 26 | AN7/RPC1/RC1 |
| 5 | RPC9/CTED7/PMA6/RC9 | 27 | AN8/RPC2/PMA2/RC2 |
| 6 | VSS | 28 | VDD |
| 7 | VCAP | 29 | VSS |
| 8 | PGED2/RPB10/D+/CTED11/RB10 | 30 | OSC1/CLKI/RPA2/RA2 |
| 9 | PGEC2/RPB11/D-/RB11 | 31 | OSC2/CLKO/RPA3/RA3 |
| 10 | VUSB3V3 | 32 | TDO/RPA8/PMA8/RA8 |
| 11 | AN11/RPB13/CTPLS/PMRD/RB13 | 33 | SOSCI/RPB4/RB4 |
| 12 | PGED4(4)/TMS/PMA10/RA10 | 34 | SOSCO/RPA4/T1CK/CTED9/RA4 |
| 13 | PGEC4(4)/TCK/CTED8/PMA7/RA7 | 35 | TDI/RPA9/PMA9/RA9 |
| 14 | CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14 | 36 | AN12/RPC3/RC3 |
| 15 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 | 37 | RPC4/PMA4/RC4 |
| 16 | AVSS | 38 | RPC5/PMA3/RC5 |
| 17 | AVDD | 39 | VSS |
| 18 | $\overline{\text{MCLR}}$ | 40 | VDD |
| 19 | PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 | 41 | RPB5/USBID/RB5 |
| 20 | PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 | 42 | VBUS |
| 21 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 | 43 | RPB7/CTED3/PMD5/INT0/RB7 |
| 22 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 | 44 | RPB8/SCL1/CTED10/PMD4/RB8 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** This pin function is not available on PIC32MX210F016D and PIC32MX220F032D devices.

**5:** Shaded pins are 5V tolerant.

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### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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## 9.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32, such as Peripheral Bus devices: SPI, UART, PMP, etc., or memory itself. Figure 9-1 show a block diagram of the DMA Controller module.

The DMA Controller module has the following key features:

- Four identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

**FIGURE 9-1: DMA BLOCK DIAGRAM**

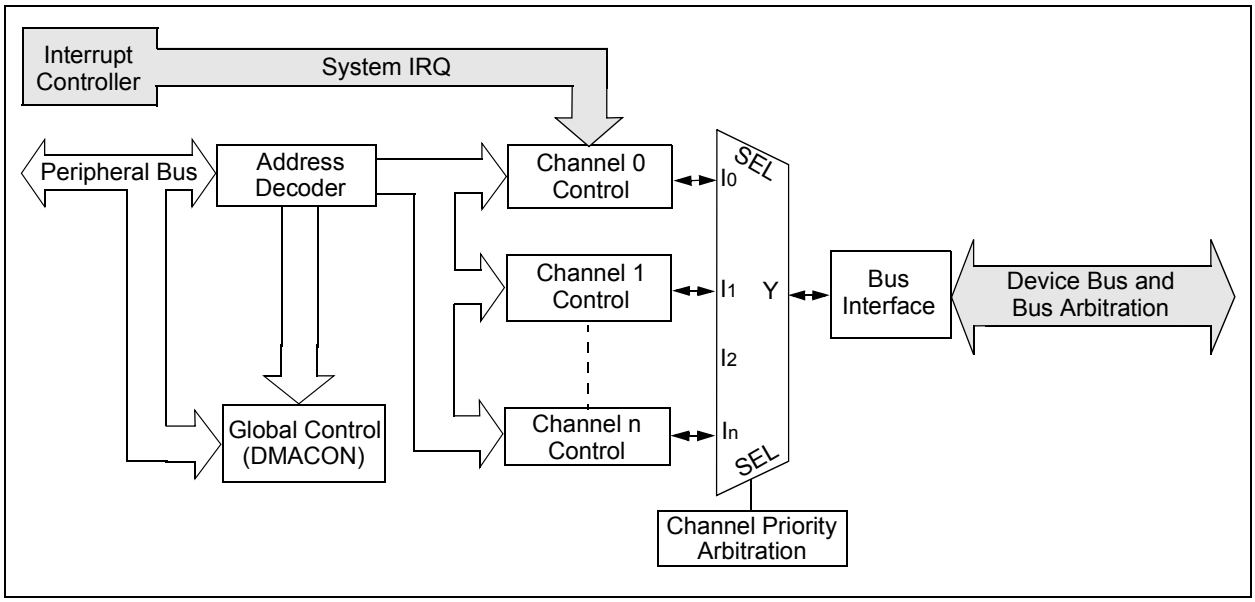


**TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3170 | DCH1SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3180 | DCH1DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3190 | DCH1SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31A0 | DCH1DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31B0 | DCH1CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31C0 | DCH1CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31D0 | DCH1DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 31E0 | DCH2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 31F0 | DCH2ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 3200 | DCH2INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3210 | DCH2SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3220 | DCH2DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3230 | DCH2SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3240 | DCH2DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3250 | DCH2SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3260 | DCH2DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3270 | DCH2CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

**REGISTER 10-6: U1IR: USB INTERRUPT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R-0 | R/WC-0, HS |
| | STALLIF | ATTACHIF(1) | RESUMEIF(2) | IDLEIF | TRNIF(3) | SOFIF | UERRIF(4) | URSTIF(5) / DETACHIF(6) |

| Legend: | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
1 = In Host mode a STALL handshake was received during the handshake phase of the transaction
In Device mode a STALL handshake was transmitted during the handshake phase of the transaction
0 = STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit(1)
1 = Peripheral attachment was detected by the USB module
0 = Peripheral attachment was not detected

bit 5 **RESUMEIF:** Resume Interrupt bit(2)
1 = K-State is observed on the D+ or D- pin for 2.5 µs
0 = K-State is not observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
1 = Idle condition detected (constant Idle state of 3 ms or more)
0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit(3)
1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information
0 = Processing of current token not complete

bit 2 **SOFIF:** SOF Token Interrupt bit
1 = SOF token received by the peripheral or the SOF threshold reached by the host
0 = SOF token was not received nor threshold reached

bit 1 **UERRIF**: USB Error Condition Interrupt bit(4)
1 = Unmasked error condition has occurred
0 = Unmasked error condition has not occurred

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)(5)
1 = Valid USB Reset has occurred
0 = No USB Reset has occurred
**DETACHIF:** USB Detach Interrupt bit (Host mode)(6)
1 = Peripheral detachment was detected by the USB module
0 = Peripheral detachment was not detected

**Note 1:** This bit is valid only if the HOSTEN bit is set (see Register 10-11), there is no activity on the USB for 2.5 µs, and the current bus state is not SE0.
**2:** When not in Suspend mode, this interrupt should be disabled.
**3:** Clearing this bit will cause the STAT FIFO to advance.
**4:** Only error conditions enabled through the U1EIE register will set this bit.
**5:** Device mode.
**6:** Host mode.

**REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS |
| | BTSEF | BMXEF | DMAEF(1) | BTOEF(2) | DFN8EF | CRC16EF | CRC5EF(4) / EOFEF(3,5) | PIDEF |

| Legend: | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit
- 1 = Packet rejected due to bit stuff error
- 0 = Packet accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
- 1 = The base address, of the Buffer Descriptor Table, or the address of an individual buffer pointed to by a Buffer Descriptor Table entry, is invalid.
- 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit(1)
- 1 = USB DMA error condition detected
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit(2)
- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit
- 1 = Data field received is not an integral number of bytes
- 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
- 1 = Data packet rejected due to CRC16 error
- 0 = Data packet accepted

**Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

**2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

**3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

**4:** Device mode.

**5:** Host mode.

**TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FB00 | RPA0R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA0<3:0> | | | | 0000 |
| FB04 | RPA1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA1<3:0> | | | | 0000 |
| FB08 | RPA2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA2<3:0> | | | | 0000 |
| FB0C | RPA3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA3<3:0> | | | | 0000 |
| FB10 | RPA4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA4<3:0> | | | | 0000 |
| FB20 | RPA8R(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA8<3:0> | | | | 0000 |
| FB24 | RPA9R(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPA9<3:0> | | | | 0000 |
| FB2C | RPB0R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB0<3:0> | | | | 0000 |
| FB30 | RPB1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB1<3:0> | | | | 0000 |
| FB34 | RPB2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB2<3:0> | | | | 0000 |
| FB38 | RPB3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB3<3:0> | | | | 0000 |
| FB3C | RPB4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB4<3:0> | | | | 0000 |
| FB40 | RPB5R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB5<3:0> | | | | 0000 |
| FB44 | RPB6R(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB6<3:0> | | | | 0000 |
| FB48 | RPB7R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB7<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is only available on 44-pin devices.
**2:** This register is only available on PIC32MX1XX devices.
**3:** This register is only available on 36-pin and 44-pin devices.

## 13.2 Timer Control Registers

**TABLE 13-1: TIMER2-TIMER5 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0800 | T2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | T32 | — | TCS | — | 0000 |
| 0810 | TMR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR2<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0820 | PR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR2<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0A00 | T3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | — | — | TCS | — | 0000 |
| 0A10 | TMR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR3<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0A20 | PR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR3<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0C00 | T4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | T32 | — | TCS | — | 0000 |
| 0C10 | TMR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR4<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0C20 | PR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR4<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0E00 | T5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | — | — | TCS | — | 0000 |
| 0E10 | TMR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR5<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0E20 | PR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR5<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

Figure 19-2 and Figure 19-3 illustrate typical receive and transmit timing for the UART module.

**FIGURE 19-2: UART RECEPTION**

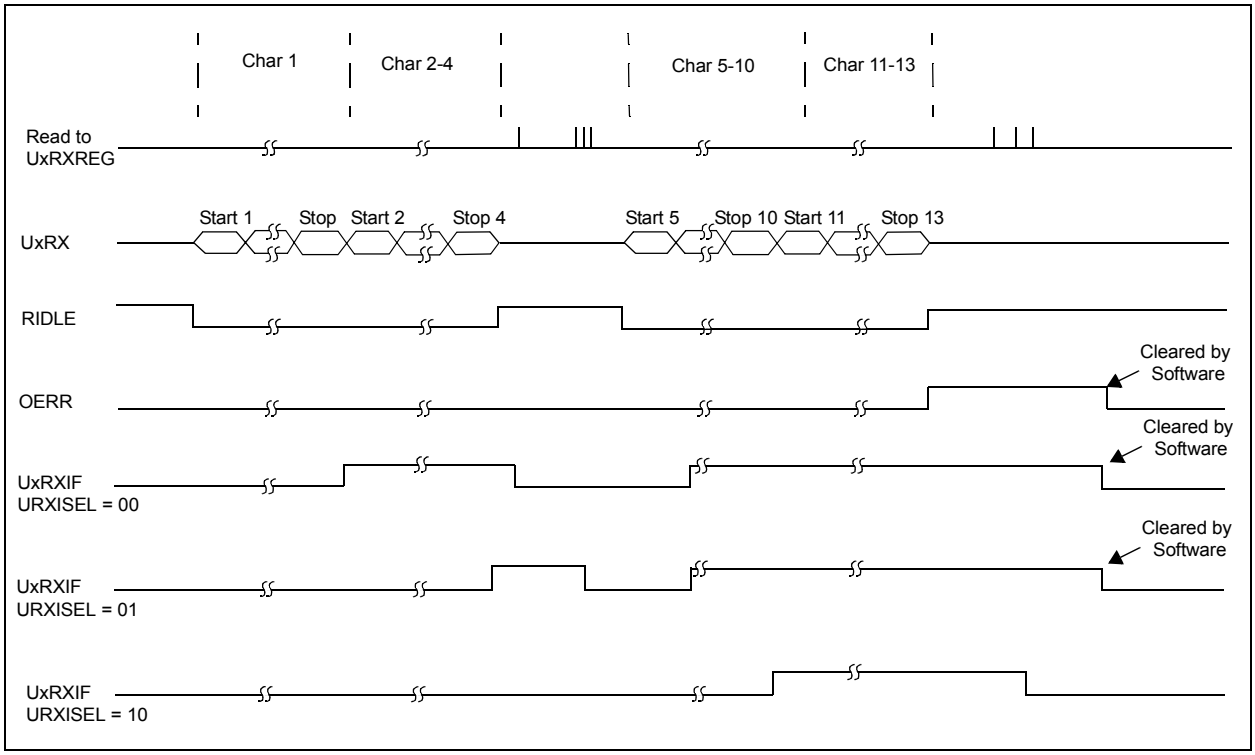
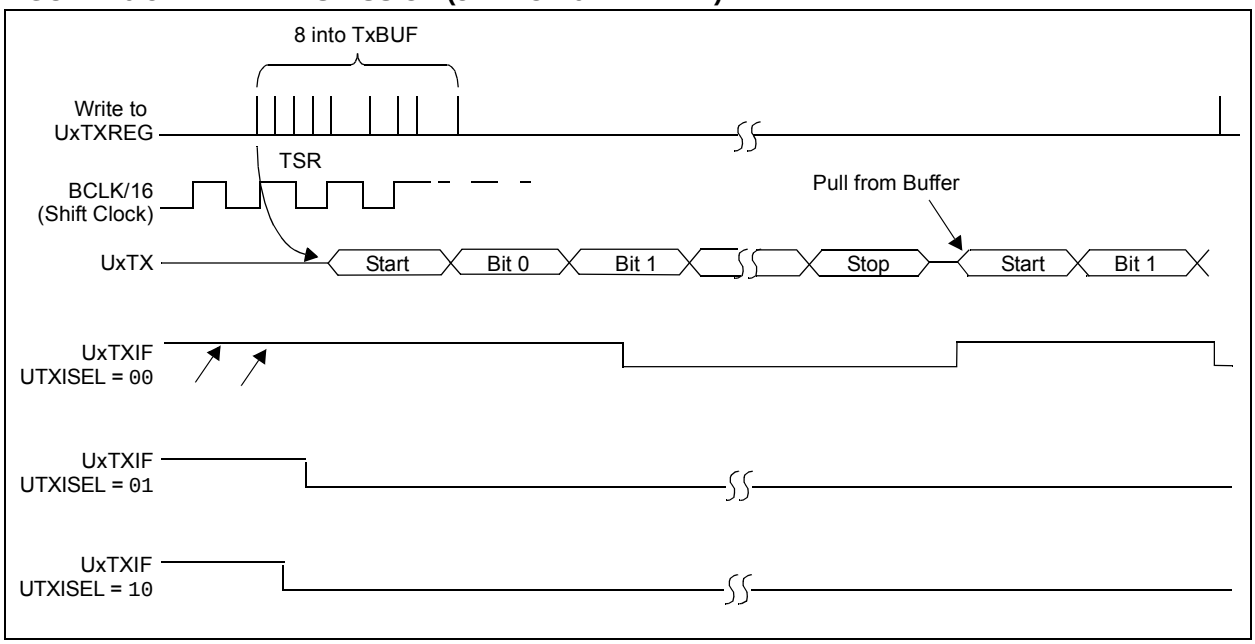



**FIGURE 19-3: TRANSMISSION (8-BIT OR 9-BIT DATA)**



**REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | FORM<2:0> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0, HSC | R/C-0, HSC |
| | SSRC<2:0> | | | CLRASAM | — | ASAM | SAMP(2) | DONE(3) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit(1)
- 1 = ADC module is operating
- 0 = ADC module is not operating

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits
- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
- 000 =Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.

**3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

**REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)**

bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)
1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
0 = Normal operation, buffer contents will be overwritten by the next conversion sequence

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit(2)
1 = The ADC sample and hold amplifier is sampling
0 = The ADC sample/hold amplifier is holding
When ASAM = 0, writing '1' to this bit starts sampling.
When SSRC = 000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** Analog-to-Digital Conversion Status bit(3)
1 = Analog-to-digital conversion is done
0 = Analog-to-digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.

**3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

**REGISTER 22-3: AD1CON3: ADC CONTROL REGISTER 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADRC | — | — | SAMC<4:0>(1) | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W | R/W-0 |
| | ADCS<7:0>(2) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = Clock derived from FRC
0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits(2)
11111111 = TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD
•
•
•
00000001 = TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD
00000000 = TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

**Note 1:** This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
**2:** This bit is not used if the ADRC (AD1CON3<15>) bit = 1.

**REGISTER 24-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | — | — | — | — | — | — |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | CVROE | CVRR | CVRSS | CVR<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit(1)
- 1 = Module is enabled
  Setting this bit does not affect other bits in the register.
- 0 = Module is disabled and does not consume current.
  Clearing this bit does not affect the other bits in the register.

bit 14-7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** CVREFOUT Enable bit
- 1 = Voltage level is output on CVREFOUT pin
- 0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit
- 1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size
- 0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit
- 1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)
- 0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>:** CVREF Value Selection 0 ≤ CVR<3:0> ≤ 15 bits

When CVRR = 1:
CVREF = (CVR<3:0>/24) • (CVRSRC)

When CVRR = 0:
CVREF = 1/4 • (CVRSRC) + (CVR<3:0>/32) • (CVRSRC)

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)**

bit 24 **EDG1STAT:** Edge1 Status bit
Indicates the status of Edge1 and can be written to control edge source
1 = Edge1 has occurred
0 = Edge1 has not occurred

bit 23 **EDG2MOD:** Edge2 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 22 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge2 programmed for a positive edge response
0 = Edge2 programmed for a negative edge response

bit 21-18 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = C3OUT pin is selected
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = PBCLK clock is selected
1011 = IC3 Capture Event is selected
1010 = IC2 Capture Event is selected
1001 = IC1 Capture Event is selected
1000 = CTED13 pin is selected
0111 = CTED12 pin is selected
0110 = CTED11 pin is selected
0101 = CTED10 pin is selected
0100 = CTED9 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 17-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ON Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode

bit 12 **TGEN:** Time Generation Enable bit**(1)**
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

**Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

**2:** The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**3:** Refer to the CTMU Current Source Specifications (Table 30-41) in **Section 30.0 "Electrical Characteristics"** for current values.

**4:** This bit setting is not available for the CTMU temperature diode.

## 27.2 Configuration Registers

### TABLE 27-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

| Virtual Address (BFC0_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0BF0 | DEVCFG3 | 31:16 | FVBUSONIO | FUSBIDIO | IOL1WAY | PMDL1WAY | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | USERID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 0BF4 | DEVCFG2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | FPLLODIV<2:0> | | | xxxx |
| | | 15:0 | UPLLEN(1) | — | — | — | — | UPLLIDIV<2:0>(1) | | | — | FPLLMUL<2:0> | | | — | FPLLIDIV<2:0> | | | xxxx |
| 0BF8 | DEVCFG1 | 31:16 | — | — | — | — | — | — | FWDTWINSZ<1:0> | | FWDTEN | WINDIS | — | WDTPS<4:0> | | | | | xxxx |
| | | 15:0 | FCKSM<1:0> | | FPBDIV<1:0> | | — | OSCIOFNC | POSCMOD<1:0> | | IESO | — | FSOSCEN | — | — | FNOSC<2:0> | | | xxxx |
| 0BFC | DEVCFG0 | 31:16 | — | — | — | CP | — | — | — | BWP | — | — | — | — | — | PWP<8:6>(2) | | | xxxx |
| | | 15:0 | PWP<5:0> | | | | | | — | — | — | — | — | ICESEL<1:0> | | JTAGEN | DEBUG<1:0> | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is only available on PIC32MX2XX devices.

**2:** PWP<8:7> are only available on devices with 256 KB of Flash.

### TABLE 27-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F220 | DEVID | 31:16 | VER<3:0> | | | | DEVID<27:16> | | | | | | | | | | | | xxxx(1) |
| | | 15:0 | DEVID<15:0> | | | | | | | | | | | | | | | | xxxx(1) |
| F200 | CFGCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | IOLOCK | PMDLOCK | — | — | — | — | — | — | — | — | JTAGEN | — | — | TDOEN | 000B |
| F230 | SYSKEY(3) | 31:16 | SYSKEY<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Reset values are dependent on the device variant.

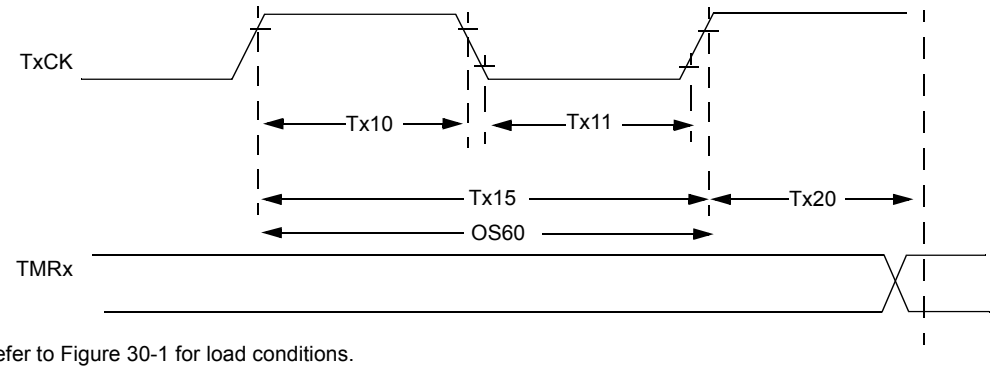
**TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDD | **Supply Voltage (Note 2)** | 2.3 | — | 3.6 | V | — |
| DC12 | VDR | **RAM Data Retention Voltage (Note 1)** | 1.75 | — | — | V | — |
| DC16 | VPOR | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | 1.75 | — | 2.1 | V | — |
| DC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 0.00005 | — | 0.115 | V/μs | — |

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.

**FIGURE 30-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS**

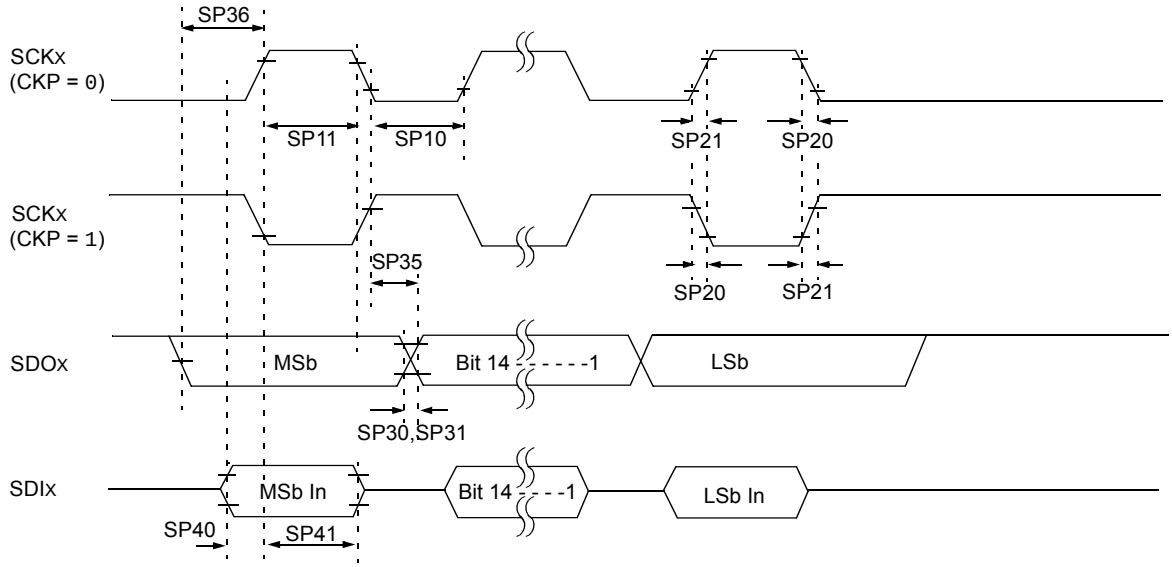
| **AC CHARACTERISTICS(1)** | | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| TA10 | TTXH | TxCK High Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | — | ns | Must also meet parameter TA15 |
| | | | Asynchronous, with prescaler | 10 | — | — | ns | — |
| TA11 | TTXL | TxCK Low Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | — | ns | Must also meet parameter TA15 |
| | | | Asynchronous, with prescaler | 10 | — | — | ns | — |
| TA15 | TTXP | TxCK Input Period | Synchronous, with prescaler | [(Greater of 25 ns or 2 TPB)/N] + 30 ns | — | — | ns | VDD > 2.7V |
| | | | | [(Greater of 25 ns or 2 TPB)/N] + 50 ns | — | — | ns | VDD < 2.7V |
| | | | Asynchronous, with prescaler | 20 | — | — | ns | VDD > 2.7V **(Note 3)** |
| | | | | 50 | — | — | ns | VDD < 2.7V **(Note 3)** |
| OS60 | FT1 | SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting the TCS (T1CON<1>) bit) | | 32 | — | 100 | kHz | — |
| TA20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | — | 1 | TPB | — |

**Note 1:** Timer1 is a Type A timer.

**2:** This parameter is characterized, but not tested in manufacturing.

**3:** N = Prescale Value (1, 8, 64, 256).

**FIGURE 30-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP11 | TscH | SCKx Output High Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP20 | TscF | SCKx Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 15 | — | — | ns | — |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

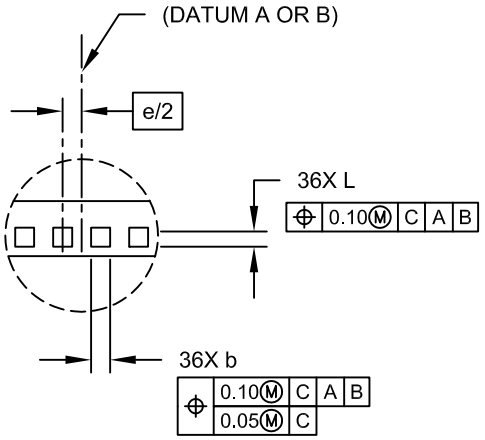
**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

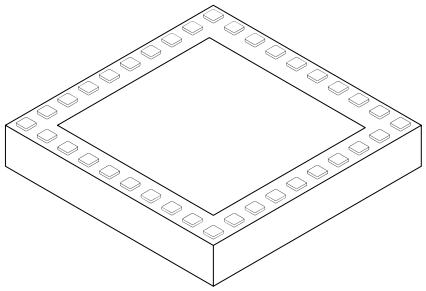
**4:** Assumes 50 pF load on all SPIx pins.

## 36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL A**



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension | Limits | MIN | NOM | MAX |
| Number of Pins | N | | 36 | |
| Number of Pins per Side | ND | | 10 | |
| Number of Pins per Side | NE | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.025 | - | 0.075 |
| Overall Width | E | | 5.00 BSC | |
| Exposed Pad Width | E2 | 3.60 | 3.75 | 3.90 |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 3.60 | 3.75 | 3.90 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.25 | 0.30 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2

## Revision E (October 2012)

All singular pin diagram occurrences of CVREF were changed to: CVREFOUT. In addition, minor text and formatting changes were incorporated throughout the document.

All major changes are referenced by their respective section in Table A-4.

**TABLE A-4: MAJOR SECTION UPDATES**

| Section | Update Description |
|---|---|
| **"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"** | Updated the following feature sections:<br>• **"Operating Conditions"**<br>• **"Communication Interfaces"** |
| **2.0 "Guidelines for Getting Started with 32-bit MCUs"** | Removed Section 2.8 "Configuration of Analog and Digital Pins During ICSP Operations". |
| **3.0 "CPU"** | Removed references to GPR shadow registers in **3.1 "Features"** and **3.2.1 "Execution Unit"**. |
| **4.0 "Memory Organization"** | Updated the BRG bit range in the SPI1 and SPI2 Register Map (see Table 4-8).<br>Added the PWP<6> bit to the Device Configuration Word Summary (see Table 4-17). |
| **5.0 "Flash Program Memory"** | Added a note with Flash page size and row size information. |
| **7.0 "Interrupt Controller"** | Updated the TPC<2:0> bit definitions (see Register 7-1).<br>Updated the IPTMR<31:0> bit definition (see Register 7-3). |
| **8.0 "Oscillator Configuration"** | Updated the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1).<br>Updated the RODIV<14:0> bit definitions (see Register 8-3). |
| **10.0 "USB On-The-Go (OTG)"** | Updated the Notes in the USB Interface Diagram (see Figure 10-1). |
| **18.0 "Universal Asynchronous Receiver Transmitter (UART)"** | Updated the baud rate range in the list of primary features. |
| **26.0 "Special Features"** | Added the PWP<6> bit to the Device Configuration Word 0 (see Register 26-1). |
| **29.0 "Electrical Characteristics"** | Added Note 1 to Operating MIPS vs. Voltage (see Table 29-1).<br>Added Note 2 to DC Temperature and Voltage Specifications (see Table 29-4).<br>Updated the Conditions for parameter DC25 in DC Characteristics: Operating Current (IDD) (see Table 29-5).<br>Added Note 2 to Electrical Characteristics: BOR (see Table 29-10).<br>Added Note 4 to Comparator Specifications (see Table 29-12).<br>Added Note 5 to ADC Module Specifications (see Table 29-32).<br>Updated the 10-bit Conversion Rate Parameters and added Note 3 (see Table 29-33).<br>Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 29-34).<br>Added Note 3 to CTMU Current Source Specifications (see Table 29-39). |
| **30.0 "50 MHz Electrical Characteristics"** | New chapter with electrical characteristics for 50 MHz devices. |
| **31.0 "Packaging Information"** | The 36-pin and 44-pin VTLA packages have been updated. |