## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 40MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 19 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 9x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256bt-i-ss |

**TABLE 1: PIC32MX1XX 28/36/44-PIN GENERAL PURPOSE FAMILY FEATURES**

| Device | Pins | Program Memory (KB)[1] | Data Memory (KB) | Remappable Peripherals | | | | | Analog Comparators | USB On-The-Go (OTG) | I$^2$C | PMP | DMA Channels (Programmable/Dedicated) | CTMU | 10-bit 1 Msps ADC (Channels) | RTCC | I/O Pins | JTAG | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Remappable Pins | Timers[2]/Capture/Compare | UART | SPI/I$^2$S | External Interrupts[3] | | | | | | | | | | | |
| PIC32MX110F016B | 28 | 16+3 | 4 | 20 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 10 | Y | 21 | Y | SOIC, SSOP, SPDIP, QFN |
| PIC32MX110F016C | 36 | 16+3 | 4 | 24 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 12 | Y | 25 | Y | VTLA |
| PIC32MX110F016D | 44 | 16+3 | 4 | 32 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 13 | Y | 35 | Y | VTLA, TQFP, QFN |
| PIC32MX120F032B | 28 | 32+3 | 8 | 20 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 10 | Y | 21 | Y | SOIC, SSOP, SPDIP, QFN |
| PIC32MX120F032C | 36 | 32+3 | 8 | 24 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 12 | Y | 25 | Y | VTLA |
| PIC32MX120F032D | 44 | 32+3 | 8 | 32 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 13 | Y | 35 | Y | VTLA, TQFP, QFN |
| PIC32MX130F064B | 28 | 64+3 | 16 | 20 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 10 | Y | 21 | Y | SOIC, SSOP, SPDIP, QFN |
| PIC32MX130F064C | 36 | 64+3 | 16 | 24 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 12 | Y | 25 | Y | VTLA |
| PIC32MX130F064D | 44 | 64+3 | 16 | 32 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 13 | Y | 35 | Y | VTLA, TQFP, QFN |
| PIC32MX150F128B | 28 | 128+3 | 32 | 20 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 10 | Y | 21 | Y | SOIC, SSOP, SPDIP, QFN |
| PIC32MX150F128C | 36 | 128+3 | 32 | 24 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 12 | Y | 25 | Y | VTLA |
| PIC32MX150F128D | 44 | 128+3 | 32 | 32 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 13 | Y | 35 | Y | VTLA, TQFP, QFN |
| PIC32MX130F256B | 28 | 256+3 | 16 | 20 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 10 | Y | 21 | Y | SOIC, SSOP, SPDIP, QFN |
| PIC32MX130F256D | 44 | 256+3 | 16 | 32 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 13 | Y | 35 | Y | VTLA, TQFP, QFN |
| PIC32MX170F256B | 28 | 256+3 | 64 | 20 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 10 | Y | 21 | Y | SOIC, SSOP, SPDIP, QFN |
| PIC32MX170F256D | 44 | 256+3 | 64 | 32 | 5/5/5 | 2 | 2 | 5 | 3 | N | 2 | Y | 4/0 | Y | 13 | Y | 35 | Y | VTLA, TQFP, QFN |

**Note 1:** This device features 3 KB of boot Flash memory.

**2:** Four out of five timers are remappable.

**3:** Four out of five external interrupts are remappable.

**TABLE 4-1: SFR MEMORY MAP**

| Peripheral | Virtual Address | |
|---|---|---|
| | Base | Offset Start |
| Watchdog Timer | 0xBF80 | 0x0000 |
| RTCC | | 0x0200 |
| Timer1-5 | | 0x0600 |
| Input Capture 1-5 | | 0x2000 |
| Output Compare 1-5 | | 0x3000 |
| IC1 and IC2 | | 0x5000 |
| SPI1 and SPI2 | | 0x5800 |
| UART1 and UART2 | | 0x6000 |
| PMP | | 0x7000 |
| ADC | | 0x9000 |
| CVREF | | 0x9800 |
| Comparator | | 0xA000 |
| CTMU | | 0xA200 |
| Oscillator | | 0xF000 |
| Device and Revision ID | | 0xF220 |
| Peripheral Module Disable | | 0xF240 |
| Flash Controller | | 0xF400 |
| Reset | | 0xF600 |
| PPS | | 0xFA04 |
| Interrupts | 0xBF88 | 0x1000 |
| Bus Matrix | | 0x2000 |
| DMA | | 0x3000 |
| USB | | 0x5050 |
| PORTA-PORTC | | 0x6000 |
| Configuration | 0xBFC0 | 0x0BF0 |

## 6.1 Reset Control Registers

### TABLE 6-1: RESET CONTROL REGISTER MAP

| Virtual Address (BF80_#) | Register Name$^{(1)}$ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F600 | RCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CMR | VREGS | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR | POR | xxxx$^{(2)}$ |
| F610 | RSWRST | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SWRST | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

### REGISTER 10-11: U1CON: USB CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-x | R-x | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | JSTATE | SE0 | PKTDIS(4)<br>TOKBUSY(1,5) | USBRST | HOSTEN(2) | RESUME(3) | PPBRST | USBEN(4)<br>SOFEN(5) |

**Legend:**

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’

-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit
1 = JSTATE was detected on the USB
0 = No JSTATE was detected

bit 6 **SE0:** Live Single-Ended Zero flag bit
1 = Single-Ended Zero was detected on the USB
0 = No Single-Ended Zero was detected

bit 5 **PKTDIS:** Packet Transfer Disable bit(4)
1 = Token and packet processing is disabled (set upon SETUP token received)
0 = Token and packet processing is enabled

**TOKBUSY:** Token Busy Indicator bit(1,5)
1 = Token is being executed by the USB module
0 = No token is being executed

bit 4 **USBRST:** Module Reset bit(5)
1 = USB reset generated
0 = USB reset terminated

bit 3 **HOSTEN:** Host Mode Enable bit(2)
1 = USB host capability is enabled
0 = USB host capability is disabled

bit 2 **RESUME:** RESUME Signaling Enable bit(3)
1 = RESUME signaling is activated
0 = RESUME signaling is disabled

**Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).

**2:** All host control logic is reset any time that the value of this bit is toggled.

**3:** Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.

**4:** Device mode.

**5:** Host mode.

**REGISTER 11-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A, B, C)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as ‘`0`’

bit 15 **ON:** Change Notice (CN) Control ON bit

`1` = CN is enabled
`0` = CN is disabled

bit 14 **Unimplemented:** Read as ‘`0`’

bit 13 **SIDL:** Stop in Idle Control bit

`1` = Idle mode halts CN operation
`0` = Idle does not affect CN operation

bit 12-0 **Unimplemented:** Read as ‘`0`’

### REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

| | |
|---|---|
| bit 3 | **T32:** 32-Bit Timer Mode Select bit(2)<br>`1` = Odd numbered and even numbered timers form a 32-bit timer<br>`0` = Odd numbered and even numbered timers form a separate 16-bit timer |
| bit 2 | **Unimplemented:** Read as ‘`0`’ |
| bit 1 | **TCS:** Timer Clock Source Select bit(3)<br>`1` = External clock from TxCK pin<br>`0` = Internal peripheral clock |
| bit 0 | **Unimplemented:** Read as ‘`0`’ |

**Note 1:** When using 1:1 PBCLK divisor, the user’s software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

**2:** This bit is available only on even numbered timers (Timer2 and Timer4).

**3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.

**4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

### REGISTER 15-1: ICxCON: INPUT CAPTURE ‘x’ CONTROL REGISTER (CONTINUED)

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits

`111` = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
`110` = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
`101` = Prescaled Capture Event mode – every sixteenth rising edge
`100` = Prescaled Capture Event mode – every fourth rising edge
`011` = Simple Capture Event mode – every rising edge
`010` = Simple Capture Event mode – every falling edge
`001` = Edge Detect mode – every edge (rising and falling)
`000` = Input Capture module is disabled

**Note 1:** When using 1:1 PBCLK divisor, the user’s software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

### REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
`1` = Frame synchronization pulse coincides with the first bit clock
`0` = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(2)
`1` = Enhanced Buffer mode is enabled
`0` = Enhanced Buffer mode is disabled

bit 15 **ON:** SPI Peripheral On bit(1)
`1` = SPI Peripheral is enabled
`0` = SPI Peripheral is disabled

bit 14 **Unimplemented:** Read as ‘`0`’

bit 13 **SIDL:** Stop in Idle Mode bit
`1` = Discontinue module operation when the device enters Idle mode
`0` = Continue module operation when the device enters Idle mode

bit 12 **DISSDO:** Disable SDOx pin bit
`1` = SDOx pin is not used by the module. Pin is controlled by associated PORT register
`0` = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits

When AUDEN = `1`:

| MODE32 | MODE16 | Communication |
|---|---|---|
| 1 | 1 | 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame |
| 1 | 0 | 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame |
| 0 | 1 | 16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame |
| 0 | 0 | 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame |

When AUDEN = `0`:

| MODE32 | MODE16 | Communication |
|---|---|---|
| 1 | x | 32-bit |
| 0 | 1 | 16-bit |
| 0 | 0 | 8-bit |

bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = `1`):
`1` = Input data sampled at end of data output time
`0` = Input data sampled at middle of data output time
Slave mode (MSTEN = `0`):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = `0`.

To write a '`1`' to this bit, the MSTEN value = `1` must first be written.

bit 8 **CKE:** SPI Clock Edge Select bit(3)
`1` = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
`0` = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
`1` = $\overline{\text{SSx}}$ pin used for Slave mode
`0` = $\overline{\text{SSx}}$ pin not used for Slave mode, pin controlled by port function.

bit 6 **CKP:** Clock Polarity Select bit(4)
`1` = Idle state for clock is a high level; active state is a low level
`0` = Idle state for clock is a low level; active state is a high level

**Note 1:** When using the 1:1 PBCLK divisor, the user’s software should not read or write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

**2:** This bit can only be written when the ON bit = `0`.

**3:** This bit is not used in the Framed SPI mode. The user should program this bit to ‘`0`’ for the Framed SPI mode (FRMEN = `1`).

**4:** When AUDEN = `1`, the SPI module functions as if the CKP bit is equal to ‘`1`’, regardless of the actual value of CKP.

**NOTES:**

## 20.1 PMP Control Registers

### TABLE 20-1: PARALLEL MASTER PORT REGISTER MAP

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 7000 | PMCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | ADRMUX<1:0> | | PMPTTL | PTWREN | PTRDEN | CSF<1:0> | | ALP | — | CS1P | — | WRSP | RDSP | 0000 |
| 7010 | PMMODE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BUSY | IRQM<1:0> | | INCM<1:0> | | — | MODE<1:0> | | WAITB<1:0> | | WAITM<3:0> | | | | WAITE<1:0> | | 0000 |
| 7020 | PMADDR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | CS1<br>ADDR14 | — | — | — | ADDR<10:0> | | | | | | | | | | | 0000 |
| 7030 | PMDOUT | 31:16 | DATAOUT<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 7040 | PMDIN | 31:16 | DATAIN<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 7050 | PMAEN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | PTEN14 | — | — | — | PTEN<10:0> | | | | | | | | | | | 0000 |
| 7060 | PMSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F | OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E | 008F |

**Legend:** x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

## 22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

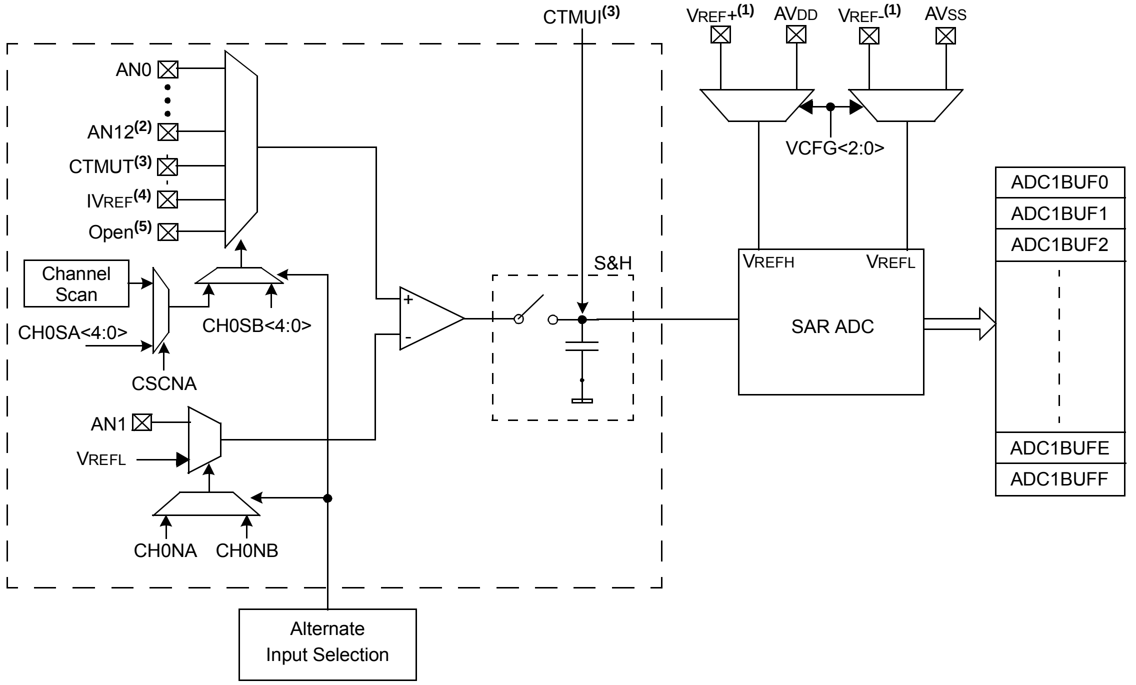
> **Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 13 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. Figure 22-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

**FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM**



**Note 1:** VREF+ and VREF- inputs can be multiplexed with other analog inputs.

**2:** AN8 is only available on 44-pin devices. AN6, AN7, and AN12 are not available on 28-pin devices.

**3:** Connected to the CTMU module. See **Section 25.0 "Charge Time Measurement Unit (CTMU)"** for more information.

**4:** Internal precision voltage reference (1.2V).

**5:** This selection is only used with CTMU capacitive and time measurement.

**TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

| AC CHARACTERISTICS | | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.(1)** | **Max.** | **Units** | **Conditions** |
| IM10 | TLO:SCL | Clock Low Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | — |
| IM11 | THI:SCL | Clock High Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | — |
| IM20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode **(Note 2)** | — | 100 | ns | |
| IM21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode **(Note 2)** | — | 300 | ns | |
| IM25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | — |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode **(Note 2)** | 100 | — | ns | |
| IM26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | — |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode **(Note 2)** | 0 | 0.3 | µs | |
| IM30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | |
| IM31 | THD:STA | Start Condition Hold Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | |
| IM33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | µs | |
| IM34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | TPB * (BRG + 2) | — | ns | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | ns | |
| | | | 1 MHz mode **(Note 2)** | TPB * (BRG + 2) | — | ns | |

**Note 1:** BRG is the value of the $I^2C$ Baud Rate Generator.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

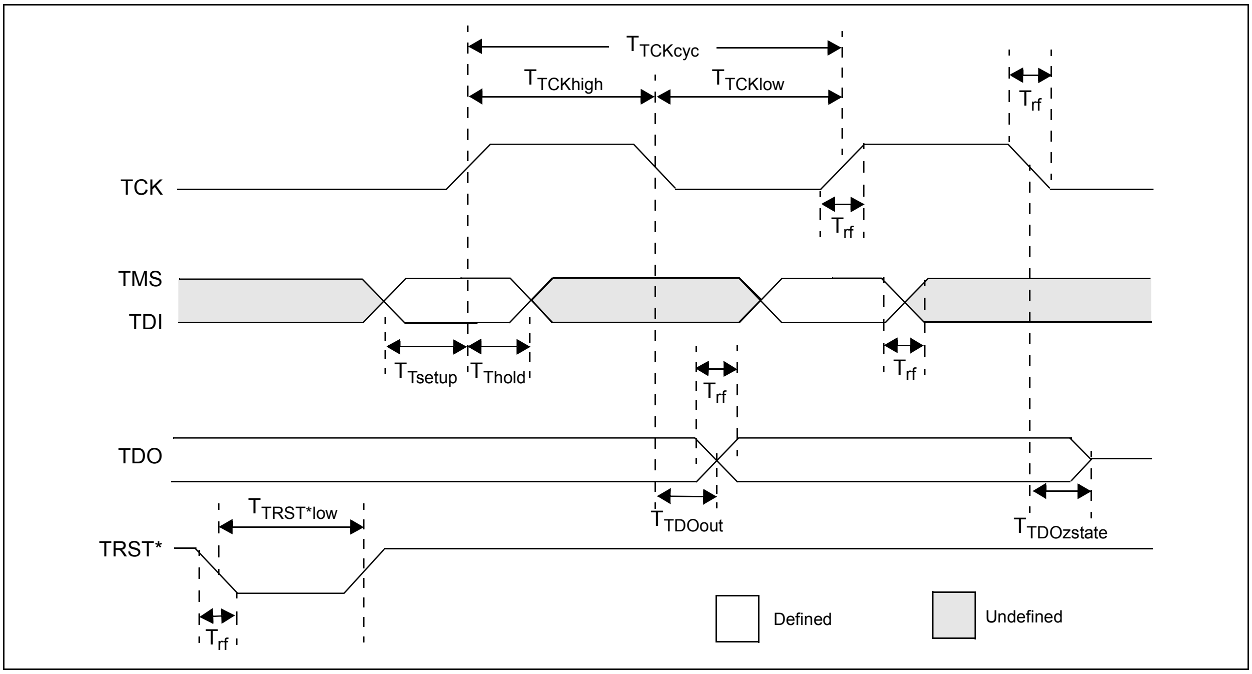
**3:** The typical value for this parameter is 104 ns.

### TABLE 30-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

| **AC CHARACTERISTICS** | | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | μs | PBCLK must operate at a minimum of 800 kHz |
| | | | 400 kHz mode | 1.3 | — | μs | PBCLK must operate at a minimum of 3.2 MHz |
| | | | 1 MHz mode **(Note 1)** | 0.5 | — | μs | — |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | μs | PBCLK must operate at a minimum of 800 kHz |
| | | | 400 kHz mode | 0.6 | — | μs | PBCLK must operate at a minimum of 3.2 MHz |
| | | | 1 MHz mode **(Note 1)** | 0.5 | — | μs | — |
| IS20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode **(Note 1)** | — | 100 | ns | |
| IS21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode **(Note 1)** | — | 300 | ns | |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | — |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | — |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| | | | 1 MHz mode **(Note 1)** | 0 | 0.3 | μs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4700 | — | ns | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 250 | — | ns | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4000 | — | ns | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 250 | — | ns | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 600 | — | ns | |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

FIGURE 30-23: EJTAG TIMING CHARACTERISTICS



### TABLE 30-42: EJTAG TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ $T_A$ ≤ +85°C for Industrial<br>-40°C ≤ $T_A$ ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Description[1]** | **Min.** | **Max.** | **Units** | **Conditions** |
| EJ1 | TTCKCYC | TCK Cycle Time | 25 | — | ns | — |
| EJ2 | TTCKHIGH | TCK High Time | 10 | — | ns | — |
| EJ3 | TTCKLOW | TCK Low Time | 10 | — | ns | — |
| EJ4 | TTSETUP | TAP Signals Setup Time Before Rising TCK | 5 | — | ns | — |
| EJ5 | TTHOLD | TAP Signals Hold Time After Rising TCK | 3 | — | ns | — |
| EJ6 | TTDOOUT | TDO Output Delay Time from Falling TCK | — | 5 | ns | — |
| EJ7 | TTDOZSTATE | TDO 3-State Delay Time from Falling TCK | — | 5 | ns | — |
| EJ8 | TTRSTLOW | TRST Low Time | 25 | — | ns | — |
| EJ9 | TRF | TAP Signals Rise/Fall Time, All Input and Output | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

### TABLE 31-5: EXTERNAL CLOCK TIMING REQUIREMENTS

| **AC CHARACTERISTICS** | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| MOS10 | FOSC | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC<br>4 | —<br>— | 50<br>50 | MHz<br>MHz | EC **(Note 2)**<br>ECPLL **(Note 1)** |

**Note 1:** PLL input requirements: 4 MHz ≤ FPLLIN ≤ 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

**2:** This parameter is characterized, but not tested in manufacturing.

### TABLE 31-6: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

| **AC CHARACTERISTICS** | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| MSP10 | TSCL | SCKx Output Low Time **(Note 1,2)** | TSCK/2 | — | — | ns | — |
| MSP11 | TSCH | SCKx Output High Time **(Note 1,2)** | TSCK/2 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

### TABLE 31-7: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

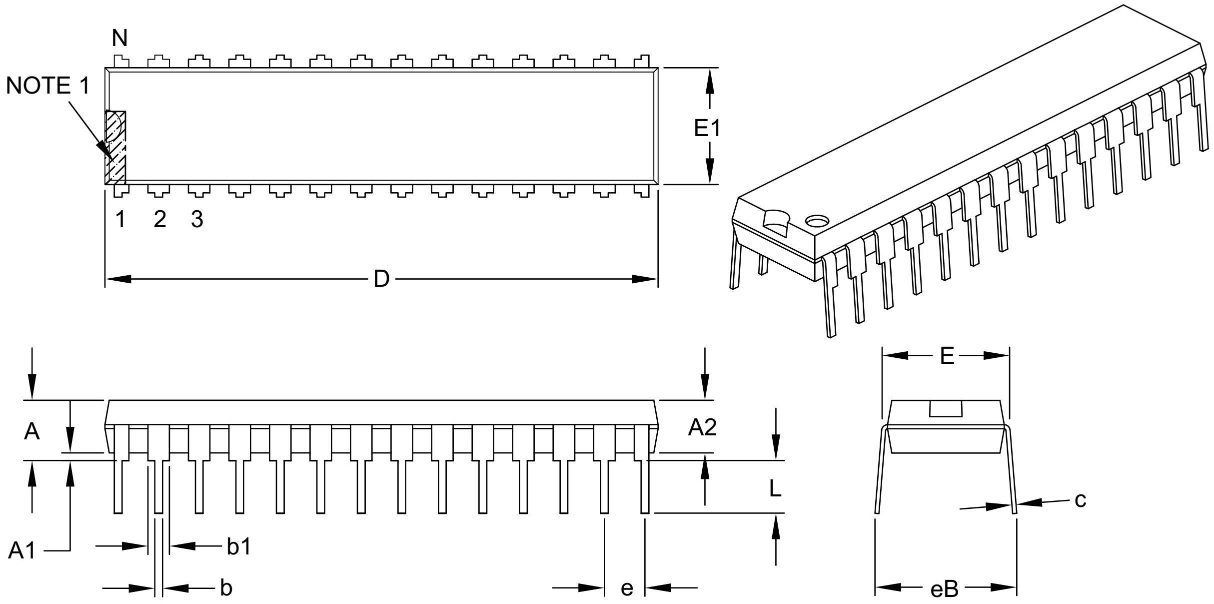
| **AC CHARACTERISTICS** | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics**[1] | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| MSP10 | TSCL | SCKx Output Low Time **(Note 1,2)** | TSCK/2 | — | — | ns | — |
| MSP11 | TSCH | SCKx Output High Time **(Note 1,2)** | TSCK/2 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

### 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|



| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

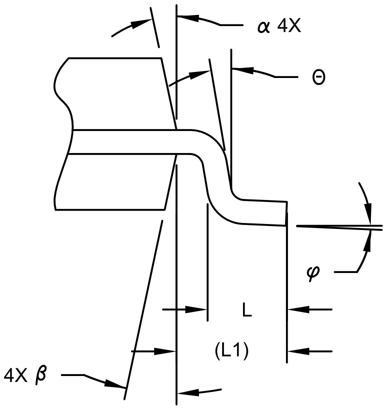
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

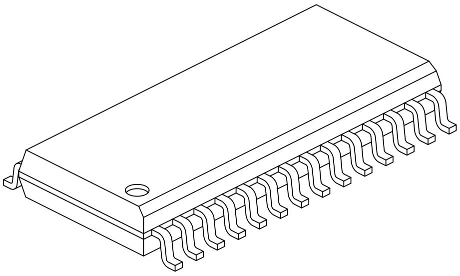
Microchip Technology Drawing C04-070B

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



**VIEW C**



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - |
| Standoff § | A1 | 0.10 | - | 0.30 |
| Overall Width | E | 10.30 BSC | | |
| Molded Package Width | E1 | 7.50 BSC | | |
| Overall Length | D | 17.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.75 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.40 REF | | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.18 | - | 0.33 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

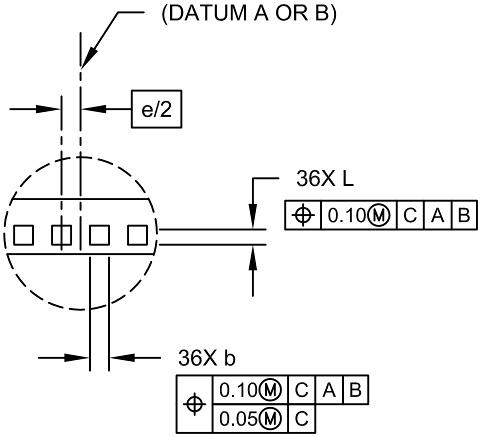
**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

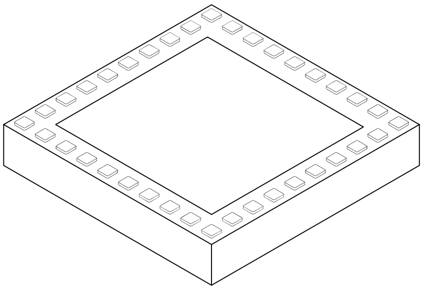
Microchip Technology Drawing C04-052C Sheet 2 of 2

## 36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



**DETAIL A**



| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension | Limits | MIN | NOM | MAX |
| Number of Pins | N | | 36 | |
| Number of Pins per Side | ND | | 10 | |
| Number of Pins per Side | NE | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.025 | - | 0.075 |
| Overall Width | E | | 5.00 BSC | |
| Exposed Pad Width | E2 | 3.60 | 3.75 | 3.90 |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 3.60 | 3.75 | 3.90 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.25 | 0.30 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2

## APPENDIX A: REVISION HISTORY

### Revision A (May 2011)

This is the initial released version of this document.

### Revision B (October 2011)

The following two global changes are included in this revision:

- All packaging references to VLAP have been changed to VTLA throughout the document
- All references to VCORE have been removed
- All occurrences of the ASCL1, ASCL2, ASDA1, and ASDA2 pins have been removed
- V-temp temperature range (-40ºC to +105ºC) was added to all electrical specification tables

This revision includes the addition of the following devices:

- PIC32MX130F064B
- PIC32MX130F064C
- PIC32MX130F064D
- PIC32MX150F128B
- PIC32MX150F128C
- PIC32MX150F128D
- PIC32MX230F064B
- PIC32MX230F064C
- PIC32MX230F064D
- PIC32MX250F128B
- PIC32MX250F128C
- PIC32MX250F128D

Text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-1.

**TABLE A-1: MAJOR SECTION UPDATES**

| Section | Update Description |
|---|---|
| **“**32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog**”** | Split the existing Features table into two: PIC32MX1XX General Purpose Family Features (Table 1) and PIC32MX2XX USB Family Features (Table 2).<br>Added the SPDIP package reference (see Table 1, Table 2, and **“Pin Diagrams”**).<br>Added the new devices to the applicable pin diagrams.<br>Changed PGED2 to PGED1 on pin 35 of the 36-pin VTLA diagram for PIC32MX220F032C, PIC32MX220F016C, PIC32MX230F064C, and PIC32MX250F128C devices. |
| **1.0 “Device Overview”** | Added the SPDIP package reference and updated the pin number for AN12 for 44-pin QFN devices in the Pinout I/O Descriptions (see Table 1-1).<br>Added the PGEC4/PGED4 pin pair and updated the C1INA-C1IND and C2INA-C2IND pin numbers for 28-pin SSOP/SPDIP/SOIC devices in the Pinout I/O Descriptions (see Table 1-1). |
| **2.0 “Guidelines for Getting Started with 32-bit Microcontrollers”** | Updated the Recommended Minimum Connection diagram (see Figure 2-1). |

## Revision D (February 2012)

All occurrences of $V_{USB}$ were changed to: $V_{USB3V3}$. In addition, text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

| Section | Update Description |
|---|---|
| "32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog" | Corrected a part number error in all pin diagrams.<br>Updated the DMA Channels (Programmable/Dedicated) column in the PIC32MX1XX General Purpose Family Features (see Table 1). |
| **1.0 "Device Overview"** | Added the TQFP and VTLA packages to the 44-pin column heading and updated the pin numbers for the SCL1, SCL2, SDA1, and SDA2 pins in the Pinout I/O Descriptions (see Table 1-1). |
| **7.0 "Interrupt Controller"** | Updated the Note that follows the features.<br>Updated the Interrupt Controller Block Diagram (see Figure 7-1). |
| **29.0 "Electrical Characteristics"** | Updated the Maximum values for parameters DC20-DC24, and the Minimum value for parameter DC21 in the Operating Current ($I_{DD}$) DC Characteristics (see Table 29-5).<br>Updated all Minimum and Maximum values for the Idle Current ($I_{IDLE}$) DC Characteristics (see Table 29-6).<br>Updated the Maximum values for parameters DC40k, DC40l, DC40n, and DC40m in the Power-down Current ($I_{PD}$) DC Characteristics (see Table 29-7).<br>Changed the minimum clock period for SCKx from 40 ns to 50 ns in Note 3 of the SPIx Master and Slave Mode Timing Requirements (see Table 29-26 through Table 29-29). |
| **30.0 "DC and AC Device Characteristics Graphs"** | Updated the Typical $I_{IDLE}$ Current @ $V_{DD}$ = 3.3V graph (see Figure 30-5). |