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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

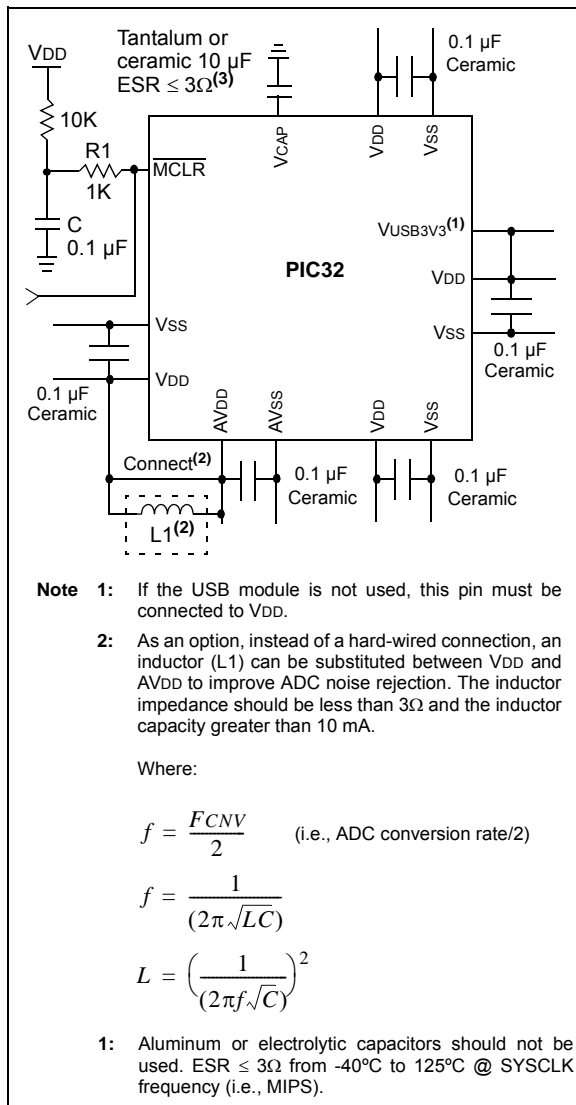
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256d-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256d-i-ml</a>

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION**



## 2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7  $\mu\text{F}$  to 47  $\mu\text{F}$ . This capacitor should be located as close to the device as possible.

## 2.3 Capacitor on Internal Voltage Regulator (VCAP)

### 2.3.1 INTERNAL REGULATOR MODE

A low-ESR (3 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **30.0 "Electrical Characteristics"** for additional information on CEFC specifications.

## 2.4 Master Clear ( $\overline{\text{MCLR}}$ ) Pin

The  $\overline{\text{MCLR}}$  pin provides two specific device functions:

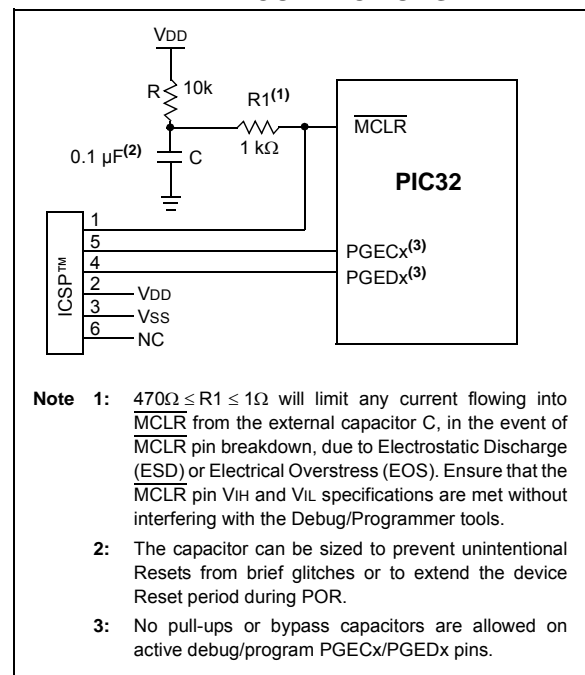
- Device Reset
- Device programming and debugging

Pulling The  $\overline{\text{MCLR}}$  pin low generates a device Reset. Figure 2-2 illustrates a typical  $\overline{\text{MCLR}}$  circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the  $\overline{\text{MCLR}}$  pin. Consequently, specific voltage levels ( $V_{IH}$  and  $V_{IL}$ ) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the  $\overline{\text{MCLR}}$  pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the  $\overline{\text{MCLR}}$  pin.

**FIGURE 2-2: EXAMPLE OF  $\overline{\text{MCLR}}$  PIN CONNECTIONS**



## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDUPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDUPBA<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUPBA<15:10>:** DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** Read-Only bits

This value is always '0', which forces 1 KB increments

- Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.
- 2:** The value in this register must be less than or equal to BMXDRMSZ.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 5.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. “Flash Program Memory”** (DS60001121), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

PIC32MX1XX/2XX 28/36/44-pin Family devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. “Flash Program Memory”** (DS60001121) in the *“PIC32 Family Reference Manual”*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *“PIC32 Flash Programming Specification”* (DS60001145), which can be downloaded from the Microchip web site.

**Note:** The Flash page size on PIC32MX-1XX/2XX 28/36/44-pin Family devices is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)**

Interrupt Source <sup>(1)</sup>	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
			Flag	Enable	Priority	Sub-priority	
U1E – UART1 Fault	39	32	IFS1<7>	IEC1<7>	IPC8<4:2>	IPC8<1:0>	Yes
U1RX – UART1 Receive Done	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>	Yes
U1TX – UART1 Transfer Done	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>	Yes
I2C1B – I2C1 Bus Collision Event	42	33	IFS1<10>	IEC1<10>	IPC8<12:10>	IPC8<9:8>	Yes
I2C1S – I2C1 Slave Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>	Yes
I2C1M – I2C1 Master Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>	Yes
CNA – PORTA Input Change Interrupt	45	34	IFS1<13>	IEC1<13>	IPC8<20:18>	IPC8<17:16>	Yes
CNB – PORTB Input Change Interrupt	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>	Yes
CNC – PORTC Input Change Interrupt	47	34	IFS1<15>	IEC1<15>	IPC8<20:18>	IPC8<17:16>	Yes
PMP – Parallel Master Port	48	35	IFS1<16>	IEC1<16>	IPC8<28:26>	IPC8<25:24>	Yes
PMPE – Parallel Master Port Error	49	35	IFS1<17>	IEC1<17>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2E – SPI2 Fault	50	36	IFS1<18>	IEC1<18>	IPC9<4:2>	IPC9<1:0>	Yes
SPI2RX – SPI2 Receive Done	51	36	IFS1<19>	IEC1<19>	IPC9<4:2>	IPC9<1:0>	Yes
SPI2TX – SPI2 Transfer Done	52	36	IFS1<20>	IEC1<20>	IPC9<4:2>	IPC9<1:0>	Yes
U2E – UART2 Error	53	37	IFS1<21>	IEC1<21>	IPC9<12:10>	IPC9<9:8>	Yes
U2RX – UART2 Receiver	54	37	IFS1<22>	IEC1<22>	IPC9<12:10>	IPC9<9:8>	Yes
U2TX – UART2 Transmitter	55	37	IFS1<23>	IEC1<23>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2B – I2C2 Bus Collision Event	56	38	IFS1<24>	IEC1<24>	IPC9<20:18>	IPC9<17:16>	Yes
I2C2S – I2C2 Slave Event	57	38	IFS1<25>	IEC1<25>	IPC9<20:18>	IPC9<17:16>	Yes
I2C2M – I2C2 Master Event	58	38	IFS1<26>	IEC1<26>	IPC9<20:18>	IPC9<17:16>	Yes
CTMU – CTMU Event	59	39	IFS1<27>	IEC1<27>	IPC9<28:26>	IPC9<25:24>	Yes
DMA0 – DMA Channel 0	60	40	IFS1<28>	IEC1<28>	IPC10<4:2>	IPC10<1:0>	No
DMA1 – DMA Channel 1	61	41	IFS1<29>	IEC1<29>	IPC10<12:10>	IPC10<9:8>	No
DMA2 – DMA Channel 2	62	42	IFS1<30>	IEC1<30>	IPC10<20:18>	IPC10<17:16>	No
DMA3 – DMA Channel 3	63	43	IFS1<31>	IEC1<31>	IPC10<28:26>	IPC10<25:24>	No
Lowest Natural Order Priority							

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX1XX 28/36/44-Pin General Purpose Family Features”** and **TABLE 2: “PIC32MX2XX 28/36/44-pin USB Family Features”** for the lists of available peripherals.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IP03<2:0>			IS03<1:0>	
23:16	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IP02<2:0>			IS02<1:0>	
15:8	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IP01<2:0>			IS01<1:0>	
7:0	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IP00<2:0>			IS00<1:0>	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP03<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

.

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS03<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP02<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

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010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS02<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP01<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

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010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8> <sup>(1,3)</sup>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0> <sup>(1,3)</sup>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON	—	SIDL	OE	RSLP <sup>(2)</sup>	—	DIVSWEN	ACTIVE
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0> <sup>(1)</sup>			

<b>Legend:</b>	HC = Hardware Clearable	HS = Hardware Settable
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits<sup>(1,3)</sup>

The value selects the reference clock divider bits. See Figure 8-1 for information.

bit 15 **ON:** Output Enable bit

1 = Reference Oscillator module is enabled  
0 = Reference Oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode  
0 = Continue module operation when the device enters Idle mode

bit 12 **OE:** Reference Clock Output Enable bit

1 = Reference clock is driven out on REFCLKO pin  
0 = Reference clock is not driven out on REFCLKO pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit<sup>(2)</sup>

1 = Reference Oscillator module output continues to run in Sleep  
0 = Reference Oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit

1 = Divider switch is in progress  
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit

1 = Reference clock request is active  
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

**Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

**2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

**3:** While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

**TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)**

Virtual Address (BF88_#)	Register Name <sup>(f)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	—	0000
31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIHQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3210	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3220	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>**: Channel Source Size bits

1111111111111111 = 65,535 byte source size

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.

.

0000000000000010 = 2 byte source size

0000000000000001 = 1 byte source size

0000000000000000 = 65,536 byte source size

**REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>**: Channel Destination Size bits

1111111111111111 = 65,535 byte destination size

.

.

.

0000000000000010 = 2 byte destination size

0000000000000001 = 1 byte destination size

0000000000000000 = 65,536 byte destination size

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 10-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
	ENDPT<3:0>				DIR	PPBI	—	—

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits  
(Represents the number of the Buffer Descriptor Table, updated by the last USB transfer.)

1111 = Endpoint 15

1110 = Endpoint 14

.

.

.

0001 = Endpoint 1

0000 = Endpoint 0

bit 3 **DIR:** Last Buffer Descriptor Direction Indicator bit

1 = Last transaction was a transmit (TX) transfer

0 = Last transaction was a receive (RX) transfer

bit 2 **PPBI:** Ping-Pong Buffer Descriptor Pointer Indicator bit

1 = The last transaction was to the ODD Buffer Descriptor bank

0 = The last transaction was to the EVEN Buffer Descriptor bank

bit 1-0 **Unimplemented:** Read as '0'

**Note:** The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF (U1IR<3>) bit is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 10-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit

1 = Next token command to be executed at Low-Speed

0 = Next token command to be executed at Full-Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

## REGISTER 10-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON <sup>(1,3)</sup>	—	SIDL <sup>(4)</sup>	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE <sup>(3)</sup>	TCKPS<2:0> <sup>(3)</sup>			T32 <sup>(2)</sup>	—	TCS <sup>(3)</sup>	—

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit<sup>(1,3)</sup>

1 = Module is enabled

0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit<sup>(4)</sup>

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit<sup>(3)</sup>

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits<sup>(3)</sup>

111 = 1:256 prescale value

110 = 1:64 prescale value

101 = 1:32 prescale value

100 = 1:16 prescale value

011 = 1:8 prescale value

010 = 1:4 prescale value

001 = 1:2 prescale value

000 = 1:1 prescale value

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is available only on even numbered timers (Timer2 and Timer4).

**3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.

**4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 14.0 WATCHDOG TIMER (WDT)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog, Deadman, and Power-up Timers”** (DS60001114), which are available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

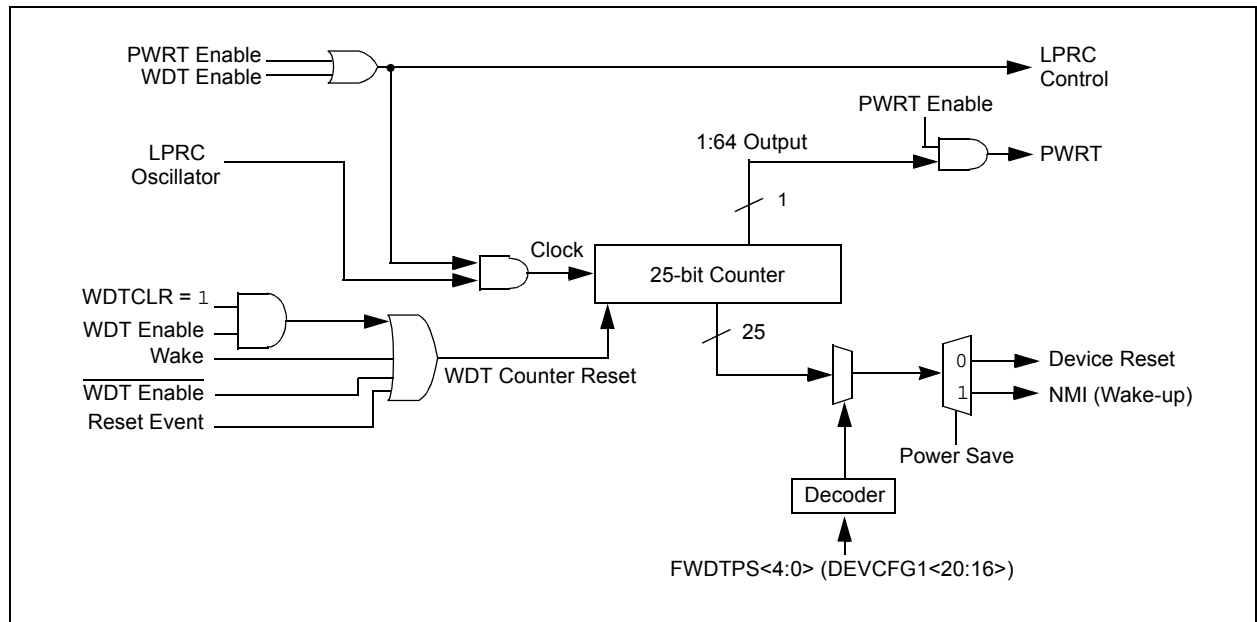
The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle mode

Figure 14-1 illustrates a block diagram of the WDT and Power-up timer.

**FIGURE 14-1: WATCHDOG TIMER AND POWER-UP TIMER BLOCK DIAGRAM**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 16-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON <sup>(1)</sup>	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT <sup>(2)</sup>	OCTSEL	OCM<2:0>		

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit<sup>(1)</sup>

1 = Output Compare peripheral is enabled

0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit

1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source

0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit<sup>(2)</sup>

1 = PWM Fault condition has occurred (cleared in hardware only)

0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit

1 = Timer3 is the clock source for this Output Compare module

0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits

111 = PWM mode on OCx; Fault pin enabled

110 = PWM mode on OCx; Fault pin disabled

101 = Initialize OCx pin low; generate continuous output pulses on OCx pin

100 = Initialize OCx pin low; generate single output pulse on OCx pin

011 = Compare event toggles OCx pin

010 = Initialize OCx pin high; compare event forces OCx pin low

001 = Initialize OCx pin low; compare event forces OCx pin high

000 = Output compare peripheral is disabled but continues to draw current

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

## 17.1 SPI Control Registers

TABLE 17-1: SPI1 AND SPI2 REGISTER MAP

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
5810	SPI1STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5820	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
5830	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>												—	0000
5840	SPI1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000
5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
5A10	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
5A20	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>												—	0000
5A40	SPI2CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 21.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

Following are some of the key features of this module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: day, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range:  $\pm 0.66$  seconds error per month
- Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin

**FIGURE 21-1: RTCC BLOCK DIAGRAM**

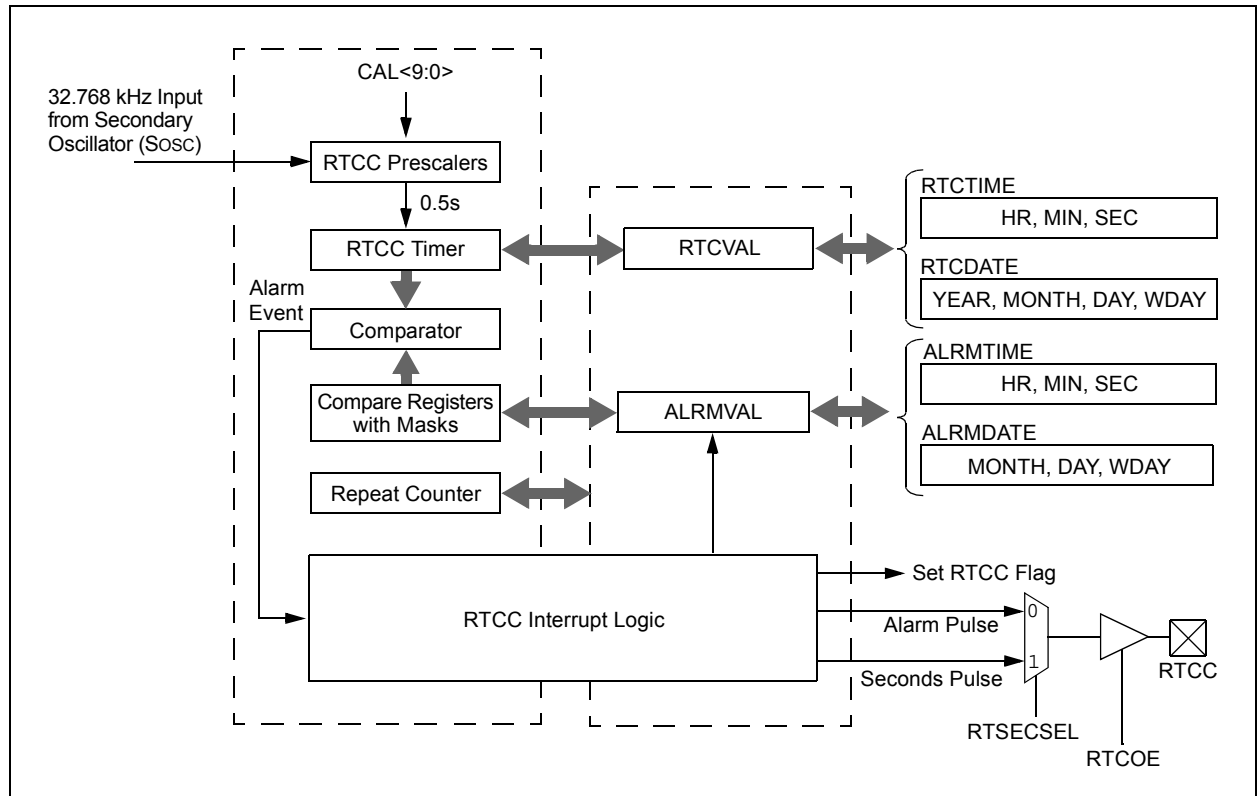


TABLE 22-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9120	ADC1BUFB	31:16	ADC Result Word B (ADC1BUFB<31:0>)																0000
		15:0																	0000
9130	ADC1BUFC	31:16	ADC Result Word C (ADC1BUFC<31:0>)																0000
		15:0																	0000
9140	ADC1BUFD	31:16	ADC Result Word D (ADC1BUFD<31:0>)																0000
		15:0																	0000
9150	ADC1BUFE	31:16	ADC Result Word E (ADC1BUFE<31:0>)																0000
		15:0																	0000
9160	ADC1BUFF	31:16	ADC Result Word F (ADC1BUFF<31:0>)																0000
		15:0																	0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for details.

## 24.1 Comparator Voltage Reference Control Register

**TABLE 24-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP**

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9800	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

- bit 15-14 **FCKSM<1:0>**: Clock Switching and Monitor Selection Configuration bits  
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled  
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled  
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
- bit 13-12 **FPBDIV<1:0>**: Peripheral Bus Clock Divisor Default Value bits  
11 = PBCLK is SYSCLK divided by 8  
10 = PBCLK is SYSCLK divided by 4  
01 = PBCLK is SYSCLK divided by 2  
00 = PBCLK is SYSCLK divided by 1
- bit 11 **Reserved**: Write '1'
- bit 10 **OSCIOFNC**: CLKO Enable Configuration bit  
1 = CLKO output disabled  
0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)
- bit 9-8 **POSCMOD<1:0>**: Primary Oscillator Configuration bits  
11 = Primary Oscillator is disabled  
10 = HS Oscillator mode is selected  
01 = XT Oscillator mode is selected  
00 = External Clock mode is selected
- bit 7 **IESO**: Internal External Switchover bit  
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)  
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)
- bit 6 **Reserved**: Write '1'
- bit 5 **FSOSCEN**: Secondary Oscillator Enable bit  
1 = Enable Secondary Oscillator  
0 = Disable Secondary Oscillator
- bit 4-3 **Reserved**: Write '1'
- bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits  
111 = Fast RC Oscillator with divide-by-N (FRCDIV)  
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler  
101 = Low-Power RC Oscillator (LPRC)  
100 = Secondary Oscillator (Sosc)  
011 = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL)  
010 = Primary Oscillator (XT, HS, EC)<sup>(1)</sup>  
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)  
000 = Fast RC Oscillator (FRC)

**Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 31-5: EXTERNAL CLOCK TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
MOS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	50 50	MHz MHz	EC (Note 2) ECPLL (Note 1)

**Note 1:** PLL input requirements:  $4\text{ MHz} \leq F_{\text{PLLIN}} \leq 5\text{ MHz}$  (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

**2:** This parameter is characterized, but not tested in manufacturing.

**TABLE 31-6: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Tsck/2	—	—	ns	—
MSP11	Tsch	SCKx Output High Time (Note 1,2)	Tsck/2	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

**TABLE 31-7: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typ.	Max.	Units	Conditions
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Tsck/2	—	—	ns	—
MSP11	Tsch	SCKx Output High Time (Note 1,2)	Tsck/2	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 31-8: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
MSP70	TsCL	SCKx Input Low Time ( <b>Note 1,2</b> )	$T_{SCK}/2$	—	—	ns	—
MSP71	TsCH	SCKx Input High Time ( <b>Note 1,2</b> )	$T_{SCK}/2$	—	—	ns	—
MSP51	TssH2boZ	$\overline{SSx}$ $\uparrow$ to SDOx Output High-Impedance ( <b>Note 2</b> )	5	—	25	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns.

**TABLE 31-9: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
SP70	TsCL	SCKx Input Low Time ( <b>Note 1,2</b> )	$T_{SCK}/2$	—	—	ns	—
SP71	TsCH	SCKx Input High Time ( <b>Note 1,2</b> )	$T_{SCK}/2$	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** The minimum clock period for SCKx is 40 ns.