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Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
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256KB (256K x 8)
FLASH
-
16К х 8
2.3V ~ 3.6V
A/D 13x10b
Internal
-40°C ~ 85°C (TA)
Surface Mount
44-TQFP
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		Pin Nu	mber ⁽¹⁾						
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description		
RC0	—	—	3	25	I/O	ST	PORTC is a bidirectional I/O port		
RC1	—	—	4	26	I/O	ST	-		
RC2	—	—	_	27	I/O	ST	7		
RC3	—	—	11	36	I/O	ST			
RC4	—	—		37	I/O	ST			
RC5	—	—	—	38	I/O	ST			
RC6	—	—	_	2	I/O	ST	_		
RC7	—	—		3	I/O	ST	_		
RC8	—	—	_	4	I/O	ST	_		
RC9		-	20	5	1/0	ST			
TICK	9	12	10	34		SI	Timer1 external clock input		
T2CK	PPS	PPS	PPS	PPS		SI	Timer2 external clock input		
TACK	PP3	PP3	PP3	PP3	1	ST ST	Timers external clock input		
T4CK	PPS	PPS	PPS	PPS	1	ST	Timer5 external clock input		
						от ет			
			FF3	FF3	1	31			
	PPS DDS	PPS	PPS	PPS	0				
	PP5	PPS		PPS DDC	1	51			
	PP5	PPS	PP5	PPS	0		UARI1 transmit		
U2CTS	PPS	PPS	PPS	PPS	I	ST	UART2 clear to send		
U2RTS	PPS	PPS	PPS	PPS	0		UART2 ready to send		
U2RX	PPS	PPS	PPS	PPS	I	ST	UART2 receive		
U2TX	PPS	PPS	PPS	PPS	0	—	UART2 transmit		
SCK1	22	25	28	14	I/O	ST	Synchronous serial clock input/output for SPI1		
SDI1	PPS	PPS	PPS	PPS	I	ST	SPI1 data in		
SDO1	PPS	PPS	PPS	PPS	0	_	SPI1 data out		
SS1	PPS	PPS	PPS	PPS	I/O	ST	SPI1 slave synchronization or frame pulse I/O		
SCK2	23	26	29	15	I/O	ST	Synchronous serial clock input/output for SPI2		
SDI2	PPS	PPS	PPS	PPS	I	ST	SPI2 data in		
SDO2	PPS	PPS	PPS	PPS	0	_	SPI2 data out		
SS2	PPS	PPS	PPS	PPS	I/O	ST	SPI2 slave synchronization or frame		
SCL1	14	17	18	44	I/O	ST	Synchronous serial clock input/output for I2C1		
Legend:	CMOS = C	MOS compa	tible input	or output	I	Analog =	Analog input P = Power		
-	ST = Schmi	itt Trigger in	put with CI	MOS levels		O = Outp	but I=Input		
	TTL = TTL input buffer PPS = Peripheral Pin Select — = N/A								

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.



FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX150/250 DEVICES (32 KB RAM, 128 KB FLASH)

2: The size of this memory region is programmable (see Section 3. "Memory Organization" (DS60001115) in the "*PIC32 Family Reference Manual*") and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0						
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0						
23:10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
15:8	—	—	—	—	—	—	CMR	VREGS
	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
7:0	EXTR	SWR	_	WDTO	SLEEP	IDLE	BOR ⁽¹⁾	POR ⁽¹⁾

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Legend:	HS = Set by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-10 Unimplemented: Read as '0'

bit 9	CMR: Configuration Mismatch Reset Flag bit
	1 = Configuration mismatch Reset has occurred
	0 = Configuration mismatch Reset has not occurred
bit 8	VREGS: Voltage Regulator Standby Enable bit
	1 = Regulator is enabled and is on during Sleep mode
	0 = Regulator is disabled and is off during Sleep mode
bit 7	EXTR: External Reset (MCLR) Pin Flag bit
	1 = Master Clear (pin) Reset has occurred
	0 = Master Clear (pin) Reset has not occurred
bit 6	SWR: Software Reset Flag bit
	1 = Software Reset was executed
	0 = Software Reset as not executed
bit 5	Unimplemented: Read as '0'
bit 4	WDTO: Watchdog Timer Time-out Flag bit
	1 = WDT Time-out has occurred
	0 = WDT Time-out has not occurred
bit 3	SLEEP: Wake From Sleep Flag bit
	1 = Device was in Sleep mode
	0 = Device was not in Sleep mode
bit 2	IDLE: Wake From Idle Flag bit
	1 = Device was in Idle mode
	0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit ⁽¹⁾
	1 = Brown-out Reset has occurred
	0 = Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit ⁽¹⁾
	1 = Power-on Reset has occurred
	0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view next detection.

TABLE 10-1: USB REGISTER MAP (CONTINUED)

ess											Bit	s							
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5390	LI1EP9	31:16	—	—	—	—	—	—	-		_	_	—	—	—	-	—	—	0000
0000	UTER 9	15:0	_	—	—	—		—	_	—	_		—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5340		31:16	_	—	—	—	—	—	_	—	_	_	—		_	_	—		0000
5570	UTEL TO	15:0	-	—	_	—	_	_	-	_	_	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0		31:16		_	_	_	_	_		_			_	—			_	—	0000
5560	UILFII	15:0		—	_	_	_	_		_	-	-	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5300		31:16		_	_	_	_	_		_			_	—			_	—	0000
5500	UILF 12	15:0		—	_	_	_	_		_	-	-	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5200		31:16		—	_	_	_	_		_	-	-	—	—		-		—	0000
5500	UILF 13	15:0		—	_	_	_	_		_	-	-	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_	_	_	_	_	_	_	_	_	_	—	_	_	_	—	0000
53E0	UTEP14	15:0	_	_		_			_		_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_		_			_		_	_	_	_	_	_	_	—	0000
53FU	UTEP15	15:0	_						_			-		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

INE OIOT										
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
51.24	—	—	—	—	—	—		—		
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	-	—		
15.9	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15.0	—	—	—	—	—	—		—		
7.0	R/WC-0, HS	U-0	R/WC-0, HS							
7:0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF		VBUSVDIF		

REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable b	pit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-8 Unimplemented: Read as '0'

- bit 7 **IDIF:** ID State Change Indicator bit
 - 1 = A change in the ID state was detected
 - 0 = No change in the ID state was detected
- bit 6 T1MSECIF: 1 Millisecond Timer bit
 - 1 = 1 millisecond timer has expired
 - 0 = 1 millisecond timer has not expired

bit 5 LSTATEIF: Line State Stable Indicator bit

- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms
- bit 4 ACTVIF: Bus Activity Indicator bit
 - 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
 - 0 = Activity has not been detected
- bit 3 SESVDIF: Session Valid Change Indicator bit
 - 1 = VBUS voltage has dropped below the session end level
 - 0 = VBUS voltage has not dropped below the session end level
- bit 2 SESENDIF: B-Device VBUS Change Indicator bit
 - 1 = A change on the session end input was detected
 - 0 = No change on the session end input was detected
- bit 1 Unimplemented: Read as '0'
- bit 0 VBUSVDIF: A-Device VBUS Change Indicator bit
 - 1 = A change on the session valid input was detected
 - 0 = No change on the session valid input was detected

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0				CNT	<7:0>			

REGISTER 10-16: U1SOF: USB SOF THRESHOLD REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-0 CNT<7:0>: SOF Threshold Value bits Typical values of the threshold are:

 - 01001010 = 64-byte packet 00101010 = **32-byte packet**
 - 00011010 = **16-byte packet**
 - 00010010 = 8-byte packet

REGISTER 10-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	-	-	-	-	_
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—					_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—				-	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
7.0			B	DTPTRL<15:9)>			_

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-1 BDTPTRL<15:9>: Buffer Descriptor Table Base Address bits This 7-bit value provides address bits 15 through 9 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

bit 0 Unimplemented: Read as '0'

11.1 Parallel I/O (PIO) Ports

All port pins have 10 registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the **"Pin Diagrams"** section for the available pins and their functionality.

11.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP.

11.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MX1XX/2XX 28/36/44-pin Family devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

An additional control register (CNCONx) is shown in Register 11-3.

11.2 CLR, SET and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR, or INV register, the base register must be read.

INPUT CAPTURE 15.0

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 15. "Input Capture" (DS60001122), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- · Simple capture event modes:
 - Capture timer value on every rising and falling edge of input at ICx pin
 - Capture timer value on every edge (rising and falling)
 - Capture timer value on every edge (rising and falling), specified edge first.

- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- · Device wake-up from capture pin during Sleep and Idle modes
- · Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- · Input capture can also be used to provide additional sources of external interrupts

Figure 15-1 illustrates a general block diagram of the Input Capture module.



REGISTER 15-1: ICXCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

ICM<2:0>: Input Capture Mode Select bits

bit 2-0

- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode every sixteenth rising edge
- 100 = Prescaled Capture Event mode every fourth rising edge
- 011 = Simple Capture Event mode every rising edge
- 010 = Simple Capture Event mode every falling edge
- 001 = Edge Detect mode every edge (rising and falling)
- 000 = Input Capture module is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	ADRML	JX<1:0>	PMPTTL	PTWREN	PTRDEN
	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7:0	CSF<1:0>(2)		ALP ⁽²⁾	_	CS1P ⁽²⁾	_	WRSP	RDSP

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾
 - 1 = PMP enabled
 - 0 = PMP disabled, no off-chip access performed
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when the device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode
- bit 12-11 ADRMUX<1:0>: Address/Data Multiplexing Selection bits
 - 11 = Lower 8 bits of address are multiplexed on PMD<7:0> pins; upper 8 bits are not used
 - 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
 - 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<10:8> and PMA<14>
 - 00 = Address and data appear on separate pins
- bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
 - 1 = PMP module uses TTL input buffers
 - 0 = PMP module uses Schmitt Trigger input buffer
- bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
 - 1 = PMWR/PMENB port enabled
 - 0 = PMWR/PMENB port disabled
- bit 8 PTRDEN: Read/Write Strobe Port Enable bit
 - 1 = PMRD/PMWR port enabled
 - 0 = PMRD/PMWR port disabled
- bit 7-6 CSF<1:0>: Chip Select Function bits⁽²⁾
 - 11 = Reserved
 - 10 = PMCS1 functions as Chip Select
 - 01 = PMCS1 functions as PMA<14>
 - 00 = PMCS1 functions as PMA<14>
- bit 5 ALP: Address Latch Polarity bit⁽²⁾
 - 1 = Active-high (PMALL and PMALH)
 - $0 = \text{Active-low} (\overline{\text{PMALL}} \text{ and } \overline{\text{PMALH}})$
 - **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - 2: These bits have no effect when their corresponding pins are used as address lines.

21.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time. Following are some of the key features of this module:

- · Time: hours, minutes and seconds
- 24-hour format (military time)
- · Visibility of one-half second period
- · Provides calendar: day, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- · Alarm repeat with decrementing counter
- · Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap vear correction
- · BCD format for smaller firmware overhead
- · Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- · Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	HR10)<1:0>	HR01<3:0>			
23:16	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	MIN10<2:0>			MIN01<3:0>			
45.0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15:8	—		SEC10<2:0>		SEC01<3:0>			
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	—	—	—	—	_	_	_	_
		•						
l egend.								

REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

bit 29-28 HR10<1:0>: Binary Coded Decimal value of hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9 bit 23 **Unimplemented:** Read as '0'

bit 22-20 MIN10<2:0>: Binary Coded Decimal value of minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9 bit 15 **Unimplemented:** Read as '0'

bit 14-12 SEC10<2:0>: Binary Coded Decimal value of seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 Unimplemented: Read as '0'

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0						
31.24	—	—	—	—	—		—	_
00.40	U-0	U-0						
23:10	-	—	—	—	—		—	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	F	ORM<2:0>	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
7.0		SSRC<2:0>		CLRASAM		ASAM	SAMP ⁽²⁾	DONE ⁽³⁾

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit⁽¹⁾
 - 1 = ADC module is operating
 - 0 = ADC module is not operating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode

bit 12-11 Unimplemented: Read as '0'

- bit 10-8 **FORM<2:0>:** Data Output Format bits
 - 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
 - 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
 - 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
 - 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
 - 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
 - 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)

 - 000 =Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	—	_	—	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	_	—	—	—	—	—	_	—
45.0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
15:8	—	—	IOLOCK ⁽¹⁾	PMDLOCK ⁽¹⁾	—	—		_
7.0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-1	R/W-1
7:0	—	_	_	_	JTAGEN	_		TDOEN

REGISTER 27-5: CFGCON: CONFIGURATION CONTROL REGISTER

Legend:

Logonan			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

- bit 13 IOLOCK: Peripheral Pin Select Lock bit⁽¹⁾
 - 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
 - 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.
- bit 12 PMDLOCK: Peripheral Module Disable bit⁽¹⁾
 - 1 = Peripheral module is locked. Writes to PMD registers is not allowed.
 - 0 = Peripheral module is not locked. Writes to PMD registers is allowed.

bit 11-4 Unimplemented: Read as '0'

- bit 3 JTAGEN: JTAG Port Enable bit
 - 1 = Enable the JTAG port
 - 0 = Disable the JTAG port
- bit 2-1 Unimplemented: Read as '1'
- bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG bit
 - 1 = 2-wire JTAG protocol uses TDO
 - 0 = 2-wire JTAG protocol does not use TDO
- Note 1: To change this bit, the unlock sequence must be performed. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

TABLE 30-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARA	CTERISTICS	5	Standard Op (unless other Operating terr	erating Conditions: 2.3V to rwise stated) nperature $-40^{\circ}C \le TA \le +85^{\circ}$ $-40^{\circ}C \le TA \le +103^{\circ}$	3.6V ² C for Industrial 5°C for V-temp	
Parameter No.	Typical ⁽³⁾	Max.	Units Conditions			
Operating Current (IDD) (Notes 1, 2, 5)						
DC20	2	3	mA	4 MH	lz (Note 4)	
DC21	7	10.5	mA	1	0 MHz	
DC22	10	15	mA	20 Mł	Hz (Note 4)	
DC23	15	23	mA	30 MI	Hz (Note 4)	
DC24	20	30	mA	40 MHz		
DC25	100	150	μA	+25°C, 3.3V LPRC (31 kHz) (Note 4)		

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

- 2: The test conditions for IDD measurements are as follows:
 - Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
 - · WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - · All I/O pins are configured as inputs and pulled to Vss
 - MCLR = VDD
 - CPU executing while(1) statement from Flash
 - RTCC and JTAG are disabled
- **3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

DC CHARACTERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DO10	Vol	Output Low Voltage	_	_	0.4	V	$\text{Iol} \leq 10 \text{ mA}, \text{ Vdd} = 3.3 \text{V}$
		Output High Voltage	1.5 ⁽¹⁾	_	_		IOH \ge -14 mA, VDD = 3.3V
020	Мон	I/O Pins	2.0 ⁽¹⁾	—	—	V	IOH \ge -12 mA, VDD = 3.3V
D020	VOH		2.4	_	_	v	Ioh \geq -10 mA, Vdd = 3.3V
			3.0(1)	_	_		$IOH \ge -7 \text{ mA}, \text{ VDD} = 3.3 \text{V}$

TABLE 30-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized, but not tested.

TABLE 30-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min. ⁽¹⁾	Typical	Max.	Units	Conditions	
BO10	VBOR	BOR Event on VDD transition high-to-low ⁽²⁾	2.0		2.3	V	_	

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

АС СНА	AC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 4): 2.5V to 3.6V \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
Clock P	arameter	S					
AD50	TAD	ADC Clock Period ⁽²⁾	65	_	_	ns	See Table 30-35
Conver	sion Rate						
AD55	TCONV	Conversion Time	—	12 Tad	—		—
AD56	AD56 FCNV Throughput Rate			—	1000	ksps	AVDD = 3.0V to 3.6V
	(Sampling Speed)	(Sampling Speed)		—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1 Tad	—	—	_	TSAMP must be \geq 132 ns
Timing	Paramete	rs					
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾	_	1.0 Tad	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 Tad	_	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽³⁾	—	0.5 TAD	—	_	_
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽³⁾	_	—	2	μS	_

TABLE 30-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.







44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]





Microchip Technology Drawing C04-157C Sheet 1 of 2

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section	Update Description				
4.0 "Memory Organization"	Added Memory Maps for the new devices (see Figure 4-3 and Figure 4-4).				
	Removed the BMXCHEDMA bit from the Bus Matrix Register map (see Table 4-1).				
	Added the REFOTRIM register, added the DIVSWEN bit to the REFOCON registers, added Note 4 to the ULOCK and SOSCEN bits and added the PBDIVRDY bit in the OSCCON register in the in the System Control Register map (see Table 4-16).				
	Removed the ALTI2C1 and ALTI2C2 bits from the DEVCFG3 register and added Note 1 to the UPLLEN and UPLLIDIV<2:0> bits of the DEVCFG2 register in the Device Configuration Word Summary (see Table 4-17).				
	Updated Note 1 in the Device and Revision ID Summary (see Table 4-18).				
	Added Note 2 to the PORTA Register map (see Table 4-19).				
	Added the ANSB6 and ANSB12 bits to the ANSELB register in the PORTB Register map (see Table 4-20).				
	Added Notes 2 and 3 to the PORTC Register map (see Table 4-21).				
	Updated all register names in the Peripheral Pin Select Register map (see Table 4-23).				
	Added values in support of new devices (16 KB RAM and 32 KB RAM) in the Data RAM Size register (see Register 4-5).				
	Added values in support of new devices (64 KB Flash and 128 KB Flash) in the Data RAM Size register (see Register 4-5).				
8.0 "Oscillator Configuration"	Added Note 5 to the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1).				
	Added the PBDIVRDY bit and Note 2 to the Oscillator Control register (see Register 8-1).				
	Added the DIVSWEN bit and Note 3 to the Reference Oscillator Control register (see Register 8-3).				
	Added the REFOTRIM register (see Register 8-4).				
21.0 "10-bit Analog-to-Digital	Updated the ADC1 Module Block Diagram (see Figure 21-1).				
Converter (ADC)"	Updated the Notes in the ADC Input Select register (see Register 21-4).				
24.0 "Charge Time Measurement	Updated the CTMU Block Diagram (see Figure 24-1).				
	Added Note 3 to the CTMU Control register (see Register 24-1)				
26.0 "Special Features"	Added Note 1 and the PGEC4/PGED4 pin pair to the ICESEL<1:0> bits in DEVCFG0: Device Configuration Word 0 (see Register 26-1).				
	Removed the ALTI2C1 and ALTI2C2 bits from the Device Configuration Word 3 register (see Register 26-4).				
	Removed 26.3.3 "Power-up Requirements".				
	Added Note 3 to the Connections for the On-Chip Regulator diagram (see Figure 26-2).				
	Updated the Block Diagram of Programming, Debugging and Trace Ports diagram (see Figure 26-3).				