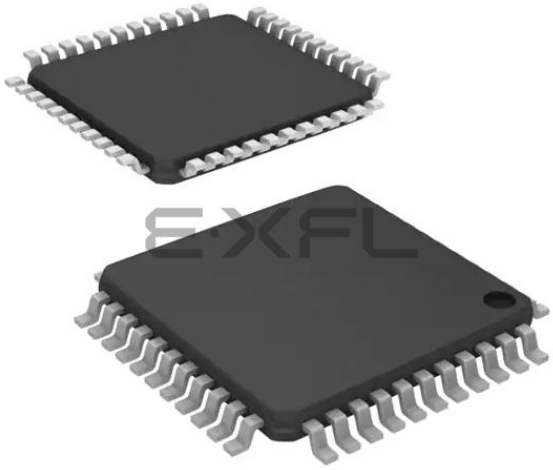
# Microchip Technology - PIC32MX230F256DT-50I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 13x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256dt-50i-pt |

**TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES**

**28-PIN QFN (TOP VIEW)(1,2,3,4)**

**PIC32MX210F016B**
**PIC32MX220F032B**
**PIC32MX230F064B**
**PIC32MX230F256B**
**PIC32MX250F128B**
**PIC32MX270F256B**

28 1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 | 15 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 | 16 | VSS |
| 3 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 | 17 | VCAP |
| 4 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 | 18 | PGED2/RPB10/D+/CTED11/RB10 |
| 5 | VSS | 19 | PGEC2/RPB11/D-/RB11 |
| 6 | OSC1/CLKI/RPA2/RA2 | 20 | VUSB3V3 |
| 7 | OSC2/CLKO/RPA3/PMA0/RA3 | 21 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 8 | SOSCI/RPB4/RB4 | 22 | CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14 |
| 9 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 23 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 10 | VDD | 24 | AVSS |
| 11 | TMS/RPB5/USBID/RB5 | 25 | AVDD |
| 12 | VBUS | 26 | $\overline{\text{MCLR}}$ |
| 13 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 27 | PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 |
| 14 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 28 | PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** Shaded pins are 5V tolerant.

## 1.0 DEVICE OVERVIEW

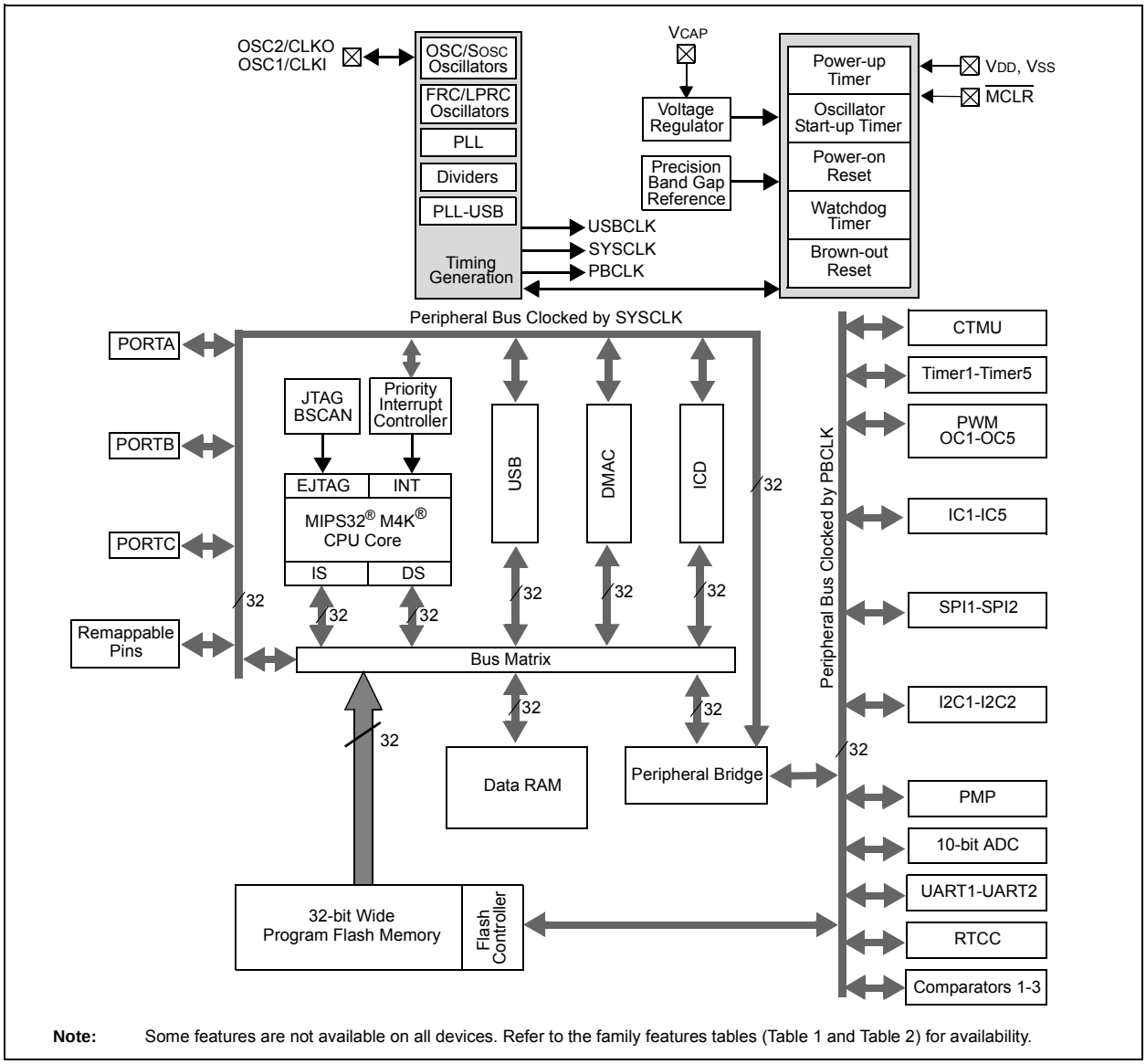
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX1XX/2XX 28/36/44-pin Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/36/44-pin Family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: BLOCK DIAGRAM**




**Note:** Some features are not available on all devices. Refer to the family features tables (Table 1 and Table 2) for availability.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number[1] | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| USBID | 11[3] | 14[3] | 15[3] | 41[3] | I | ST | USB OTG ID detect |
| CTED1 | 27 | 2 | 33 | 19 | I | ST | CTMU External Edge Input |
| CTED2 | 28 | 3 | 34 | 20 | I | ST | |
| CTED3 | 13 | 16 | 17 | 43 | I | ST | |
| CTED4 | 15 | 18 | 19 | 1 | I | ST | |
| CTED5 | 22 | 25 | 28 | 14 | I | ST | |
| CTED6 | 23 | 26 | 29 | 15 | I | ST | |
| CTED7 | — | — | 20 | 5 | I | ST | |
| CTED8 | — | — | — | 13 | I | ST | |
| CTED9 | 9 | 12 | 10 | 34 | I | ST | |
| CTED10 | 14 | 17 | 18 | 44 | I | ST | |
| CTED11 | 18 | 21 | 24 | 8 | I | ST | |
| CTED12 | 2 | 5 | 36 | 22 | I | ST | |
| CTED13 | 3 | 6 | 1 | 23 | I | ST | |
| CTPLS | 21 | 24 | 27 | 11 | O | — | CTMU Pulse Output |
| PGED1 | 1 | 4 | 35 | 21 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 1 |
| PGEC1 | 2 | 5 | 36 | 22 | I | ST | Clock input pin for Programming/Debugging Communication Channel 1 |
| PGED2 | 18 | 21 | 24 | 8 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 2 |
| PGEC2 | 19 | 22 | 25 | 9 | I | ST | Clock input pin for Programming/Debugging Communication Channel 2 |
| PGED3 | 11[2] | 14[2] | 15[2] | 41[2] | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 3 |
| | 27[3] | 2[3] | 33[3] | 19[3] | | | |
| PGEC3 | 12[2] | 15[2] | 16[2] | 42[2] | I | ST | Clock input pin for Programming/ Debugging Communication Channel 3 |
| | 28[3] | 3[3] | 34[3] | 20[3] | | | |
| PGED4 | — | — | 3 | 12 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 4 |
| PGEC4 | — | — | 4 | 13 | I | ST | Clock input pin for Programming/ Debugging Communication Channel 4 |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

**Note 1:** Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)**

bit 9-8 **IS01<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP00<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS00<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

| **Note:** | This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions. |
|---|---|

**REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | RODIV<14:8>(1,3) | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RODIV<7:0>(1,3) | | | | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0, HC | R-0, HS, HC |
| | ON | — | SIDL | OE | RSLP(2) | — | DIVSWEN | ACTIVE |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | ROSEL<3:0>(1) | | | |

| Legend: | HC = Hardware Clearable | HS = Hardware Settable | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits(1,3)

The value selects the reference clock divider bits. See Figure 8-1 for information.

bit 15 **ON:** Output Enable bit

1 = Reference Oscillator module is enabled
0 = Reference Oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode

bit 12 **OE:** Reference Clock Output Enable bit

1 = Reference clock is driven out on REFCLKO pin
0 = Reference clock is not driven out on REFCLKO pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)

1 = Reference Oscillator module output continues to run in Sleep
0 = Reference Oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit

1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit

1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

**Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

**2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

**3:** While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

## 10.0 USB ON-THE-GO (OTG)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 Full-Speed and Low-Speed embedded host, Full-Speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 10-1.

The clock generator provides the 48 MHz clock required for USB Full-Speed and Low-Speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32 USB module includes the following features:

- USB Full-Speed support for Host and Device
- Low-Speed Host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

**Note:** The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc., also referred to as USB-IF (www.usb.org). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

**REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS |
| | BTSEF | BMXEF | DMAEF(1) | BTOEF(2) | DFN8EF | CRC16EF | CRC5EF(4) / EOFEF(3,5) | PIDEF |

| Legend: | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit
- 1 = Packet rejected due to bit stuff error
- 0 = Packet accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
- 1 = The base address, of the Buffer Descriptor Table, or the address of an individual buffer pointed to by a Buffer Descriptor Table entry, is invalid.
- 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit(1)
- 1 = USB DMA error condition detected
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit(2)
- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit
- 1 = Data field received is not an integral number of bytes
- 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
- 1 = Data packet rejected due to CRC16 error
- 0 = Data packet accepted

**Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

**2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

**3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

**4:** Device mode.

**5:** Host mode.

**REGISTER 10-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BDTPTRH<23:16> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

**REGISTER 10-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BDTPTRU<31:24> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

## 15.0 INPUT CAPTURE

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
  - Capture timer value on every rising and falling edge of input at ICx pin
  - Capture timer value on every edge (rising and falling)
  - Capture timer value on every edge (rising and falling), specified edge first.
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

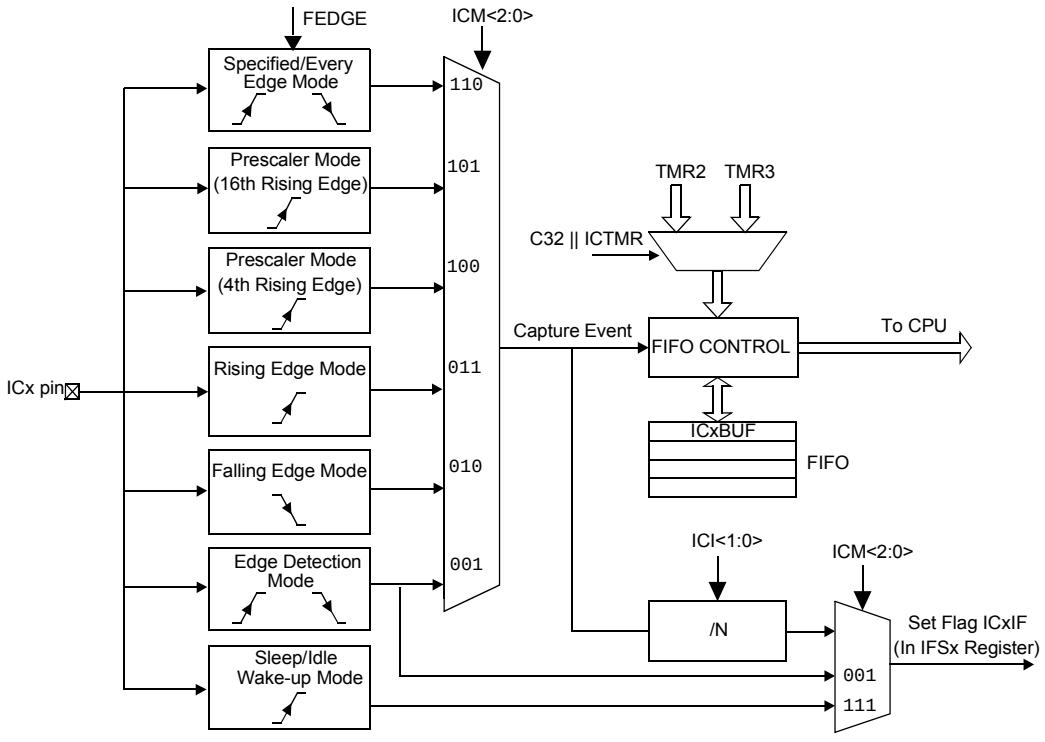
Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- Input capture can also be used to provide additional sources of external interrupts

Figure 15-1 illustrates a general block diagram of the Input Capture module.

**FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM**




**Note:** An 'x' in a signal, register or bit name denotes the number of the capture channel.

**REGISTER 16-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | OC32 | OCFLT(2) | OCTSEL | OCM<2:0> | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit(1)
- 1 = Output Compare peripheral is enabled
- 0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(2)
- 1 = PWM Fault condition has occurred (cleared in hardware only)
- 0 = No PWM Fault condition has occurred

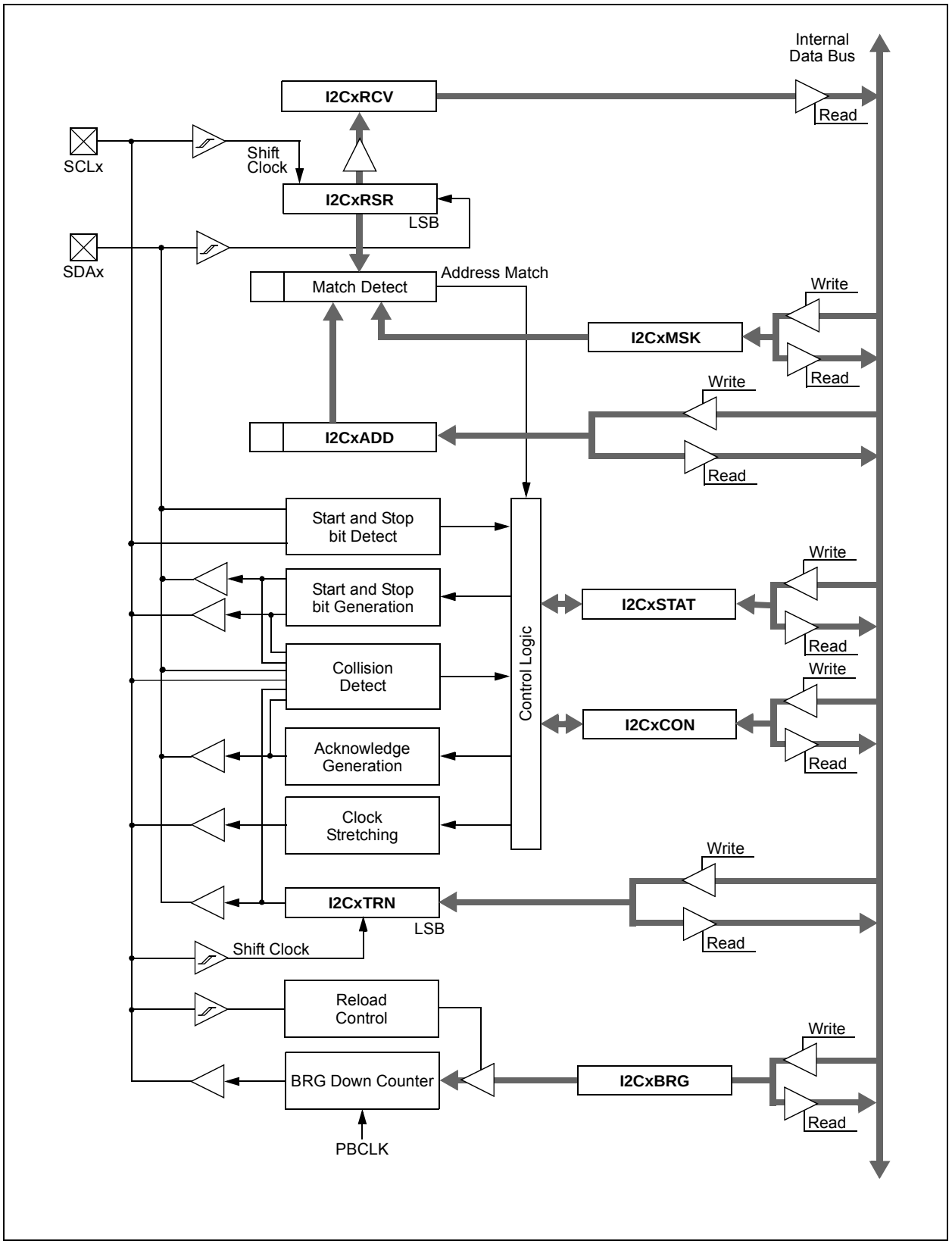
bit 3 **OCTSEL:** Output Compare Timer Select bit
- 1 = Timer3 is the clock source for this Output Compare module
- 0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

**FIGURE 18-1: I²C BLOCK DIAGRAM**



**NOTES:**

**REGISTER 20-4: PMAEN: PARALLEL PORT PIN ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | PTEN14 | — | — | — | PTEN<10:8> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTEN<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 15-14 **PTEN14:** PMCS1 Address Port Enable bits
- 1 = PMA14 functions as either PMA14 or PMCS1(1)
- 0 = PMA14 functions as port I/O

bit 13-11 **Unimplemented:** Read as '0'

bit 10-2 **PTEN<10:2>:** PMP Address Port Enable bits
- 1 = PMA<10:2> function as PMP address lines
- 0 = PMA<10:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits
- 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)
- 0 = PMA1 and PMA0 pads functions as port I/O

**Note 1:** The use of this pin as PMA14 or CS1 is selected by the CSF<1:0> bits in the PMCON register.

**2:** The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by bits ADRMUX<1:0> in the PMCON register.

**REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EDG1MOD | EDG1POL | EDG1SEL<3:0> | | | | EDG2STAT | EDG1STAT |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | EDG2MOD | EDG2POL | EDG2SEL<3:0> | | | | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON | — | CTMUSIDL | TGEN(1) | EDGEN | EDGSEQEN | IDISSEN(2) | CTTRIG |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ITRIM<5:0> | | | | | | IRNG<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **EDG1MOD:** Edge1 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge1 programmed for a positive edge response
0 = Edge1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = C3OUT pin is selected
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = IC3 Capture Event is selected
1011 = IC2 Capture Event is selected
1010 = IC1 Capture Event is selected
1001 = CTED8 pin is selected
1000 = CTED7 pin is selected
0111 = CTED6 pin is selected
0110 = CTED5 pin is selected
0101 = CTED4 pin is selected
0100 = CTED3 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 25 **EDG2STAT:** Edge2 Status bit
Indicates the status of Edge2 and can be written to control edge source
1 = Edge2 has occurred
0 = Edge2 has not occurred

**Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

**2:** The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**3:** Refer to the CTMU Current Source Specifications (Table 30-41) in **Section 30.0 "Electrical Characteristics"** for current values.

**4:** This bit setting is not available for the CTMU temperature diode.

## 27.2 Configuration Registers

### TABLE 27-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

| Virtual Address (BFC0_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0BF0 | DEVCFG3 | 31:16 | FVBUSONIO | FUSBIDIO | IOL1WAY | PMDL1WAY | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | USERID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 0BF4 | DEVCFG2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | FPLLODIV<2:0> | | | xxxx |
| | | 15:0 | UPLLEN(1) | — | — | — | — | UPLLIDIV<2:0>(1) | | | — | FPLLMUL<2:0> | | | — | FPLLIDIV<2:0> | | | xxxx |
| 0BF8 | DEVCFG1 | 31:16 | — | — | — | — | — | — | FWDTWINSZ<1:0> | | FWDTEN | WINDIS | — | WDTPS<4:0> | | | | | xxxx |
| | | 15:0 | FCKSM<1:0> | | FPBDIV<1:0> | | — | OSCIOFNC | POSCMOD<1:0> | | IESO | — | FSOSCEN | — | — | FNOSC<2:0> | | | xxxx |
| 0BFC | DEVCFG0 | 31:16 | — | — | — | CP | — | — | — | BWP | — | — | — | — | — | PWP<8:6>(2) | | | xxxx |
| | | 15:0 | PWP<5:0> | | | | | | — | — | — | — | — | ICESEL<1:0> | | JTAGEN | DEBUG<1:0> | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is only available on PIC32MX2XX devices.

**2:** PWP<8:7> are only available on devices with 256 KB of Flash.

### TABLE 27-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F220 | DEVID | 31:16 | VER<3:0> | | | | DEVID<27:16> | | | | | | | | | | | | xxxx(1) |
| | | 15:0 | DEVID<15:0> | | | | | | | | | | | | | | | | xxxx(1) |
| F200 | CFGCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | IOLOCK | PMDLOCK | — | — | — | — | — | — | — | — | JTAGEN | — | — | TDOEN | 000B |
| F230 | SYSKEY(3) | 31:16 | SYSKEY<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Reset values are dependent on the device variant.

**TABLE 30-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP51 | TSSH2DOZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)** | 5 | — | 25 | ns | — |
| SP52 | TSCH2SSH<br>TSCL2SSH | $\overline{SSx}$ ↑ after SCKx Edge | TSCK + 20 | — | — | ns | — |
| SP60 | TSSL2DOV | SDOx Data Output Valid after $\overline{SSx}$ Edge | — | — | 25 | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

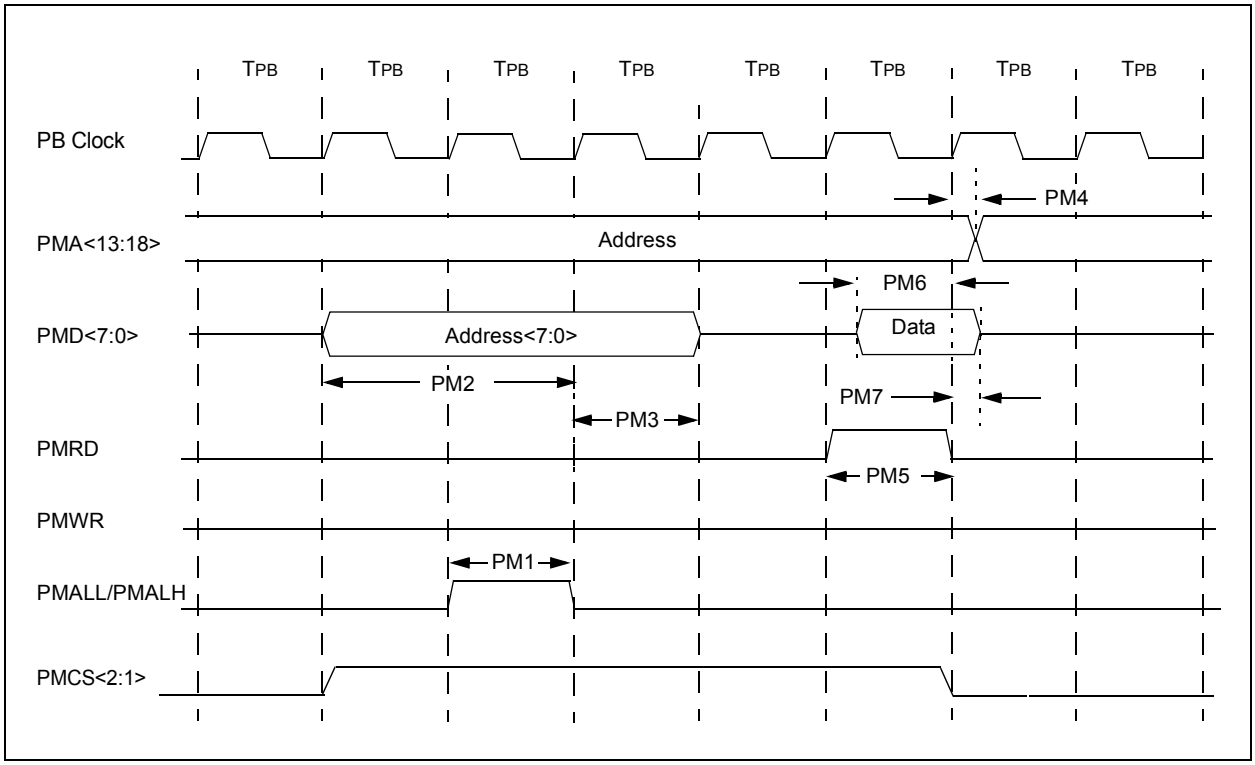
**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 30-37: PARALLEL SLAVE PORT REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param.No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PS1 | TdtV2wrH | Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time) | 20 | — | — | ns | — |
| PS2 | TwrH2dtI | $\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time) | 40 | — | — | ns | — |
| PS3 | TrdL2dtV | $\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid | — | — | 60 | ns | — |
| PS4 | TrdH2dtI | $\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid | 0 | — | 10 | ns | — |
| PS5 | Tcs | $\overline{CS}$ Active Time | TPB + 40 | — | — | ns | — |
| PS6 | TWR | $\overline{WR}$ Active Time | TPB + 25 | — | — | ns | — |
| PS7 | TRD | $\overline{RD}$ Active Time | TPB + 25 | — | — | ns | — |

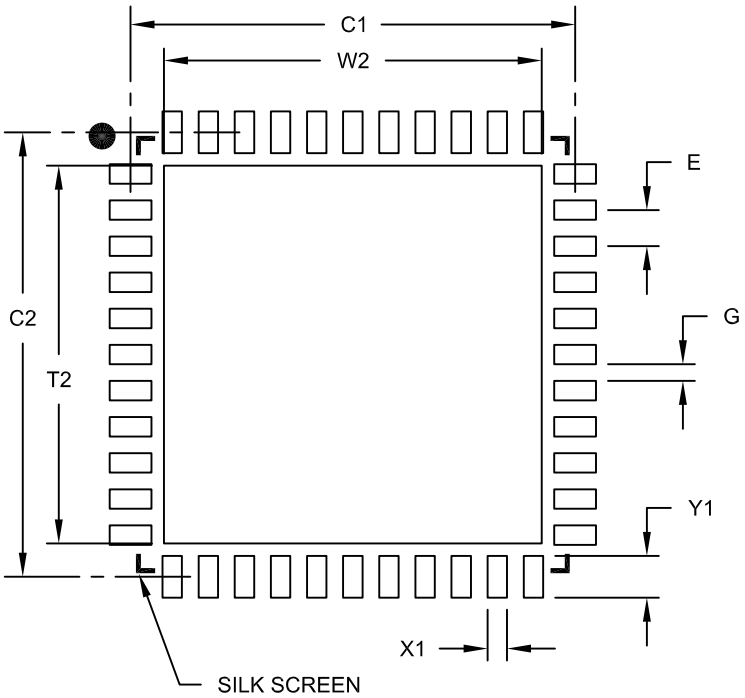
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 30-21: PARALLEL MASTER PORT READ TIMING DIAGRAM**



### 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 6.80 |
| Optional Center Pad Length | T2 | | | 6.80 |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Width (X44) | X1 | | | 0.35 |
| Contact Pad Length (X44) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section | Update Description |
|---|---|
| **4.0 "Memory Organization"** | Added Memory Maps for the new devices (see Figure 4-3 and Figure 4-4).<br>Removed the BMXCHEDMA bit from the Bus Matrix Register map (see Table 4-1).<br>Added the REFOTRIM register, added the DIVSWEN bit to the REFOCON registers, added Note 4 to the ULOCK and SOSCEN bits and added the PBDIVRDY bit in the OSCCON register in the in the System Control Register map (see Table 4-16).<br>Removed the ALTI2C1 and ALTI2C2 bits from the DEVCFG3 register and added Note 1 to the UPLLEN and UPLLIDIV<2:0> bits of the DEVCFG2 register in the Device Configuration Word Summary (see Table 4-17).<br>Updated Note 1 in the Device and Revision ID Summary (see Table 4-18).<br>Added Note 2 to the PORTA Register map (see Table 4-19).<br>Added the ANSB6 and ANSB12 bits to the ANSELB register in the PORTB Register map (see Table 4-20).<br>Added Notes 2 and 3 to the PORTC Register map (see Table 4-21).<br>Updated all register names in the Peripheral Pin Select Register map (see Table 4-23).<br>Added values in support of new devices (16 KB RAM and 32 KB RAM) in the Data RAM Size register (see Register 4-5).<br>Added values in support of new devices (64 KB Flash and 128 KB Flash) in the Data RAM Size register (see Register 4-5). |
| **8.0 "Oscillator Configuration"** | Added Note 5 to the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1).<br>Added the PBDIVRDY bit and Note 2 to the Oscillator Control register (see Register 8-1).<br>Added the DIVSWEN bit and Note 3 to the Reference Oscillator Control register (see Register 8-3).<br>Added the REFOTRIM register (see Register 8-4). |
| **21.0 "10-bit Analog-to-Digital Converter (ADC)"** | Updated the ADC1 Module Block Diagram (see Figure 21-1).<br>Updated the Notes in the ADC Input Select register (see Register 21-4). |
| **24.0 "Charge Time Measurement Unit (CTMU)"** | Updated the CTMU Block Diagram (see Figure 24-1).<br>Added Note 3 to the CTMU Control register (see Register 24-1) |
| **26.0 "Special Features"** | Added Note 1 and the PGEC4/PGED4 pin pair to the ICESEL<1:0> bits in DEVCFG0: Device Configuration Word 0 (see Register 26-1).<br>Removed the ALTI2C1 and ALTI2C2 bits from the Device Configuration Word 3 register (see Register 26-4).<br>Removed 26.3.3 "Power-up Requirements".<br>Added Note 3 to the Connections for the On-Chip Regulator diagram (see Figure 26-2).<br>Updated the Block Diagram of Programming, Debugging and Trace Ports diagram (see Figure 26-3). |

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