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Details

| | |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status | Obsolete |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 13x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VFTLA Exposed Pad |
| Supplier Device Package | 44-VTLA (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256dt-50i-tl |

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS

| Pin Name | Pin Number ⁽¹⁾ | | | | Pin Type | Buffer Type | Description |
|----------|---------------------------|--------------------------|----------------------------------------|----------------------------------------|----------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| AN0 | 27 | 2 | 33 | 19 | I | Analog | Analog input channels. |
| AN1 | 28 | 3 | 34 | 20 | I | Analog | |
| AN2 | 1 | 4 | 35 | 21 | I | Analog | |
| AN3 | 2 | 5 | 36 | 22 | I | Analog | |
| AN4 | 3 | 6 | 1 | 23 | I | Analog | |
| AN5 | 4 | 7 | 2 | 24 | I | Analog | |
| AN6 | — | — | 3 | 25 | I | Analog | |
| AN7 | — | — | 4 | 26 | I | Analog | |
| AN8 | — | — | — | 27 | I | Analog | |
| AN9 | 23 | 26 | 29 | 15 | I | Analog | |
| AN10 | 22 | 25 | 28 | 14 | I | Analog | |
| AN11 | 21 | 24 | 27 | 11 | I | Analog | |
| AN12 | 20 ⁽²⁾ | 23 ⁽²⁾ | 26 ⁽²⁾ 11 ⁽³⁾ | 10 ⁽²⁾ 36 ⁽³⁾ | I | Analog | |
| CLKI | 6 | 9 | 7 | 30 | I | ST/CMOS | External clock source input. Always associated with OSC1 pin function. |
| CLKO | 7 | 10 | 8 | 31 | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function. |
| OSC1 | 6 | 9 | 7 | 30 | I | ST/CMOS | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. |
| OSC2 | 7 | 10 | 8 | 31 | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| SOSCI | 8 | 11 | 9 | 33 | I | ST/CMOS | 32.768 kHz low-power oscillator crystal input; CMOS otherwise. |
| SOSCO | 9 | 12 | 10 | 34 | O | — | 32.768 kHz low-power oscillator crystal output. |
| REFCLKI | PPS | PPS | PPS | PPS | I | ST | Reference Input Clock |
| REFCLKO | PPS | PPS | PPS | PPS | O | — | Reference Output Clock |
| IC1 | PPS | PPS | PPS | PPS | I | ST | Capture Inputs 1-5 |
| IC2 | PPS | PPS | PPS | PPS | I | ST | |
| IC3 | PPS | PPS | PPS | PPS | I | ST | |
| IC4 | PPS | PPS | PPS | PPS | I | ST | |
| IC5 | PPS | PPS | PPS | PPS | I | ST | |

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input
— = N/A

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e[®] Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS32[®] M4K[®] PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

| Opcode | Operand Size (mul <i>rt</i>) (div <i>rs</i>) | Latency | Repeat Rate |
|------------------------------------|------------------------------------------------|---------|-------------|
| MULT/MULTU, MADD/MADDU, MSUB/MSUBU | 16 bits | 1 | 1 |
| | 32 bits | 2 | 2 |
| MUL | 16 bits | 2 | 1 |
| | 32 bits | 3 | 2 |
| DIV/DIVU | 8 bits | 12 | 11 |
| | 16 bits | 19 | 18 |
| | 24 bits | 26 | 25 |
| | 32 bits | 33 | 32 |

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. For detailed information, refer to **Section 3. “Memory Organization”** (DS60001115), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|------------|----------------|----------------|-----------------------------|------------------------------|-------------------------------|----------------|---------------|---------------|
| 31:24 | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 23:16 | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 15:8 | R/W-0 WR | R/W-0 WREN | R-0 WRERR ⁽¹⁾ | R-0 LVDERR ⁽¹⁾ | R-0 LVDSTAT ⁽¹⁾ | U-0 — | U-0 — | U-0 — |
| 7:0 | U-0 — | U-0 — | U-0 — | U-0 — | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NVMOP<3:0> | | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit

This bit is writable when WREN = 1 and the unlock sequence is followed.

1 = Initiate a Flash operation. Hardware clears this bit when the operation completes

0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit

This is the only bit in this register reset by a device Reset.

1 = Enable writes to WR bit and enables LVD circuit

0 = Disable writes to WR bit and disables LVD circuit

bit 13 **WRERR:** Write Error bit⁽¹⁾

This bit is read-only and is automatically set by hardware.

1 = Program or erase sequence did not complete successfully

0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit (LVD circuit must be enabled)⁽¹⁾

This bit is read-only and is automatically set by hardware.

1 = Low-voltage detected (possible data corruption, if WRERR is set)

0 = Voltage level is acceptable for programming

bit 11 **LVDSTAT:** Low-Voltage Detect Status bit (LVD circuit must be enabled)⁽¹⁾

This bit is read-only and is automatically set and cleared by the hardware.

1 = Low-voltage event is active

0 = Low-voltage event is not active

bit 10-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits

These bits are writable when WREN = 0.

1111 = Reserved

•
•
•

0111 = Reserved

0110 = No operation

0101 = Program Flash Memory (PFM) erase operation: erases PFM, if all pages are not write-protected

0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected

0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected

0010 = No operation

0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected

0000 = No operation

Note 1: This bit is cleared by setting NVMOP == 'b0000, and initiating a Flash operation (i.e., WR).

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REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 31:24 | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 23:16 | R/W-0 CHSDIE | R/W-0 CHSHIE | R/W-0 CHDDIE | R/W-0 CHDHIE | R/W-0 CHBCIE | R/W-0 CHCCIE | R/W-0 CHTAIE | R/W-0 CHERIE |
| 15:8 | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 7:0 | R/W-0 CHSDIF | R/W-0 CHSHIF | R/W-0 CHDDIF | R/W-0 CHDHIF | R/W-0 CHBCIF | R/W-0 CHCCIF | R/W-0 CHTAIF | R/W-0 CHERIF |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit

1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)

0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit

1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)

0 = No interrupt is pending

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit

1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)

0 = No interrupt is pending

10.1 USB Control Registers

TABLE 10-1: USB REGISTER MAP

| Virtual Address (BF88-#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|-------|-------|------|------|------------------------|--------------|-------------------|----------|---------|----------|-----------------|--------------------|--------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5040 | U1OTGIR ⁽²⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF | 0000 |
| 5050 | U1OTGIE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | IDIE | T1MSECIE | LSTATEIE | ACTVIE | SESVDIE | SESENDIE | — | VBUSVDIE | 0000 |
| 5060 | U1OTGSTAT ⁽³⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ID | — | LSTATE | — | SESVD | SESEND | — | VBUSVD | 0000 |
| 5070 | U1OTGCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | DPPULUP | DMPULUP | DPPULDWN | DMPULDWN | VBUSON | OTGEN | VBUSCHG | VBUSDIS | 0000 |
| 5080 | U1PWRC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | UACTPND ⁽⁴⁾ | — | — | USLPGRD | USBBUSY | — | USUSPEND | USBPWR | 0000 |
| 5200 | U1IR ⁽²⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | STALLIF | ATTACHIF | RESUMEIF | IDLEIF | TRNIF | SOFIF | UERRIF | URSTIF DETACHIF | 0000 0000 |
| 5210 | U1IE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | STALLIE | ATTACHIE | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE | URSTIE DETACHIE | 0000 0000 |
| 5220 | U1EIR ⁽²⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BTSEF | BMXEF | DMAEF | BTOEF | DFN8EF | CRC16EF | CRC5EF EOFEF | PIDEF | 0000 0000 |
| 5230 | U1EIE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BTSEE | BMXEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE EOFEE | PIDEE | 0000 0000 |
| 5240 | U1STAT ⁽³⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ENDPT<3:0> | | | | DIR | PPBI | — | — | 0000 |
| 5250 | U1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | JSTATE | SE0 | PKTDIS TOKBUSY | USBRST | HOSTEN | RESUME | PPBRST | USBEN SOFEN | 0000 0000 |
| 5260 | U1ADDR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LSPDEN | DEVADDR<6:0> | | | | | | | 0000 |
| 5270 | U1BDTP1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRL<15:9> | | | | | | | — | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.
- 2: This register does not have associated SET and INV registers.
- 3: This register does not have associated CLR, SET and INV registers.
- 4: Reset value for this bit is undefined.

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REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)

- bit 1 **CRC5EF:** CRC5 Host Error Flag bit⁽⁴⁾
 1 = Token packet rejected due to CRC5 error
 0 = Token packet accepted
 EOFEF: EOF Error Flag bit^(3,5)
 1 = An EOF error condition was detected
 0 = No EOF error condition was detected
- bit 0 **PIDEF:** PID Check Failure Flag bit
 1 = PID check failed
 0 = PID check passed

- Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
- 2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
- 3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
- 4:** Device mode.
- 5:** Host mode.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
| | UTEYE | UOEMON | — | USBSIDL | — | — | — | UASUSPND |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit

1 = Eye-Pattern Test is enabled

0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB $\overline{\text{OE}}$ Monitor Enable bit

1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving

0 = OE signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit

1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 10-5.

0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock.

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11.1 Parallel I/O (PIO) Ports

All port pins have 10 registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

See the “**Pin Diagrams**” section for the available pins and their functionality.

11.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP.

11.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MX1XX/2XX 28/36/44-pin Family devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

An additional control register (CNCONx) is shown in Register 11-3.

11.2 CLR, SET and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

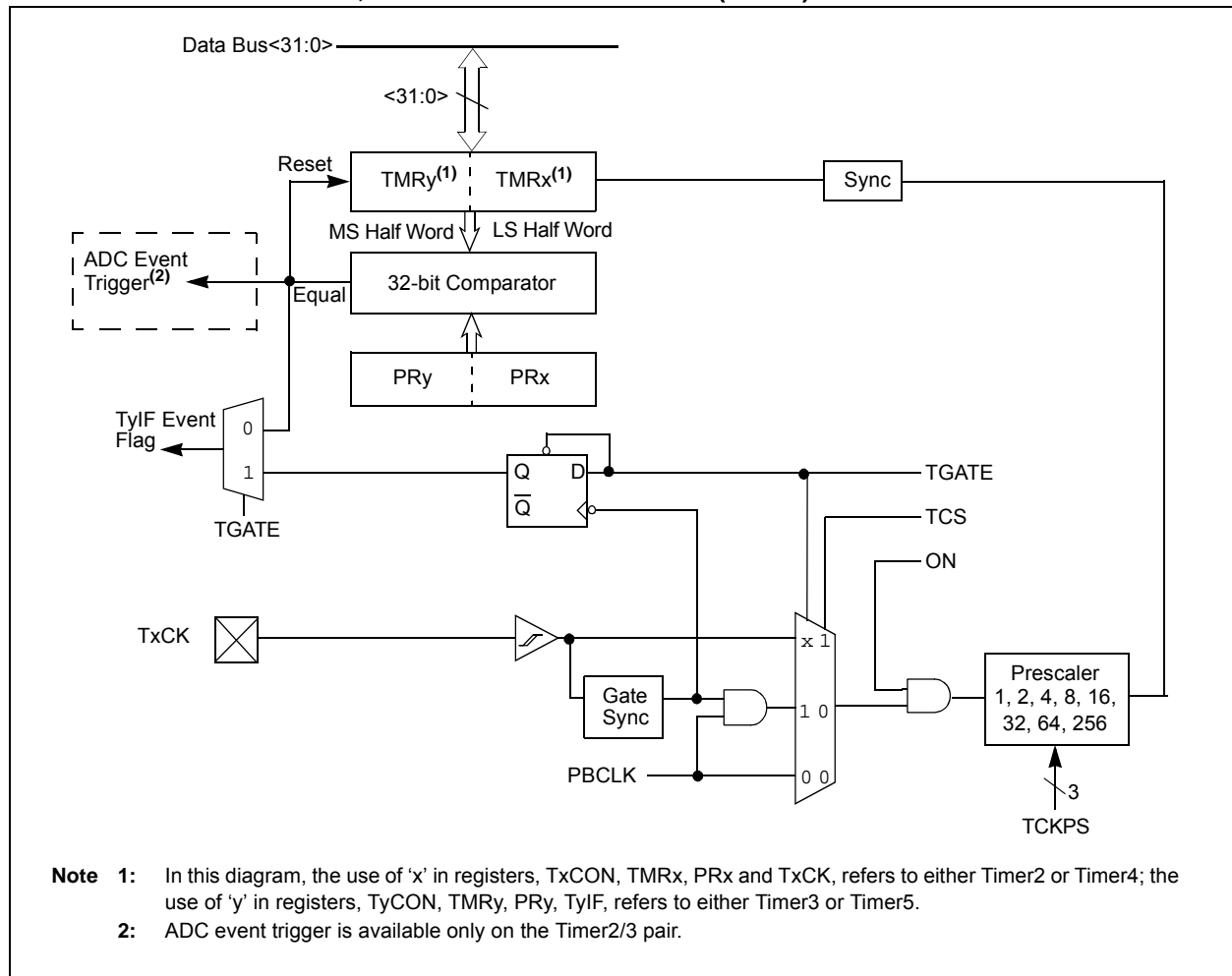
Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR, or INV register, the base register must be read.

TABLE 11-6: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|-----------------------------|------------------|-----------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|---------------|------|------|------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FA54 | U1CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U1CTSR<3:0> | | | | 0000 |
| FA58 | U2RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U2RXR<3:0> | | | | 0000 |
| FA5C | U2CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U2CTSR<3:0> | | | | 0000 |
| FA84 | SDI1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI1R<3:0> | | | | 0000 |
| FA88 | SS1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS1R<3:0> | | | | 0000 |
| FA90 | SDI2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI2R<3:0> | | | | 0000 |
| FA94 | SS2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS2R<3:0> | | | | 0000 |
| FAB8 | REFCLKIR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | REFCLKIR<3:0> | | | | 0000 |

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 13-2: TIMER2/3, TIMER4/5 BLOCK DIAGRAM (32-BIT)



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

bit 2-0 **ICM<2:0>**: Input Capture Mode Select bits

- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode – every sixteenth rising edge
- 100 = Prescaled Capture Event mode – every fourth rising edge
- 011 = Simple Capture Event mode – every rising edge
- 010 = Simple Capture Event mode – every falling edge
- 001 = Edge Detect mode – every edge (rising and falling)
- 000 = Input Capture module is disabled

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 1-0 **WAITE<1:0>**: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾

11 = Wait of 4 TPB
10 = Wait of 3 TPB
01 = Wait of 2 TPB
00 = Wait of 1 TPB (default)

For Read operations:

11 = Wait of 3 TPB
10 = Wait of 2 TPB
01 = Wait of 1 TPB
00 = Wait of 0 TPB (default)

- Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
- 2:** Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

25.1 CTMU Control Registers

TABLE 25-1: CTMU REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | All Resets | | |
|-----------------------------|---------------------------------|-----------|---------|---------|--------------|-------|-------|----------|----------|----------|------------|---------|--------------|------|------|------|------------|------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | | 17/1 | 16/0 |
| A200 | CTMUCON | 31:16 | EDG1MOD | EDG1POL | EDG1SEL<3:0> | | | | EDG2STAT | EDG1STAT | EDG2MOD | EDG2POL | EDG2SEL<3:0> | | | | — | — | 0000 |
| | | 15:0 | ON | — | CTMUSIDL | TGEN | EDGEN | EDGSEQEN | IDISSEN | CTTRIG | ITRIM<5:0> | | | | | | IRNG<1:0> | | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 27-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|------------------------------|-----------------------|----------------|----------------|----------------|------------------------------------|---------------|---------------|
| 31:24 | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — |
| 23:16 | r-1 — | r-1 — | r-1 — | r-1 — | r-1 — | R/P FPLLODIV<2:0> | R/P | R/P |
| 15:8 | R/P UPLLEN ⁽¹⁾ | r-1 — | r-1 — | r-1 — | r-1 — | R/P UPLLDIV<2:0> ⁽¹⁾ | R/P | R/P |
| 7:0 | r-1 — | R/P-1 FPLLMUL<2:0> | R/P | R/P-1 | r-1 — | R/P FPLLDIV<2:0> | R/P | R/P |

| | | |
|-------------------|------------------|----------------------------------------------|
| Legend: | r = Reserved bit | P = Programmable bit |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** Default PLL Output Divisor bits

111 = PLL output divided by 256
110 = PLL output divided by 64
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit⁽¹⁾
1 = Disable and bypass USB PLL
0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLDIV<2:0>:** USB PLL Input Divider bits⁽¹⁾

111 = 12x divider
110 = 10x divider
101 = 6x divider
100 = 5x divider
011 = 4x divider
010 = 3x divider
010 = 3x divider
001 = 2x divider
000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits

111 = 24x multiplier
110 = 21x multiplier
101 = 20x multiplier
100 = 19x multiplier
011 = 18x multiplier
010 = 17x multiplier
001 = 16x multiplier
000 = 15x multiplier

bit 3 **Reserved:** Write '1'

Note 1: This bit is only available on PIC32MX2XX devices.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp | | | | |
|--------------------|------------|------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-------------|------------|-------------------------------------------------|
| Param. No. | Symbol | Characteristics | Min. | Typical ⁽¹⁾ | Max. | Units | Conditions |
| OS10 | Fosc | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC 4 | — — | 40 40 | MHz MHz | EC (Note 4) ECPLL (Note 3) |
| OS11 | | Oscillator Crystal Frequency | 3 | — | 10 | MHz | XT (Note 4) |
| OS12 | | | 4 | — | 10 | MHz | XTPLL (Notes 3,4) |
| OS13 | | | 10 | — | 25 | MHz | HS (Note 5) |
| OS14 | | | 10 | — | 25 | MHz | HSPLL (Notes 3,4) |
| OS15 | | | 32 | 32.768 | 100 | kHz | Sosc (Note 4) |
| OS20 | Tosc | Tosc = 1/Fosc = Tcy (Note 2) | — | — | — | — | See parameter OS10 for Fosc value |
| OS30 | TosL, TosH | External Clock In (OSC1) High or Low Time | 0.45 x Tosc | — | — | ns | EC (Note 4) |
| OS31 | TosR, TosF | External Clock In (OSC1) Rise or Fall Time | — | — | 0.05 x Tosc | ns | EC (Note 4) |
| OS40 | TOST | Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes) | — | 1024 | — | Tosc | (Note 4) |
| OS41 | TfSCM | Primary Clock Fail Safe Time-out Period | — | 2 | — | ms | (Note 4) |
| OS42 | GM | External Oscillator Transconductance (Primary Oscillator only) | — | 12 | — | mA/V | VDD = 3.3V, TA = +25°C (Note 4) |

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

- 2:** Instruction cycle period (Tcy) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin.
- 3:** PLL input requirements: 4 MHz ≤ F_{PLLIN} ≤ 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 4:** This parameter is characterized, but not tested in manufacturing.

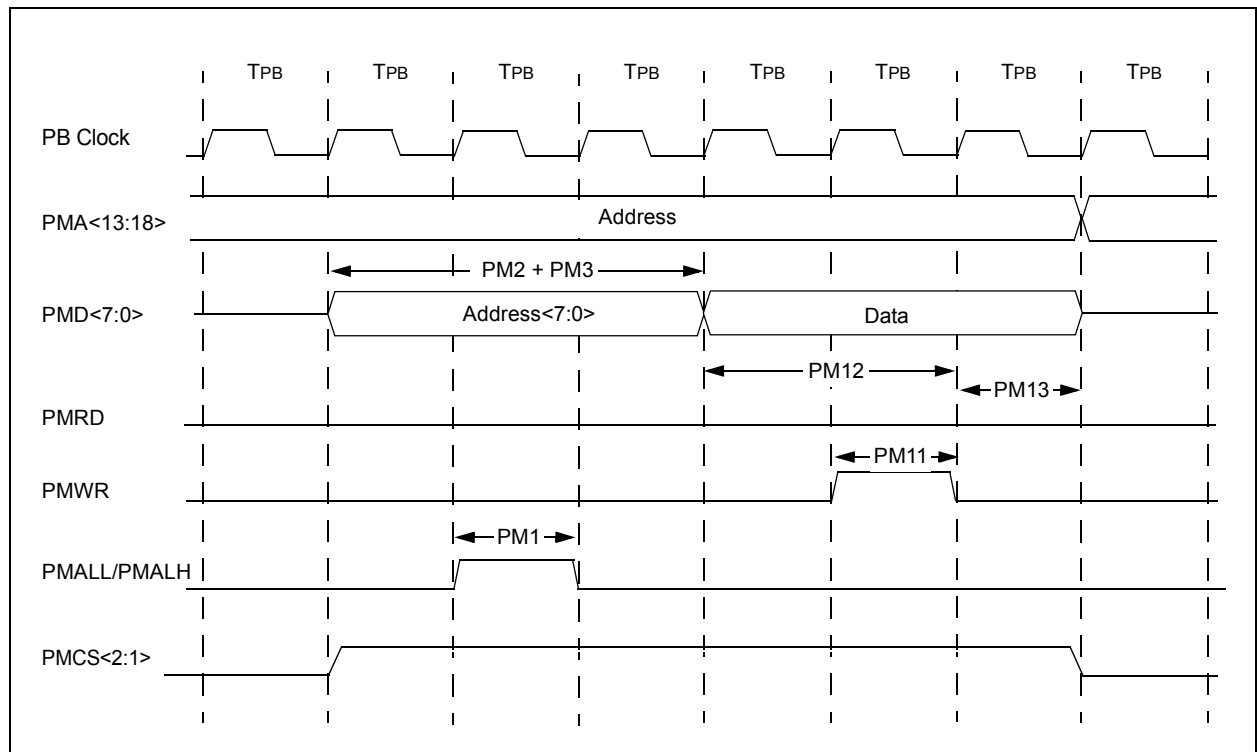
PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp | | | | |
|--------------------|---------|----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|------------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | Min. | Typ. | Max. | Units | Conditions |
| PM1 | TLAT | PMALL/PMALH Pulse Width | — | 1 TPB | — | — | — |
| PM2 | TADSU | Address Out Valid to PMALL/PMALH Invalid (address setup time) | — | 2 TPB | — | — | — |
| PM3 | TADHOLD | PMALL/PMALH Invalid to Address Out Invalid (address hold time) | — | 1 TPB | — | — | — |
| PM4 | TAHOLD | PMRD Inactive to Address Out Invalid (address hold time) | 5 | — | — | ns | — |
| PM5 | TRD | PMRD Pulse Width | — | 1 TPB | — | — | — |
| PM6 | TDSU | PMRD or PMENB Active to Data In Valid (data setup time) | 15 | — | — | ns | — |
| PM7 | TDHOLD | PMRD or PMENB Inactive to Data In Invalid (data hold time) | — | 80 | — | ns | — |

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 30-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 30-23: EJTAG TIMING CHARACTERISTICS

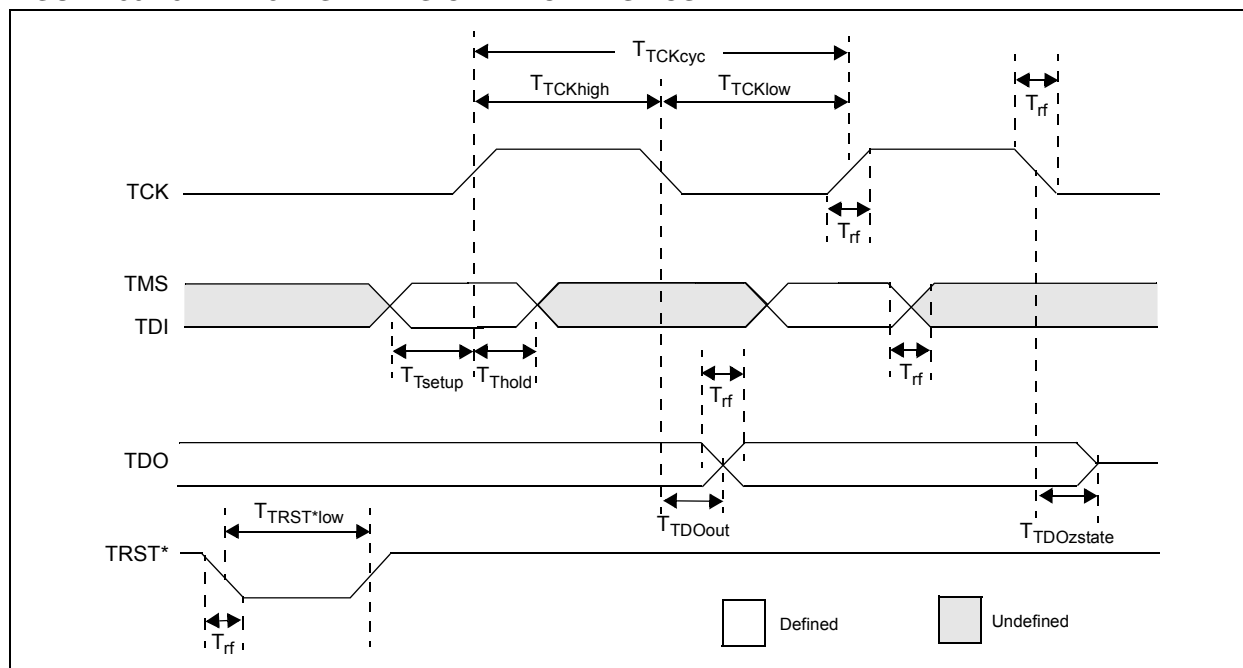


TABLE 30-42: EJTAG TIMING REQUIREMENTS

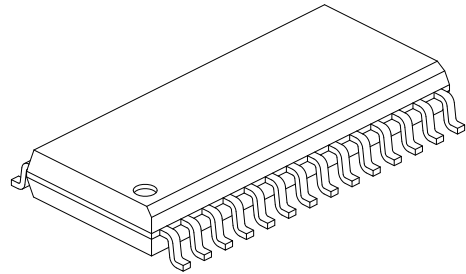
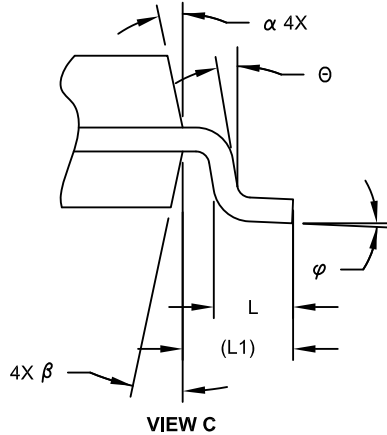
| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ Ta ≤ +85°C for Industrial -40°C ≤ Ta ≤ +105°C for V-temp | | | |
|--------------------|------------|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------------|
| Param. No. | Symbol | Description ⁽¹⁾ | Min. | Max. | Units | Conditions |
| EJ1 | TTCKCYC | TCK Cycle Time | 25 | — | ns | — |
| EJ2 | TTCKHIGH | TCK High Time | 10 | — | ns | — |
| EJ3 | TTCKLOW | TCK Low Time | 10 | — | ns | — |
| EJ4 | TTSETUP | TAP Signals Setup Time Before Rising TCK | 5 | — | ns | — |
| EJ5 | TTHOLD | TAP Signals Hold Time After Rising TCK | 3 | — | ns | — |
| EJ6 | TTDOOUT | TDO Output Delay Time from Falling TCK | — | 5 | ns | — |
| EJ7 | TTDOZSTATE | TDO 3-State Delay Time from Falling TCK | — | 5 | ns | — |
| EJ8 | TTRSTLOW | TRST Low Time | 25 | — | ns | — |
| EJ9 | TRF | TAP Signals Rise/Fall Time, All Input and Output | — | — | ns | — |

Note 1: These parameters are characterized, but not tested in manufacturing.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - |
| Standoff § | A1 | 0.10 | - | 0.30 |
| Overall Width | E | 10.30 BSC | | |
| Molded Package Width | E1 | 7.50 BSC | | |
| Overall Length | D | 17.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.75 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.40 REF | | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.18 | - | 0.33 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2