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Details

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Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f256dt-i-pt

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PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Pin Diagrams

TABLE 3: **PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES**

28	-PIN SOIC, SPDIP, SSOP (TOP VIEW) ^{(1,2,3})							
	1 SSOF	2	28	1 SC	DIC	28	1 S	PDIP	28
	PIC32MX110F016B PIC32MX120F032B PIC32MX130F064B PIC32MX130F256B PIC32MX150F128B PIC32MX170F256B								
Pin #	Full Pin Name		Pin #	Full Pin Name					
1	MCLR		15	PGEC3/RPB	6/PMD6/R	RB6			
2	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0		16	TDI/RPB7/C	ED3/PMD	05/INT0/R	B7		
3	VREF-/CVREF-/AN1/RPA1/CTED2/RA1		17	TCK/RPB8/S	CL1/CTE	D10/PMD4	4/RB8		
4	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0		18	TDO/RPB9/S	DA1/CTE	D4/PMD3	/RB9		
5	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1		19	Vss					
6	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2		20	VCAP					
7			24	PGED2/RPB10/CTED11/PMD2/RB10					
	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3		21	PGED2/RPB	10/CTED1	1/PMD2/F	RB10		
8	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss		21	PGED2/RPB PGEC2/TMS	10/CTED1 /RPB11/PI	11/PMD2/F MD1/RB1	RB10 1		
8 9	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2		21 22 23	PGED2/RPB PGEC2/TMS AN12/PMD0/	10/CTED1 /RPB11/PI RB12	11/PMD2/F MD1/RB1 [,]	RB10 1		
8 9 10	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3		21 22 23 24	PGED2/RPB PGEC2/TMS AN12/PMD0/ AN11/RPB13	10/CTED1 /RPB11/Pl RB12 /CTPLS/P	11/PMD2/F MD1/RB1 [,] PMRD/RB1	RB10 1 13		
8 9 10 11	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4		21 22 23 24 25	PGED2/RPB PGEC2/TMS AN12/PMD0/ AN11/RPB13 CVREFOUT/AI	10/CTED1 /RPB11/PI /RB12 /CTPLS/P N10/C3INE	I1/PMD2/F MD1/RB1 MRD/RB1 B/RPB14/S	RB10 1 13 SCK1/CTE	D5/PMW	R/RB14
8 9 10 11 12	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4 SOSCO/RPA4/T1CK/CTED9/PMA1/RA4		21 22 23 24 25 26	PGED2/RPB PGEC2/TMS AN12/PMD0/ AN11/RPB13 CVREFOUT/AI AN9/C3INA/F	10/CTED1 /RPB11/PI RB12 /CTPLS/P N10/C3INE RPB15/SC	I1/PMD2/F MD1/RB1 PMRD/RB1 B/RPB14/S K2/CTED	RB10 1 13 SCK1/CTE 6/PMCS1/	D5/PMW RB15	R/RB14
8 9 10 11 12 13	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4 SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 VDD		21 22 23 24 25 26 27	PGED2/RPB PGEC2/TMS AN12/PMD0/ AN11/RPB13 CVREFOUT/AI AN9/C3INA/F AVSS	10/CTED1 /RPB11/PI RB12 /CTPLS/P N10/C3INE RPB15/SC	I1/PMD2/F MD1/RB1 PMRD/RB1 B/RPB14/S K2/CTED	RB10 1 13 SCK1/CTE 6/PMCS1/	ED5/PMW RB15	R/RB14

1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

Shaded pins are 5V tolerant. 3:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
31.24	NVMKEY<31:24>										
00.40	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
23:10	NVMKEY<23:16>										
45.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
15:8	NVMKEY<15:8>										
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
7:0				NVMK	EY<7:0>						

REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMKEY<31:0>: Unlock Register bits

These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24	NVMADDR<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:10	NVMADDR<23:16>										
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
10.0	NVMADDR<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0				NVMA	DR<7:0>						

Legend:				
R = Readable bit	eadable bit W = Writable bit U = Unimplemented bit, read a			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 NVMADDR<31:0>: Flash Address bits

Bulk/Chip/PFM Erase: Address is ignored. Page Erase: Address identifies the page to erase. Row Program: Address identifies the row to program. Word Program: Address identifies the word to program.

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

(1)	IRQ	Vector		Interru	pt Bit Location		Persistent
Interrupt Source ⁽¹⁾	#	#	Flag	Enable	Priority	Sub-priority	Interrupt
		Highes	st Natural O	rder Priority	,		
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1E – SPI1 Fault	36	31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1TX – SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	_	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	—	—		
15:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0		
10.0	—	—	—	—	—	5	SRIPL<2:0> ⁽¹⁾			
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0	—	—		VEC<5:0> ⁽¹⁾						

REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 Unimplemented: Read as '0'

- bit 10-8 SRIPL<2:0>: Requested Priority Level bits⁽¹⁾
 - 111-000 = The priority level of the latest interrupt presented to the CPU
- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 VEC<5:0>: Interrupt Vector bits⁽¹⁾ 11111-00000 = The interrupt vector that is presented to the CPU
- Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
31.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
31.24		IPTMR<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
23.10	IPTMR<23:16>											
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
15.0	IPTMR<15:8>											
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
7:0				IPTM	IR<7:0>							

REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	—	—		
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
15:8	CHSPTR<15:8>									
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
7:0				CHSPTF	R<7:0>					

REGISTER 9-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER

Legend:

0			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSPTR<15:0>: Channel Source Pointer bits

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 9-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24		—	—	—	—		—	_
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16		—	—	—	—		—	_
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
10.0	CHDPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				CHDPTF	R<7:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16	Unimplemented: Read as '0'
-----------	----------------------------

bit 15-0 CHDPTR<15:0>: Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination

11.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 12. "I/O Ports" (DS60001120), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

General purpose I/O pins are the simplest of peripherals. They allow the PIC[®] MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions. These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Key features of this module include:

- · Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	—	FEDGE	C32
7.0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
7:0	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>	

REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unkno	own)	P = Programmable bit	r = Reserved bit

bit 31-16	Unimplemented: Read as '0'
bit 15	ON: Input Capture Module Enable bit ⁽¹⁾
	1 = Module is enabled
	0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Stop in Idle Control bit
	1 = Halt in Idle mode0 = Continue to operate in Idle mode
bit 12-10	Unimplemented: Read as '0'
bit 9	FEDGE: First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
	1 = Capture rising edge first
	0 = Capture falling edge first
bit 8	C32: 32-bit Capture Select bit
	1 = 32-bit timer resource capture
	0 = 16-bit timer resource capture
bit 7	ICTMR: Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
	0 = Timer3 is the counter source for capture
DIT 6-5	ICI<1:0>: Interrupt Control bits
	10 = Interrupt on every tourth capture event
	01 = Interrupt on every second capture event
	00 = Interrupt on every capture event
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
	1 = Input capture overflow has occurred
	0 = No input capture overflow has occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	 1 = Input capture buffer is not empty; at least one more capture value can be read 0 = Input capture buffer is empty
Note 1:	When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the
	STOCEN Gyole infinediately following the instruction that deals the module's ON bit.

REGISTER 18-2: I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware set or clear when Start, Repeated Start or Stop detected.
bit 3	S: Start bit
	 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last
	Hardware set or clear when Start, Repeated Start or Stop detected.
bit 2	R_W: Read/Write Information bit (when operating as I ² C slave)
	1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave
	Hardware set or clear after reception of I ² C device address byte.
bit 1	RBF: Receive Buffer Full Status bit
	1 = Receive complete, I2CxRCV is full
	0 = Receive not complete, I2CxRCV is empty
	Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit
	1 = Transmit in progress, I2CxTRN is full

0 = Transmit complete, I2CxTRN is empty

Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

- bit 1-0 WAITE<1:0>: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾
 - 11 = Wait of 4 Трв
 - 10 = Wait of 3 Трв
 - 01 = Wait of 2 TPB
 - 00 = Wait of 1 TPB (default)

For Read operations:

- 11 = Wait of 3 Трв
- 10 = Wait of 2 TPB
- 01 = Wait of 1 Трв
- 00 = Wait of 0 TPB (default)
- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
31:24	—	—	—	—	—	—	CAL<9):8>
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10				CAL<	:7:0>			
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ^(1,2)	—	SIDL	_	—	—	—	—
7.0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0
7:0	RTSECSEL ⁽³⁾	RTCCLKON	—	—	RTCWREN ⁽⁴⁾	RTCSYNC	HALFSEC ⁽⁵⁾	RTCOE

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 Unimplemented: Read as '0'

bit 25-16 CAL<9:0>: RTC Drift Calibration bits, which contain a signed 10-bit integer value 0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute 000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute 000000000 = No adjustment 1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute 100000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute ON: RTCC On bit^(1,2) bit 15 1 = RTCC module is enabled 0 = RTCC module is disabled bit 14 Unimplemented: Read as '0' bit 13 SIDL: Stop in Idle Mode bit 1 = Disables the PBCLK to the RTCC when the device enters Idle mode 0 = Continue normal operation when the device enters Idle mode bit 12-8 Unimplemented: Read as '0' bit 7 RTSECSEL: RTCC Seconds Clock Output Select bit⁽³⁾ 1 = RTCC Seconds Clock is selected for the RTCC pin 0 = RTCC Alarm Pulse is selected for the RTCC pin bit 6 RTCCLKON: RTCC Clock Enable Status bit 1 = RTCC Clock is actively running 0 = RTCC Clock is not running **Note 1:** The ON bit is only writable when RTCWREN = 1. 2: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit. 3: Requires RTCOE = 1 (RTCCON<0>) for the output to be active. 4: The RTCWREN bit can be set only when the write sequence is enabled. 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

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25.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 37. "Charge Time Measurement Unit (CTMU)" (DS60001167), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.



- Up to 13 channels available for capacitive or time measurement input
- · On-chip precision current source
- 16-edge input trigger sources
- · Selection of edge or level-sensitive inputs
- · Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- · High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- · Control of current source during auto-sampling
- · Four current source ranges
- · Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 25-1.



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						0		
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
31:24	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—		—	_
22.16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
23:16	—	—	—	—	—	—	—	-
15.0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
15.0	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
7.0	USERID<7:0>							

REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 FVBUSONIO: USB VBUSON Selection bit

- 1 = VBUSON pin is controlled by the USB module 0 = VBUSON pin is controlled by the port function
- bit 30 **FUSBIDIO:** USB USBID Selection bit 1 = USBID pin is controlled by the USB module 0 = USBID pin is controlled by the port function
- bit 29 IOL1WAY: Peripheral Pin Select Configuration bit
 - 1 = Allow only one reconfiguration
 - 0 = Allow multiple reconfigurations
- bit 28 PMDI1WAY: Peripheral Module Disable Configuration bit
 - 1 = Allow only one reconfiguration
 - 0 = Allow multiple reconfigurations
- bit 27-16 Reserved: Write '1'
- bit 15-0 USERID<15:0>: User ID bits

This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX 28/36/44-pin Family electrical characteristics for devices that operate at 40 MHz. Refer to **Section 31.0** "**50 MHz Electrical Characteristics**" for additional specifications for operations at higher frequency. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/36/44-pin Family devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	40°C to +105°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss (Note 3)	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD \ge 2.3V (Note 3)	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 2.3V (Note 3)	0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	0.3V to +5.5V
Maximum current out of Vss pin(s)	
Maximum current into VDD pin(s) (Note 2)	
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2)	200 mA

Note 1: Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: See the "Pin Diagrams" section for the 5V tolerant pins.

TABLE 30-9: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHA	ARACTER	RISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param. No.	Symbol	Characteristics	Min. Typ. ⁽¹⁾ Max. Units Conditions						
DI60a	licl	Input Low Injection Current	0	_	₋₅ (2,5)	mA	This parameter applies to all pins, with the exception of the power pins.		
DI60b	Іісн	Input High Injection Current	0	_	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, and the SOSCI, SOSCO, OSC1, D+, and D- pins.		
DI60c	∑lict	Total Input Injection Current (sum of all I/O and Control pins)	-20 (6)	_	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (IICL + IICH) $\leq \sum$ IICT)		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If Note 2, IICL = (((Vss - 0.3) - VIL source) / Rs). If Note 3, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (Vss - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp					
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DO10	Vol	Output Low Voltage	_	_	0.4	V	$\text{Iol} \leq 10 \text{ mA}, \text{ Vdd} = 3.3 \text{V}$
DO20 Voн		Output High Voltage	1.5 ⁽¹⁾	_	_		IOH \ge -14 mA, VDD = 3.3V
	Мон	I/O Pins	2.0 ⁽¹⁾	—	—	- v	IOH \ge -12 mA, VDD = 3.3V
	VOH		2.4	_	_		Ioh \geq -10 mA, Vdd = 3.3V
			3.0(1)	_	_		$IOH \ge -7 \text{ mA}, \text{ VDD} = 3.3 \text{V}$

TABLE 30-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized, but not tested.

TABLE 30-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min. ⁽¹⁾	Typical	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD transition high-to-low ⁽²⁾	2.0		2.3	V	_

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.



TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS ⁽¹⁾ Sta Opt					$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Charac	teristics ⁽²⁾		Min.	Typical	Max.	Units	Conditions	
TA10	Т⊤хН	TxCK High Time	Synchrono with presc	ous, aler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15	
			Asynchror with presc	nous, aler	10	—		ns	—	
TA11	ΤτxL	TxCK Low Time	Synchrono with presc	ous, aler	[(12.5 ns or 1 ТРв)/N] + 25 ns	—		ns	Must also meet parameter TA15	
			Asynchror with presc	nous, aler	10	—		ns	—	
TA15	ΤτχΡ	TxCK Input Period	Synchrono with presc	ous, aler	[(Greater of 25 ns or 2 TPB)/N] + 30 ns	-	_	ns	VDD > 2.7V	
					[(Greater of 25 ns or 2 TPB)/N] + 50 ns	—	_	ns	VDD < 2.7V	
			Asynchror with presc	nous, aler	20	-	_	ns	VDD > 2.7V (Note 3)	
					50	-	_	ns	VDD < 2.7V (Note 3)	
OS60	FT1	SOSC1/T1C Input Freque (oscillator en the TCS (T1	K Oscillato ncy Range abled by se CON<1>) b	r etting bit)	32	_	100	kHz	_	
TA20	TCKEXTMRL	Delay from E Clock Edge t Increment	External Tx0 to Timer	СК	_	_	1	Трв	_	

Note 1: Timer1 is a Type A timer.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

AC CHARACTERISTICS				Standard Op (unless other Operating te	erating rwise st mperatu	Conditio ated) re -40 -40	ons: 2.3V to 3.6V °C \leq TA \leq +85°C for Industrial °C \leq TA \leq +105°C for V-temp
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μS	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	μS	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode (Note 1)	0.5	—	μS	_
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μS	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	_	μS	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode (Note 1)	0.5	—	μS	
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode (Note 1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be from
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode (Note 1)	—	300	ns	
IS25	TSU:DAT	Data Input	100 kHz mode	250		ns	—
		Setup Time	400 kHz mode	100	_	ns	
			1 MHz mode (Note 1)	100	—	ns	
IS26	THD:DAT	Data Input	100 kHz mode	0		ns	—
		Hold Time	400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 1)	0	0.3	μS	
IS30	TSU:STA	Start Condition	100 kHz mode	4700		ns	Only relevant for Repeated
		Setup Time	400 kHz mode	600		ns	Start condition
			1 MHz mode (Note 1)	250	_	ns	
IS31	THD:STA	Start Condition	100 kHz mode	4000		ns	After this period, the first
		Hold Time	400 kHz mode	600	_	ns	clock pulse is generated
			1 MHz mode (Note 1)	250	—	ns	
IS33	Tsu:sto	Stop Condition	100 kHz mode	4000	_	ns	_
		Setup Time	400 kHz mode	600	—	ns]
			1 MHz mode (Note 1)	600		ns	

TABLE 30-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE A-1:	MAJOR SECTION UPDATES	(CONTINUED)	
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Section	Update Description
29.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings (removed Voltage on VCORE with respect to Vss).
	Added the SPDIP specification to the Thermal Packaging Characteristics (see Table 29-2).
	Updated the Typical values for parameters DC20-DC24 in the Operating Current (IDD) specification (see Table 29-5).
	Updated the Typical values for parameters DC30a-DC34a in the Idle Current (IIDLE) specification (see Table 29-6).
	Updated the Typical values for parameters DC40i and DC40n and removed parameter DC40m in the Power-down Current (IPD) specification (see Table 29-7).
	Removed parameter D320 (VCORE) from the Internal Voltage Regulator Specifications and updated the Comments (see Table 29-13).
	Updated the Minimum, Typical, and Maximum values for parameter F20b in the Internal FRC Accuracy specification (see Table 29-17).
	Removed parameter SY01 (TPWRT) and removed all Conditions from Resets Timing (see Table 29-20).
	Updated all parameters in the CTMU Specifications (see Table 29-39).
31.0 "Packaging Information"	Added the 28-lead SPDIP package diagram information (see 31.1 " Package Marking Information " and 31.2 " Package Details ").
"Product Identification System"	Added the SPDIP (SP) package definition.

Revision C (November 2011)

All major changes are referenced by their respective section in Table A-2.

TABLE A-2:	MAJOR SECTION UPDATES
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Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Revised the source/sink on I/O pins (see "Input/Output" on page 1). Added the SPDIP package to the PIC32MX220F032B device in the PIC32MX2XX USB Family Features (see Table 2).
4.0 "Memory Organization"	Removed ANSB6 from the ANSELB register and added the ODCB6, ODCB10, and ODCB11 bits in the PORTB Register Map (see Table 4-20).
29.0 "Electrical Characteristics"	Updated the minimum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 29-16).

Revision D (February 2012)

All occurrences of VUSB were changed to: VUSB3V3. In addition, text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-3: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 128	Corrected a part number error in all pin diagrams.
KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Updated the DMA Channels (Programmable/Dedicated) column in the PIC32MX1XX General Purpose Family Features (see Table 1).
1.0 "Device Overview"	Added the TQFP and VTLA packages to the 44-pin column heading and updated the pin numbers for the SCL1, SCL2, SDA1, and SDA2 pins in the Pinout I/O Descriptions (see Table 1-1).
7.0 "Interrupt Controller"	Updated the Note that follows the features.
	Updated the Interrupt Controller Block Diagram (see Figure 7-1).
29.0 "Electrical Characteristics"	Updated the Maximum values for parameters DC20-DC24, and the Minimum value for parameter DC21 in the Operating Current (IDD) DC Characteristics (see Table 29-5).
	Updated all Minimum and Maximum values for the Idle Current (IIDLE) DC Characteristics (see Table 29-6).
	Updated the Maximum values for parameters DC40k, DC40l, DC40n, and DC40m in the Power-down Current (IPD) DC Characteristics (see Table 29-7).
	Changed the minimum clock period for SCKx from 40 ns to 50 ns in Note 3 of the SPIx Master and Slave Mode Timing Requirements (see Table 29-26 through Table 29-29).
30.0 "DC and AC Device Characteristics Graphs"	Updated the Typical IIDLE Current @ VDD = 3.3V graph (see Figure 30-5).

Revision E (October 2012)

All singular pin diagram occurrences of CVREF were changed to: CVREFOUT. In addition, minor text and formatting changes were incorporated throughout the document.

All major changes are referenced by their respective section in Table A-4.

TABLE A-4:	MAJOR SECTION UPDATI	ΞS
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Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Updated the following feature sections: "Operating Conditions" "Communication Interfaces"
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Removed Section 2.8 "Configuration of Analog and Digital Pins During ICSP Operations".
3.0 "CPU"	Removed references to GPR shadow registers in 3.1 "Features" and 3.2.1 "Execution Unit" .
4.0 "Memory Organization"	Updated the BRG bit range in the SPI1 and SPI2 Register Map (see Table 4-8). Added the PWP<6> bit to the Device Configuration Word Summary (see Table 4-17).
5.0 "Flash Program Memory"	Added a note with Flash page size and row size information.
7.0 "Interrupt Controller"	Updated the TPC<2:0> bit definitions (see Register 7-1). Updated the IPTMR<31:0> bit definition (see Register 7-3).
8.0 "Oscillator Configuration"	Updated the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1). Updated the RODIV<14:0> bit definitions (see Register 8-3).
10.0 "USB On-The-Go (OTG)"	Updated the Notes in the USB Interface Diagram (see Figure 10-1).
18.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the baud rate range in the list of primary features.
26.0 "Special Features"	Added the PWP<6> bit to the Device Configuration Word 0 (see Register 26-1).
29.0 "Electrical Characteristics"	 Added Note 1 to Operating MIPS vs. Voltage (see Table 29-1). Added Note 2 to DC Temperature and Voltage Specifications (see Table 29-4). Updated the Conditions for parameter DC25 in DC Characteristics: Operating Current (IDD) (see Table 29-5). Added Note 2 to Electrical Characteristics: BOR (see Table 29-10). Added Note 4 to Comparator Specifications (see Table 29-12). Added Note 5 to ADC Module Specifications (see Table 29-32). Updated the 10-bit Conversion Rate Parameters and added Note 3 (see Table 29-33). Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 29-34). Added Note 3 to CTMU Current Source Specifications (see Table 29-39).
30.0 "50 MHz Electrical Characteristics"	New chapter with electrical characteristics for 50 MHz devices.
31.0 "Packaging Information"	The 36-pin and 44-pin VTLA packages have been updated.