



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128b-50i-ss

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 1: PIC32MX1XX 28/36/44-PIN GENERAL PURPOSE FAMILY FEATURES

Device	Pins	Program Memory (KB) ⁽¹⁾	Data Memory (KB)	Remappable Peripherals					Analog Comparators	USB On-The-Go (OTG)	I ² C	PMP	DMA Channels (Programmable/Dedicated)	CTMU	10-bit 1 Msps ADC (Channels)	RTCC	I/O Pins	JTAG	Packages
				Remappable Pins	Timers ⁽²⁾ /Capture/Compare	UART	SPI/I ² S	External Interrupts ⁽³⁾											
PIC32MX110F016B	28	16+3	4	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX110F016C	36	16+3	4	24	5/5/5	2	2	5	3	N	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX110F016D	44	16+3	4	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX120F032B	28	32+3	8	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX120F032C	36	32+3	8	24	5/5/5	2	2	5	3	N	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX120F032D	44	32+3	8	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX130F064B	28	64+3	16	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX130F064C	36	64+3	16	24	5/5/5	2	2	5	3	N	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX130F064D	44	64+3	16	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX150F128B	28	128+3	32	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX150F128C	36	128+3	32	24	5/5/5	2	2	5	3	N	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX150F128D	44	128+3	32	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX130F256B	28	256+3	16	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX130F256D	44	256+3	16	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX170F256B	28	256+3	64	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX170F256D	44	256+3	64	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN

- Note 1:** This device features 3 KB of boot Flash memory.
2: Four out of five timers are remappable.
3: Four out of five external interrupts are remappable.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 5: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES

28-PIN QFN (TOP VIEW)^(1,2,3,4) PIC32MX110F016B PIC32MX120F032B PIC32MX130F064B PIC32MX130F256B PIC32MX150F128B PIC32MX170F256B				28	1
Pin #	Full Pin Name	Pin #	Full Pin Name		
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9		
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	16	VSS		
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	17	VCAP		
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	18	PGED2/RPB10/CTED11/PMD2/RB10		
5	VSS	19	PGEC2/TMS/RPB11/PMD1/RB11		
6	OSC1/CLKI/RPA2/RA2	20	AN12/PMD0/RB12		
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13		
8	SOSCI/RPB4/RB4	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14		
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15		
10	VDD	24	AVSS		
11	PGED3/RPB5/PMD7/RB5	25	AVDD		
12	PGEC3/RPB6/PMD6/RB6	26	MCLR		
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0		
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	VREF-/CVREF-/AN1/RPA1/CTED2/RA1		

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

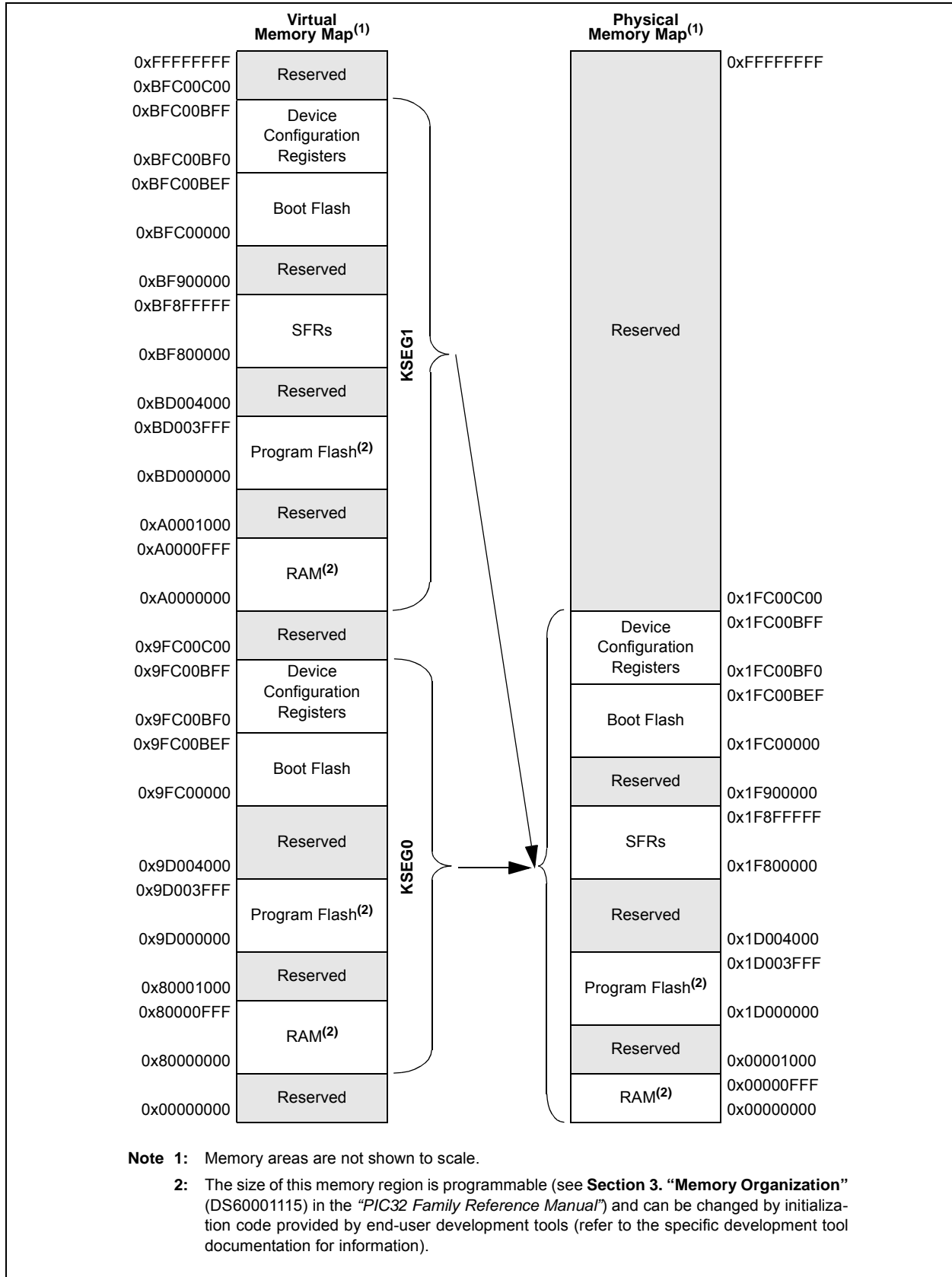
TABLE 14: PIN NAMES FOR 44-PIN USB DEVICES

44-PIN VTLA (TOP VIEW)^(1,2,3,5) PIC32MX210F016D PIC32MX220F032D PIC32MX230F064D PIC32MX230F256D PIC32MX250F128D PIC32MX270F256D				44		1	
Pin #	Full Pin Name	Pin #	Full Pin Name	Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2		
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3		
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0	25	AN6/RPC0/RC0		
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1	26	AN7/RPC1/RC1		
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2	27	AN8/RPC2/PMA2/RC2		
6	V _{SS}	28	V _{DD}	28	V _{DD}		
7	V _{CAP}	29	V _{SS}	29	V _{SS}		
8	PGED2/RPB10/D+/CTED11/RB10	30	OSC1/CLKI/RPA2/RA2	30	OSC1/CLKI/RPA2/RA2		
9	PGEC2/RPB11/D-/RB11	31	OSC2/CLKO/RPA3/RA3	31	OSC2/CLKO/RPA3/RA3		
10	V _{USB3V3}	32	TDO/RPA8/PMA8/RA8	32	TDO/RPA8/PMA8/RA8		
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4	33	SOSCI/RPB4/RB4		
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4	34	SOSCO/RPA4/T1CK/CTED9/RA4		
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9	35	TDI/RPA9/PMA9/RA9		
14	CVREFOUT/AN10/C3INB/RPB14/V _{BUSON} /SCK1/CTED5/RB14	36	AN12/RPC3/RC3	36	AN12/RPC3/RC3		
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4	37	RPC4/PMA4/RC4		
16	AV _{SS}	38	RPC5/PMA3/RC5	38	RPC5/PMA3/RC5		
17	AV _{DD}	39	V _{SS}	39	V _{SS}		
18	MCLR	40	V _{DD}	40	V _{DD}		
19	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	41	RPB5/USBID/RB5	41	RPB5/USBID/RB5		
20	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	42	V _{BUS}	42	V _{BUS}		
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7	43	RPB7/CTED3/PMD5/INT0/RB7		
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8	44	RPB8/SCL1/CTED10/PMD4/RB8		

- Note** 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
- 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to V_{SS} externally.
- 4: This pin function is not available on PIC32MX210F016D and PIC32MX220F032D devices.
- 5: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX110/210 DEVICES (4 KB RAM, 16 KB FLASH)



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDKPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDKPBA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits

When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** Read-Only bits

This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. “Oscillator Configuration”** (DS60001112), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MX1XX/2XX 28/36/44-pin Family oscillator system has the following modules and features:

- Four external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

A block diagram of the oscillator system is provided in Figure 8-1.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 9-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHP DAT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHP DAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:

Data to be matched must be stored in this register to allow a "terminate on match".

All other modes:

Unused.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS
	BTSEF	BMXEF	DMAEF ⁽¹⁾	BTOEF ⁽²⁾	DFN8EF	CRC16EF	CRC5EF ⁽⁴⁾ EOFEF ^(3,5)	PIDEF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit
 1 = Packet rejected due to bit stuff error
 0 = Packet accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
 1 = The base address, of the Buffer Descriptor Table, or the address of an individual buffer pointed to by a Buffer Descriptor Table entry, is invalid.
 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit⁽¹⁾
 1 = USB DMA error condition detected
 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit⁽²⁾
 1 = Bus turnaround time-out has occurred
 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit
 1 = Data field received is not an integral number of bytes
 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
 1 = Data packet rejected due to CRC16 error
 0 = Data packet accepted

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit

1 = Next token command to be executed at Low-Speed

0 = Next token command to be executed at Full-Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 10-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

TABLE 11-5: PORTC REGISTER MAP

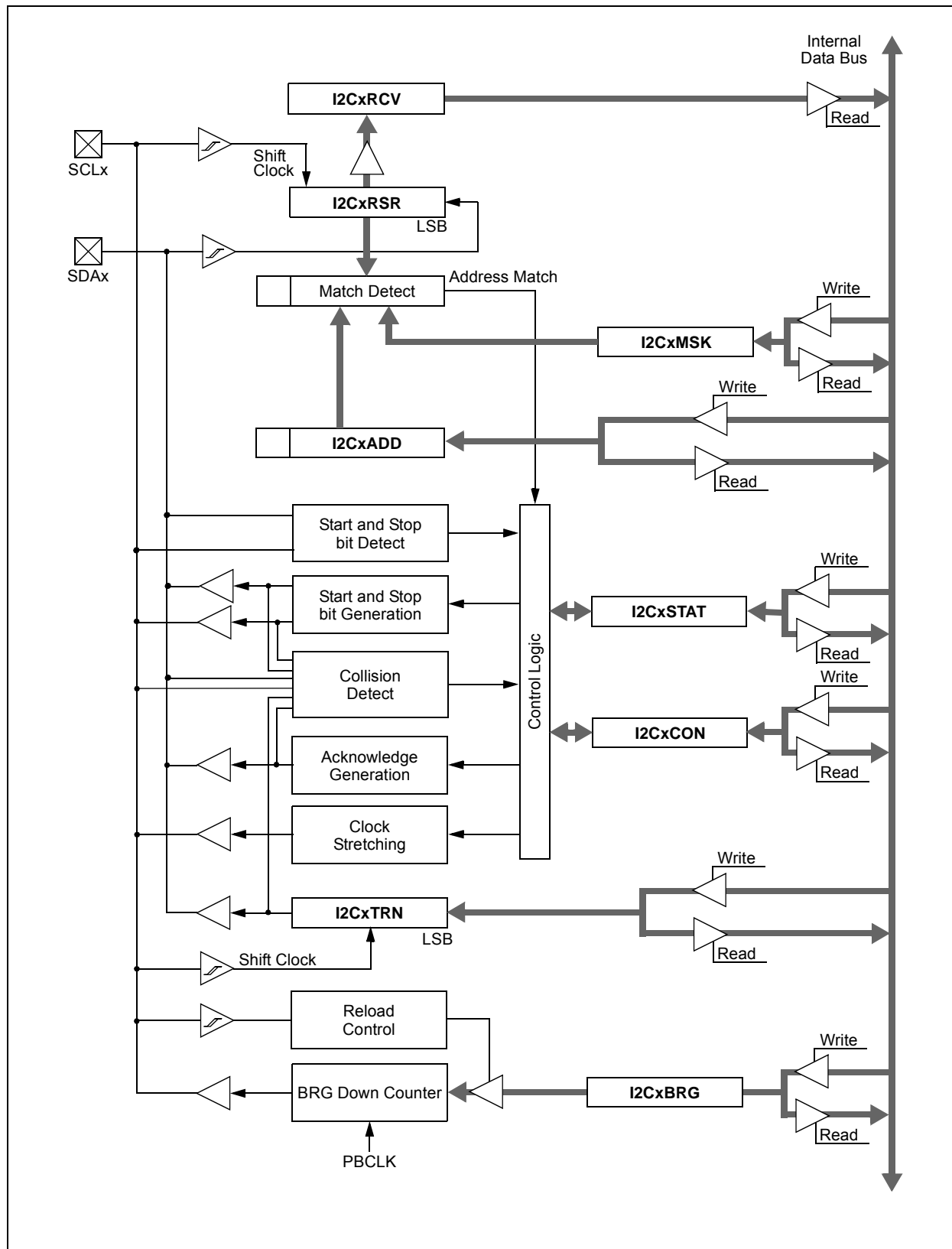
Virtual Address (BF88-#)	Register Name ^(1,2)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	ANSC3 ⁽⁴⁾	ANSC2 ⁽³⁾	ANSC1	ANSC0	000F
6210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISC9	TRISC8 ⁽³⁾	TRISC7 ⁽³⁾	TRISC6 ⁽³⁾	TRISC5 ⁽³⁾	TRISC4 ⁽³⁾	TRISC3	TRISC2 ⁽³⁾	TRISC1	TRISC0	03FF
6220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RC9	RC8 ⁽³⁾	RC7 ⁽³⁾	RC6 ⁽³⁾	RC5 ⁽³⁾	RC4 ⁽³⁾	RC3	RC2 ⁽³⁾	RC1	RC0	xxxx
6230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATC9	LATC8 ⁽³⁾	LATC7 ⁽³⁾	LATC6 ⁽³⁾	LATC5 ⁽³⁾	LATC4 ⁽³⁾	LATC3	LATC2 ⁽³⁾	LATC1	LATC0	xxxx
6240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCC9	ODCC8 ⁽³⁾	ODCC7 ⁽³⁾	ODCC6 ⁽³⁾	ODCC5 ⁽³⁾	ODCC4 ⁽³⁾	ODCC3	ODCC2 ⁽³⁾	ODCC1	ODCC0	0000
6250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUC9	CNPUC8 ⁽³⁾	CNPUC7 ⁽³⁾	CNPUC6 ⁽³⁾	CNPUC5 ⁽³⁾	CNPUC4 ⁽³⁾	CNPUC3	CNPUC2 ⁽³⁾	CNPUC1	CNPUC0	0000
6260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDC9	CNPDC8 ⁽³⁾	CNPDC7 ⁽³⁾	CNPDC6 ⁽³⁾	CNPDC5 ⁽³⁾	CNPDC4 ⁽³⁾	CNPDC3	CNPDC2 ⁽³⁾	CNPDC1	CNPDC0	0000
6270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIEC9	CNIEC8 ⁽³⁾	CNIEC7 ⁽³⁾	CNIEC6 ⁽³⁾	CNIEC5 ⁽³⁾	CNIEC4 ⁽³⁾	CNIEC3	CNIEC2 ⁽³⁾	CNIEC1	CNIEC0	0000
6290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNSTATC9	CNSTATC8 ⁽³⁾	CNSTATC7 ⁽³⁾	CNSTATC6 ⁽³⁾	CNSTATC5 ⁽³⁾	CNSTATC4 ⁽³⁾	CNSTATC3	CNSTATC2 ⁽³⁾	CNSTATC1	CNSTATC0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.
- 2: PORTC is not available on 28-pin devices.
- 3: This bit is only available on 44-pin devices.
- 4: This bit is only available on USB-enabled devices with 36 or 44 pins.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 18-1: I²C BLOCK DIAGRAM



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 19-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	IREN	RTSMD	—	UEN<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit⁽¹⁾

1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by the UEN<1:0> and UTXEN control bits.

0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal.

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit

1 = IrDA is enabled

0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit

1 = UxRTS pin is in Simplex mode

0 = UxRTS pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits

11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register

10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used

01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register

00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit

1 = Wake-up enabled

0 = Wake-up disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit

1 = Loopback mode is enabled

0 = Loopback mode is disabled

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSClk cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)

- bit 5-4 **Unimplemented:** Read as '0'
- bit 3 **RTCWREN:** RTC Value Registers Write Enable bit⁽⁴⁾
1 = RTC Value registers can be written to by the user
0 = RTC Value registers are locked out from being written to by the user
- bit 2 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read
If the register is read twice and results in the same data, the data can be assumed to be valid
0 = RTC Value registers can be read without concern about a rollover ripple
- bit 1 **HALFSEC:** Half-Second Status bit⁽⁵⁾
1 = Second half period of a second
0 = First half period of a second
- bit 0 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output enabled – clock presented onto an I/O
0 = RTCC clock output disabled

- Note 1:** The ON bit is only writable when RTCWREN = 1.
- 2:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
- 4:** The RTCWREN bit can be set only when the write sequence is enabled.
- 5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

23.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS60001110), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

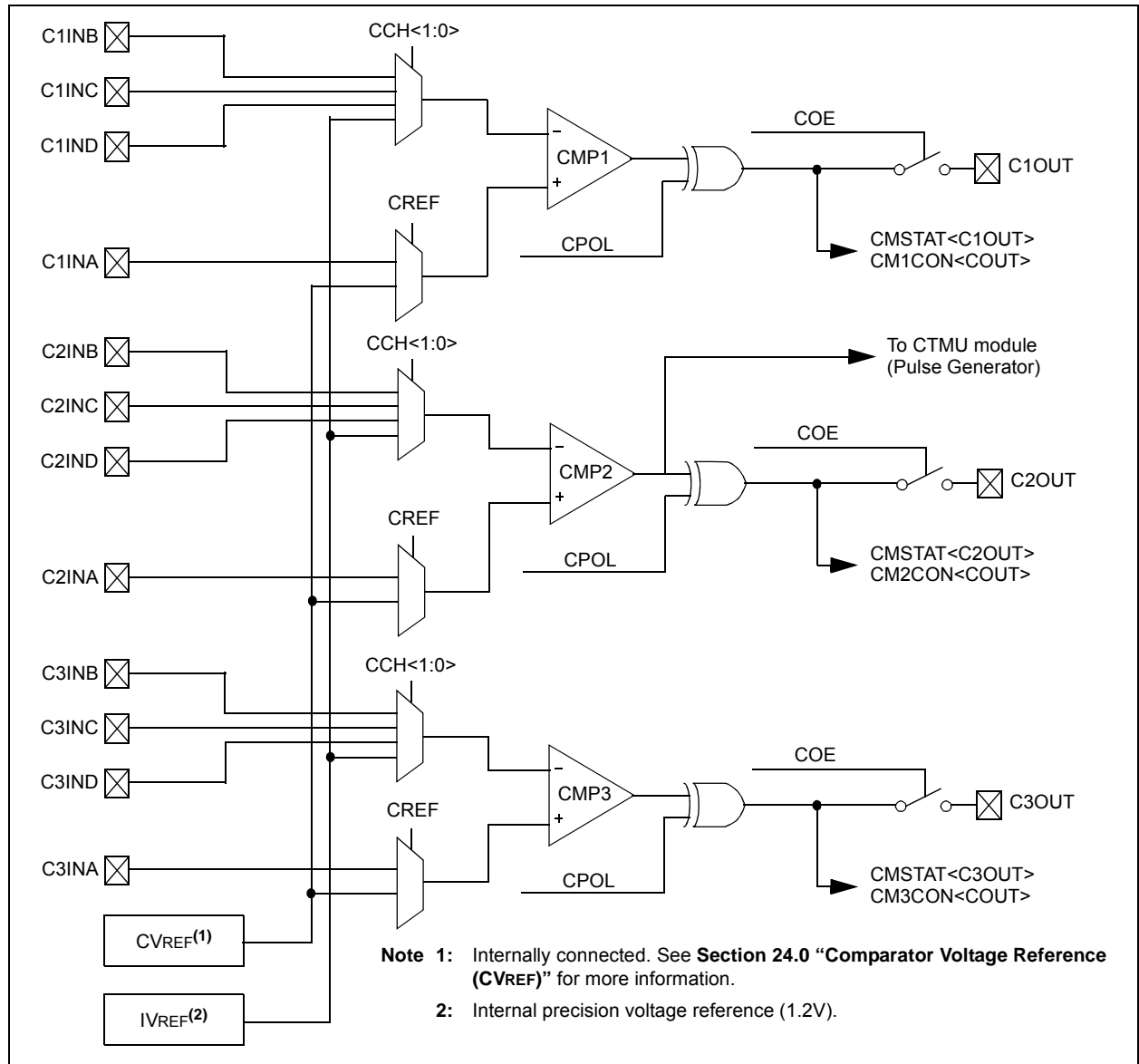
The Analog Comparator module contains three comparators that can be configured in a variety of ways.

Following are some of the key features of this module:

- Selectable inputs available include:
 - Analog inputs multiplexed with I/O pins
 - On-chip internal absolute voltage reference (IVREF)
 - Comparator voltage reference (CVREF)
- Outputs can be Inverted
- Selectable interrupt generation

A block diagram of the comparator module is provided in Figure 23-1.

FIGURE 23-1: COMPARATOR BLOCK DIAGRAM



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode (Note 1)	0.5	—	μs	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode (Note 1)	0.5	—	μs	—
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode (Note 1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode (Note 1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 1)	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode (Note 1)	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode (Note 1)	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode (Note 1)	600	—	ns	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode (Note 1)	250		ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode (Note 1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode (Note 1)	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	400	pF	—

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-34: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	AVDD	V	(Note 1)
Reference Inputs							
AD05 AD05a	VREFH	Reference Voltage High	AVSS + 2.0 2.5	— —	AVDD 3.6	V V	(Note 1) VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08 AD08a	IREF	Current Drain	— —	250 —	400 3	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15	—	Leakage Current	—	± 0.001	± 0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 k Ω
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5k	Ω	(Note 1)
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	EOFF	Offset Error	> -1	—	< 1	Lsb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

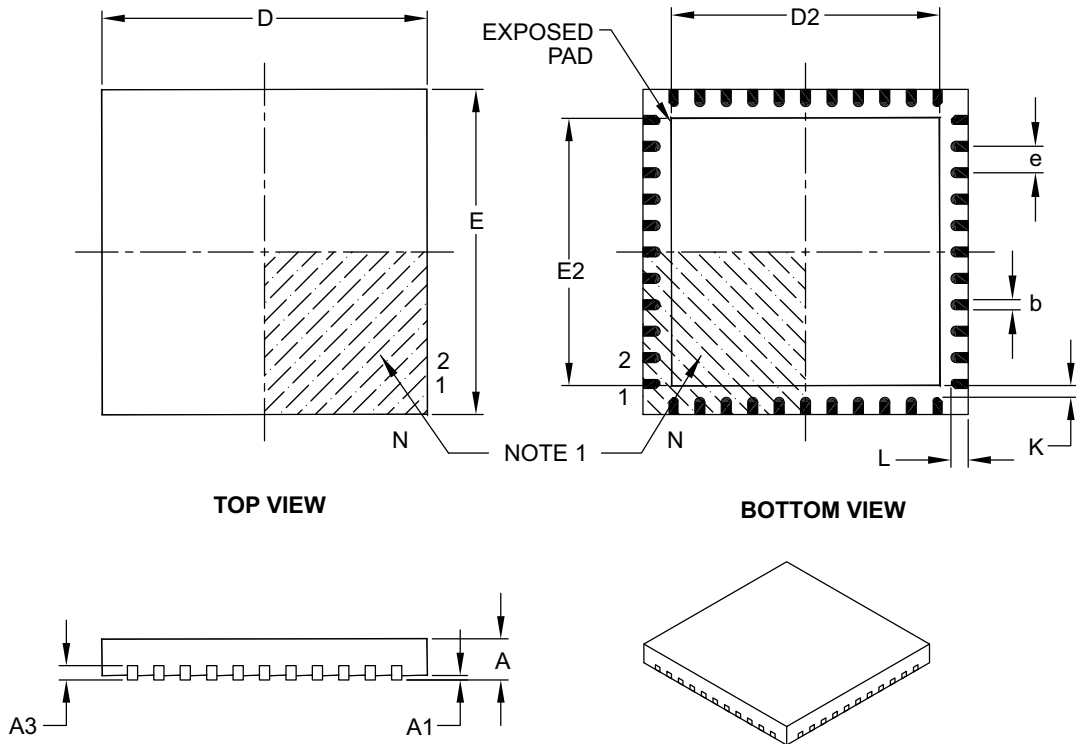
4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at $V_{BORMIN} < V_{DD} < 2.5\text{V}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		44		
Pitch	e		0.65 BSC		
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Width	E		8.00 BSC		
Exposed Pad Width	E2		6.30	6.45	6.80
Overall Length	D		8.00 BSC		
Exposed Pad Length	D2		6.30	6.45	6.80
Contact Width	b		0.25	0.30	0.38
Contact Length	L		0.30	0.40	0.50
Contact-to-Exposed Pad	K		0.20	—	—

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

INDEX

Numerics

50 MHz Electrical Characteristics	301
---	-----

A

AC Characteristics	269
10-Bit Conversion Rate Parameters	291
ADC Specifications	289
Analog-to-Digital Conversion Requirements	292
EJTAG Timing Requirements	300
Internal FRC Accuracy	271
Internal RC Accuracy	271
OTG Electrical Specifications	298
Parallel Master Port Read Requirements	297
Parallel Master Port Write	298
Parallel Master Port Write Requirements	298
Parallel Slave Port Requirements	296
PLL Clock Timing	271
Analog-to-Digital Converter (ADC)	209
Assembler	
MPASM Assembler	254

B

Block Diagrams	
ADC Module	209
Comparator I/O Operating Modes	219
Comparator Voltage Reference	223
Connections for On-Chip Voltage Regulator	250
Core and Peripheral Modules	19
CPU	33
CTMU Configurations	
Time Measurement	227
DMA	83
I2C Circuit	174
Input Capture	157
Interrupt Controller	63
JTAG Programming, Debugging and Trace Ports	250
Output Compare Module	161
PMP Pinout and Connections to External Devices	189
Reset System	59
RTCC	199
SPI Module	165
Timer1	143
Timer2/3/4/5 (16-Bit)	147
Typical Multiplexed Port Structure	127
UART	181
WDT and Power-up Timer	153
Brown-out Reset (BOR)	
and On-Chip Voltage Regulator	250

C

C Compilers	
MPLAB C18	254
Charge Time Measurement Unit. See CTMU.	
Clock Diagram	74
Comparator	
Specifications	267, 268
Comparator Module	219
Comparator Voltage Reference (CVref)	223
Configuration Bit	239
Configuring Analog Port Pins	128
CPU	
Architecture Overview	34
Coprocesor 0 Registers	35

Core Exception Types	36
EJTAG Debug Support	36
Power Management	36
CPU Module	27, 33
Customer Change Notification Service	341
Customer Notification Service	341
Customer Support	341

D

DC and AC Characteristics	
Graphs and Tables	307
DC Characteristics	258
I/O Pin Input Specifications	263, 264
I/O Pin Output Specifications	265
Idle Current (I _{IDLE})	261
Power-Down Current (I _{PD})	262
Program Memory	266
Temperature and Voltage Specifications	259
DC Characteristics (50 MHz)	302
Idle Current (I _{IDLE})	303
Power-Down Current (I _{PD})	303
Development Support	253
Direct Memory Access (DMA) Controller	83

E

Electrical Characteristics	257
AC	269
Errata	16
External Clock	
Timer1 Timing Requirements	275
Timer2, 3, 4, 5 Timing Requirements	276
Timing Requirements	270
External Clock (50 MHz)	
Timing Requirements	304

F

Flash Program Memory	53
RTSP Operation	53

I

I/O Ports	127
Parallel I/O (PIO)	128
Write/Read Timing	128
Input Change Notification	128
Instruction Set	251
Inter-Integrated Circuit (I2C)	173
Internal Voltage Reference Specifications	268
Internet Address	341
Interrupt Controller	63
IRG, Vector and Bit Location	64

M

Memory Maps	
PIC32MX110/210 Devices	
(4 KB RAM, 16 KB Flash)	38
PIC32MX120/220 Devices	
(8 KB RAM, 32 KB Flash)	39
PIC32MX130/230	
(16 KB RAM, 256 KB Flash)	43
PIC32MX130/230 Devices	
(16 KB RAM, 64 KB Flash)	40
PIC32MX150/250 Devices	
(32 KB RAM, 128 KB Flash)	41
PIC32MX170/270	

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =**

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KeeLoq, KeeLoq logo, Klear, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQL, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2011-2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN:978-1-5224-0471-2