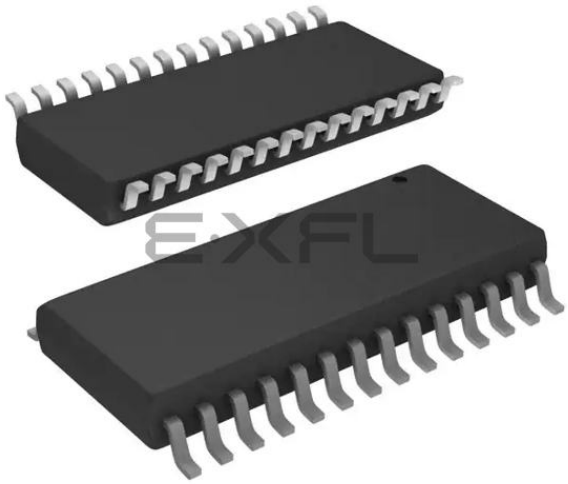

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128bt-i-so

2.9 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-5 and Figure 2-6.

FIGURE 2-5: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION

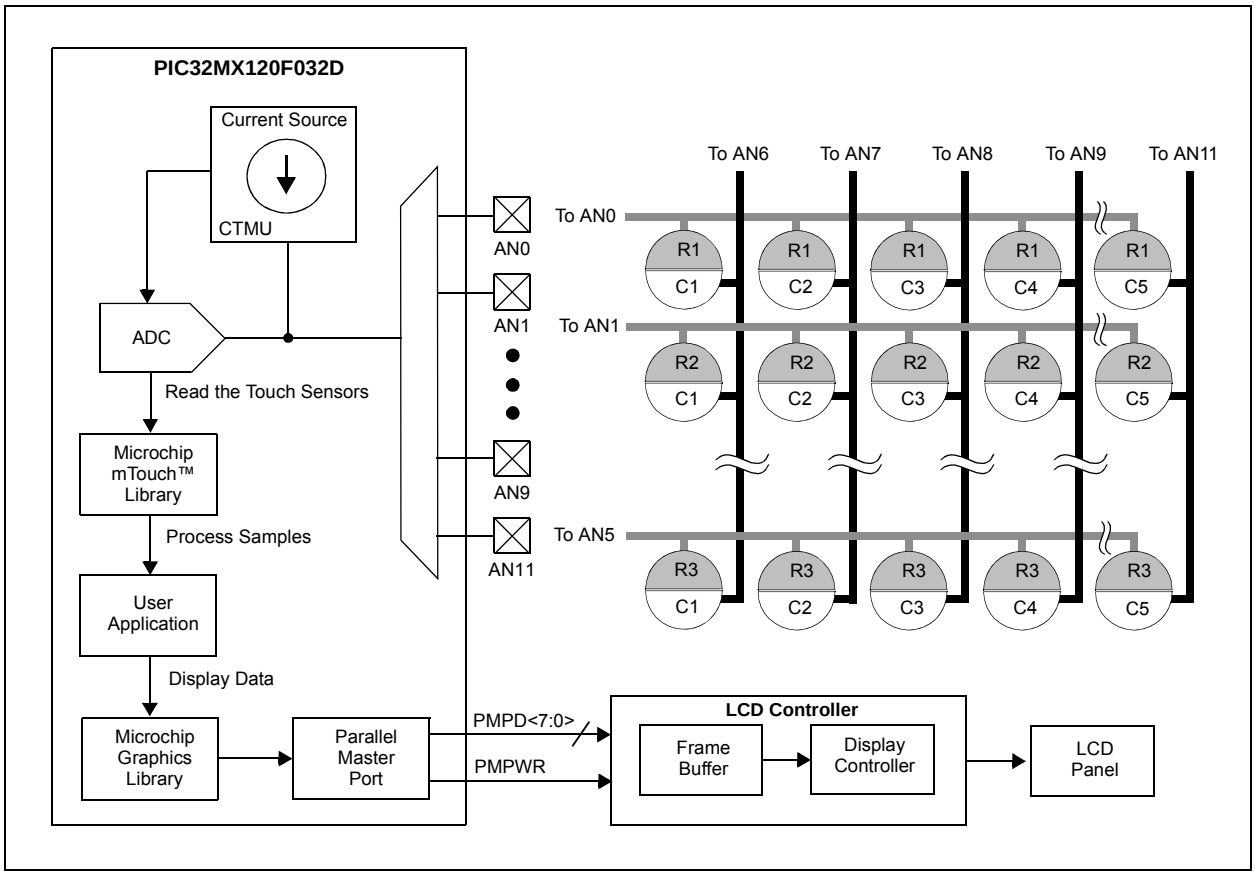
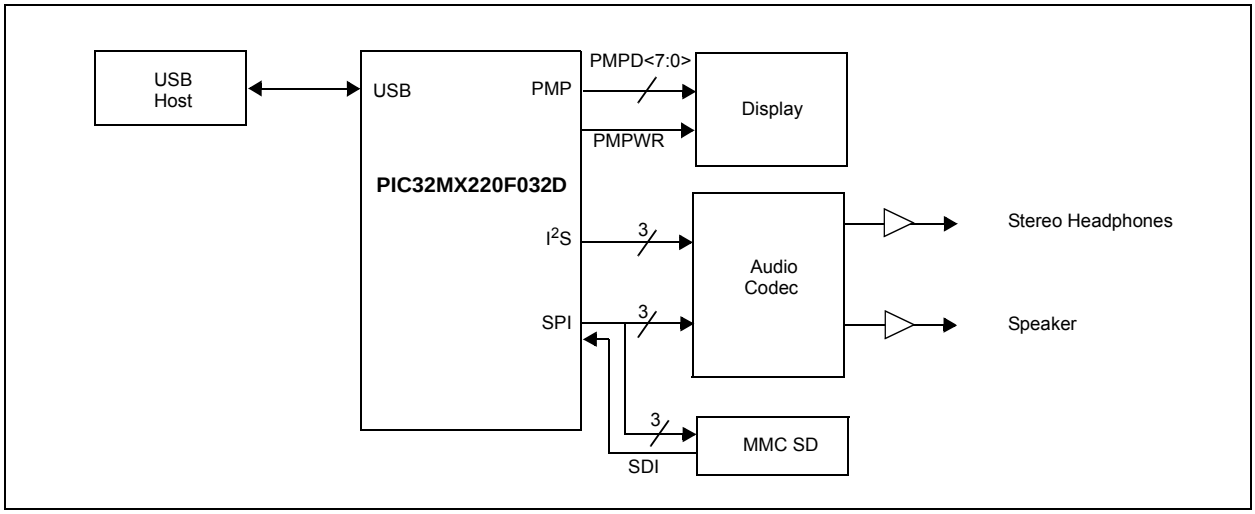


FIGURE 2-6: AUDIO PLAYBACK APPLICATION



REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDUPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDUPBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUPBA<15:10>:** DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** Read-Only bits

This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

NOTES:

NOTES:

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Oscillator Configuration"** (DS60001112), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MX1XX/2XX 28/36/44-pin Family oscillator system has the following modules and features:

- Four external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

A block diagram of the oscillator system is provided in Figure 8-1.

REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

100000 = Center frequency -12.5%
100001 =
•
•
•
111111 =
000000 = Center frequency. Oscillator runs at minimal frequency (8 MHz)
000001 =
•
•
•
011110 =
011111 = Center frequency +12.5%

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 6 **CRCAPP:** CRC Append Mode bit(1)
- 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
- 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination

bit 5 **CRCTYP:** CRC Type Selection bit
- 1 = The CRC module will calculate an IP header checksum
- 0 = The CRC module will calculate a LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
- 111 = CRC is assigned to Channel 7
- 110 = CRC is assigned to Channel 6
- 101 = CRC is assigned to Channel 5
- 100 = CRC is assigned to Channel 4
- 011 = CRC is assigned to Channel 3
- 010 = CRC is assigned to Channel 2
- 001 = CRC is assigned to Channel 1
- 000 = CRC is assigned to Channel 0

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Reset all Even/Odd buffer pointers to the EVEN Buffer Descriptor banks
0 = Even/Odd buffer pointers are not Reset

bit 0 **USBEN:** USB Module Enable bit(4)
1 = USB module and supporting circuitry is enabled
0 = USB module and supporting circuitry is disabled

SOFEN: SOF Enable bit(5)
1 = SOF token is sent every 1 ms
0 = SOF token is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).

2: All host control logic is reset any time that the value of this bit is toggled.

3: Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.

4: Device mode.

5: Host mode.

11.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions.

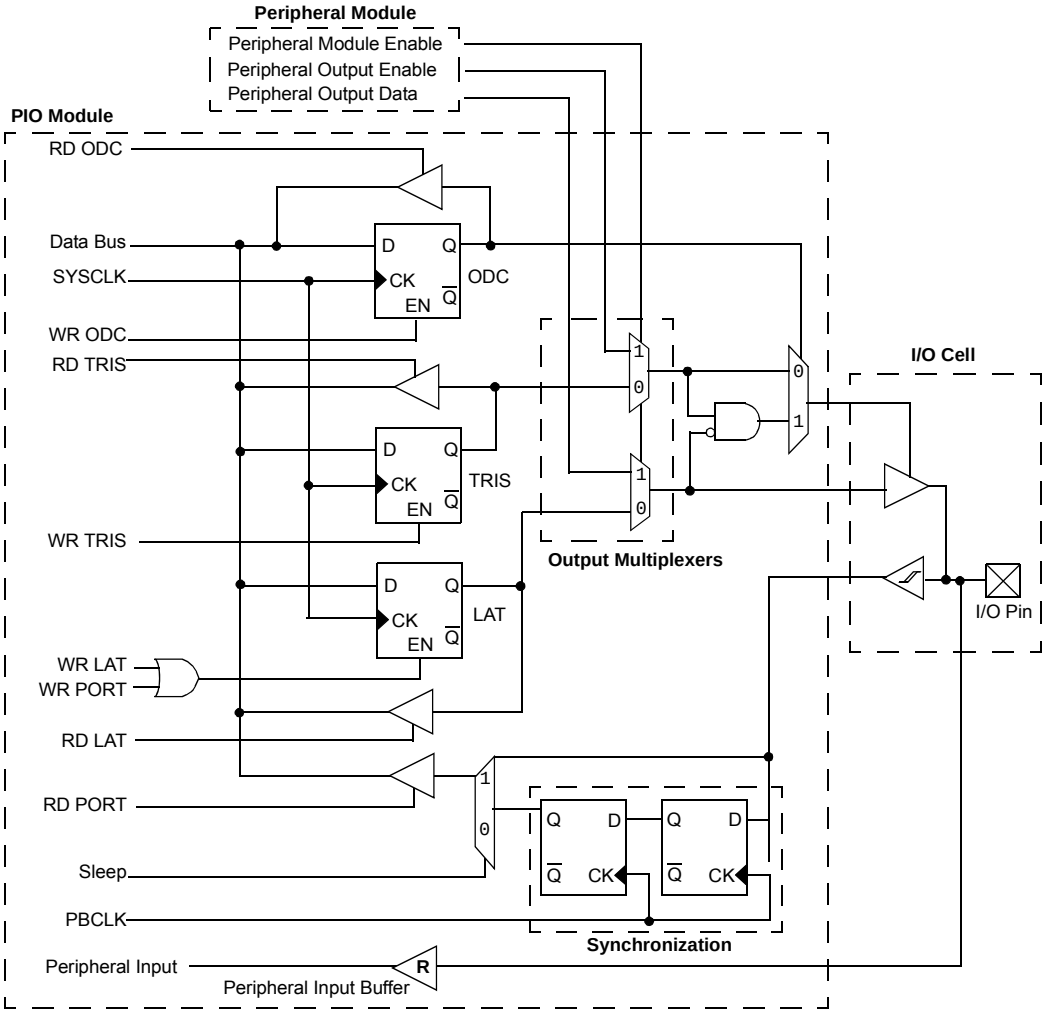
These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Key features of this module include:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



Legend: R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

Note: This block diagram is a general representation of a shared port/peripheral structure and is only provided for illustration purposes. The actual structure for any specific port/peripheral combination may be different than it is shown here.

13.2 Timer Control Registers

TABLE 13-1: TIMER2-TIMER5 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0810	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0820	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0A00	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0A10	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0A20	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0C00	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0C10	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0C20	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0E00	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0E10	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0E20	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

14.1 Watchdog Timer Control Registers

TABLE 14-1: WATCHDOG TIMER CONTROL REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					WDTWINEN	WDTCLR	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

20.1 PMP Control Registers

TABLE 20-1: PARALLEL MASTER PORT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	PMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	—	CS1P	—	WRSP	RDSP	0000
7010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		—	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
7020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	CS1 / ADDR14	—	—	—	ADDR<10:0>											0000
7030	PMDOUT	31:16	DATAOUT<31:0>																0000
		15:0																	0000
7040	PMDIN	31:16	DATAIN<31:0>																0000
		15:0																	0000
7050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	PTEN14	—	—	—	PTEN<10:0>											0000
7060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		—	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0>(1)		WAITM<3:0>(1)				WAITE<1:0>(1)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)
- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
- 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle(2)
- 01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle(2)
- 00 = No increment or decrement of address

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
- 11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)
- 10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)
- 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
- 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits(1)
- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits(1)
- 1111 = Wait of 16 TPB
- .
- .
- .
- 0001 = Wait of 2 TPB
- 0000 = Wait of 1 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NB	—	—	—	CH0SB<3:0>			
23:16	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA	—	—	—	CH0SA<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **CH0NB:** Negative Input Select bit for Sample B
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CH0SB<3:0>:** Positive Input Select bits for Sample B
1111 = Channel 0 positive input is Open(1)
1110 = Channel 0 positive input is IVREF(2)
1101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(3)
1100 = Channel 0 positive input is AN12(4)
•
•
•
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting(2)
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 22-20 **Unimplemented:** Read as '0'

bit 19-16 **CH0SA<3:0>:** Positive Input Select bits for Sample A Multiplexer Setting
1111 = Channel 0 positive input is Open(1)
1110 = Channel 0 positive input is IVREF(2)
1101 = Channel 0 positive input is CTMU temperature (CTMUT)(3)
1100 = Channel 0 positive input is AN12(4)
•
•
•
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0

bit 15-0 **Unimplemented:** Read as '0'

Note 1: This selection is only used with CTMU capacitive and time measurement.
2: See **Section 24.0 "Comparator Voltage Reference (CVREF)"** for more information.
3: See **Section 25.0 "Charge Time Measurement Unit (CTMU)"** for more information.
4: AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.

REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge1 must occur before Edge2 can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
11 = 100 times base current
10 = 10 times base current
01 = Base current level
00 = 1000 times base current(4)

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 30-41) in **Section 30.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

NOTES:

30.1 DC Characteristics

TABLE 30-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)(1)	Temp. Range (in °C)	Max. Frequency
			PIC32MX1XX/2XX 28/36/44-pin Family
DC5	2.3-3.6V	-40°C to +85°C	40 MHz
DC5b	2.3-3.6V	-40°C to +105°C	40 MHz

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
V-temp Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+105	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH) I/O Pin Power Dissipation: I/O = S (({VDD – VOH} x IOH) + S (VOL x IOL))	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 28-pin SSOP	θJA	71	—	°C/W	**1**
Package Thermal Resistance, 28-pin SOIC	θJA	50	—	°C/W	**1**
Package Thermal Resistance, 28-pin SPDIP	θJA	42	—	°C/W	**1**
Package Thermal Resistance, 28-pin QFN	θJA	35	—	°C/W	**1**
Package Thermal Resistance, 36-pin VTLA	θJA	31	—	°C/W	**1**
Package Thermal Resistance, 44-pin QFN	θJA	32	—	°C/W	**1**
Package Thermal Resistance, 44-pin TQFP	θJA	45	—	°C/W	**1**
Package Thermal Resistance, 44-pin VTLA	θJA	30	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O Pins with PMP	VSS	—	0.15 VDD	V	
		I/O Pins	VSS	—	0.2 VDD	V	
DI18		SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	VSS	—	0.8	V	SMBus enabled **(Note 4)**
	VIH	**Input High Voltage**					
DI20		I/O Pins not 5V-tolerant(5)	0.65 VDD	—	VDD	V	**(Note 4,6)**
		I/O Pins 5V-tolerant with PMP(5)	0.25 VDD + 0.8V	—	5.5	V	**(Note 4,6)**
		I/O Pins 5V-tolerant(5)	0.65 VDD	—	5.5	V	
DI28		SDAx, SCLx	0.65 VDD	—	5.5	V	SMBus disabled **(Note 4,6)**
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)**
DI30	ICNPU	**Change Notification Pull-up Current**	—	—	-50	µA	VDD = 3.3V, VPIN = VSS **(Note 3,6)**
DI31	ICNPD	**Change Notification Pull-down Current(4)**	—	—	-50	µA	VDD = 3.3V, VPIN = VDD
	IIL	**Input Leakage Current (Note 3)**					
DI50		I/O Ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{\text{MCLR}}$(2)	—	—	±1	µA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

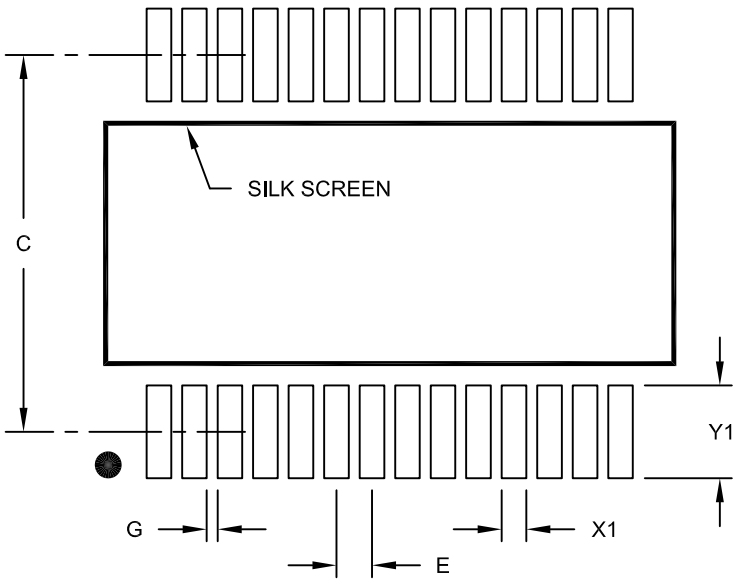
4: This parameter is characterized, but not tested in manufacturing.

5: See the **"Pin Diagrams"** section for the 5V-tolerant pins.

6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

Revision G (April 2015)

This revision includes the addition of the following devices:

- PIC32MX130F256B
- PIC32MX230F256B
- PIC32MX130F256D
- PIC32MX230F256D

The title of the document was updated to avoid confusion with the PIC32MX1XX/2XX/5XX 64/100-pin Family data sheet.

All peripheral SFR maps have been relocated from the Memory chapter to their respective peripheral chapters.

In addition, this revision includes the following major changes as described in Table A-6, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-6: MAJOR SECTION UPDATES

Section	Update Description
32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog	Added new devices to the family features (see Table 1 and Table 2). Updated pin diagrams to include new devices (see Pin Diagrams).
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Updated these sections: **2.2 "Decoupling Capacitors"**, **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**, **2.4 "Master Clear (MCLR) Pin"**, **2.8.1 "Crystal Oscillator Design Consideration"**
4.0 "Memory Organization"	Added Memory Map for new devices (see Figure 4-6).
14.0 "Watchdog Timer (WDT)"	New chapter created from content previously located in the Special Features chapter.
30.0 "Electrical Characteristics"	Removed parameter D312 (TSET) from the Comparator Specifications (see Table 30-12). Added the Comparator Voltage Reference Specifications (see Table 30-13). Updated Table 30-12.

Revision H (July 2015)

This revision includes the following major changes as described in Table A-7, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-7: MAJOR SECTION UPDATES

Section	Update Description
2.0 "Guidelines for Getting Started with 32-bit MCUs"	**Section 2.9 "Sosc Design Recommendation"** was removed.
8.0 "Oscillator Configuration"	The Primary Oscillator (POSC) logic in the Oscillator diagram was updated (see Figure 8-1).
30.0 "Electrical Characteristics"	The Power-Down Current (IPD) DC Characteristics parameter DC40k was updated (see Table 30-7). **Table 30-9: "DC Characteristics: I/O Pin Input Injection current Specifications"** was added.