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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128bt-v-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128bt-v-ss</a>

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 10: PIN NAMES FOR 44-PIN USB DEVICES**

44-PIN QFN (TOP VIEW) <sup>(1,2,3,5)</sup>			
<b>PIC32MX210F016D</b> <b>PIC32MX220F032D</b> <b>PIC32MX230F064D</b> <b>PIC32MX230F256D</b> <b>PIC32MX250F128D</b> <b>PIC32MX270F256D</b>			
		44	1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	VSS	28	VDD
7	VCAP	29	VSS
8	PGED2/RPB10/D+/CTED11/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/D-/RB11	31	OSC2/CLKO/RPA3/RA3
10	VUSB3V3	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4/TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4/TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14	36	AN12/RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVSS	38	RPC5/PMA3/RC5
17	AVDD	39	VSS
18	MCLR	40	VDD
19	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	41	RPB5/USBID/RB5
20	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	42	VBUS
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
  - 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
  - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
  - 4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.
  - 5: Shaded pins are 5V tolerant.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number <sup>(1)</sup>				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
SDA1	15	18	19	1	I/O	ST	Synchronous serial data input/output for I2C1
SCL2	4	7	2	24	I/O	ST	Synchronous serial clock input/output for I2C2
SDA2	3	6	1	23	I/O	ST	Synchronous serial data input/output for I2C2
TMS	19 <sup>(2)</sup>	22 <sup>(2)</sup>	25 <sup>(2)</sup>	12	I	ST	JTAG Test mode select pin
	11 <sup>(3)</sup>	14 <sup>(3)</sup>	15 <sup>(3)</sup>				
TCK	14	17	18	13	I	ST	JTAG test clock input pin
TDI	13	16	17	35	O	—	JTAG test data input pin
TDO	15	18	19	32	O	—	JTAG test data output pin
RTCC	4	7	2	24	O	ST	Real-Time Clock alarm output
CVREF-	28	3	34	20	I	Analog	Comparator Voltage Reference (low)
CVREF+	27	2	33	19	I	Analog	Comparator Voltage Reference (high)
CVREFOUT	22	25	28	14	O	Analog	Comparator Voltage Reference output
C1INA	4	7	2	24	I	Analog	Comparator Inputs
C1INB	3	6	1	23	I	Analog	
C1INC	2	5	36	22	I	Analog	
C1IND	1	4	35	21	I	Analog	
C2INA	2	5	36	22	I	Analog	
C2INB	1	4	35	21	I	Analog	
C2INC	4	7	2	24	I	Analog	
C2IND	3	6	1	23	I	Analog	
C3INA	23	26	29	15	I	Analog	
C3INB	22	25	28	14	I	Analog	
C3INC	27	2	33	19	I	Analog	
C3IND	1	4	35	21	I	Analog	
C1OUT	PPS	PPS	PPS	PPS	O	—	Comparator Outputs
C2OUT	PPS	PPS	PPS	PPS	O	—	
C3OUT	PPS	PPS	PPS	PPS	O	—	

**Legend:** CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels  
TTL = TTL input buffer

Analog = Analog input  
O = Output  
PPS = Peripheral Pin Select

P = Power  
I = Input  
— = N/A

**Note 1:** Pin numbers are provided for reference only. See the “**Pin Diagrams**” section for device pin availability.  
**2:** Pin number for PIC32MX1XX devices only.  
**3:** Pin number for PIC32MX2XX devices only.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number <sup>(1)</sup>				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
USBID	11 <sup>(3)</sup>	14 <sup>(3)</sup>	15 <sup>(3)</sup>	41 <sup>(3)</sup>	I	ST	USB OTG ID detect
CTED1	27	2	33	19	I	ST	CTMU External Edge Input
CTED2	28	3	34	20	I	ST	
CTED3	13	16	17	43	I	ST	
CTED4	15	18	19	1	I	ST	
CTED5	22	25	28	14	I	ST	
CTED6	23	26	29	15	I	ST	
CTED7	—	—	20	5	I	ST	
CTED8	—	—	—	13	I	ST	
CTED9	9	12	10	34	I	ST	
CTED10	14	17	18	44	I	ST	
CTED11	18	21	24	8	I	ST	
CTED12	2	5	36	22	I	ST	
CTED13	3	6	1	23	I	ST	
CTPLS	21	24	27	11	O	—	CTMU Pulse Output
PGED1	1	4	35	21	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	2	5	36	22	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	18	21	24	8	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	19	22	25	9	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
PGED3	11 <sup>(2)</sup>	14 <sup>(2)</sup>	15 <sup>(2)</sup>	41 <sup>(2)</sup>	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3
	27 <sup>(3)</sup>	2 <sup>(3)</sup>	33 <sup>(3)</sup>	19 <sup>(3)</sup>			
PGEC3	12 <sup>(2)</sup>	15 <sup>(2)</sup>	16 <sup>(2)</sup>	42 <sup>(2)</sup>	I	ST	Clock input pin for Programming/Debugging Communication Channel 3
	28 <sup>(3)</sup>	3 <sup>(3)</sup>	34 <sup>(3)</sup>	20 <sup>(3)</sup>			
PGED4	—	—	3	12	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 4
PGEC4	—	—	4	13	I	ST	Clock input pin for Programming/Debugging Communication Channel 4

**Legend:** CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels  
TTL = TTL input buffer

Analog = Analog input  
O = Output  
PPS = Peripheral Pin Select

P = Power  
I = Input  
— = N/A

**Note 1:** Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXDRMSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXDRMSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXDRMSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXDRMSZ<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **BMXDRMSZ<31:0>**: Data RAM Memory (DRM) Size bits

Static value that indicates the size of the Data RAM in bytes:

0x00001000 = Device has 4 KB RAM

0x00002000 = Device has 8 KB RAM

0x00004000 = Device has 16 KB RAM

0x00008000 = Device has 32 KB RAM

0x00010000 = Device has 64 KB RAM

**REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	BMXPUPBA<19:16>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
	BMXPUPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXPUPBA<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-20 **Unimplemented**: Read as '0'

bit 19-11 **BMXPUPBA<19:11>**: Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>**: Read-Only bits

This value is always '0', which forces 2 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

**2:** The value in this register must be less than or equal to BMXPFMSZ.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION**

Interrupt Source <sup>(1)</sup>	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
			Flag	Enable	Priority	Sub-priority	
Highest Natural Order Priority							
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1E – SPI1 Fault	36	31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1TX – SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX1XX 28/36/44-Pin General Purpose Family Features”** and **TABLE 2: “PIC32MX2XX 28/36/44-pin USB Family Features”** for the lists of available peripherals.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SRIPL<2:0> <sup>(1)</sup>		
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	VEC<5:0> <sup>(1)</sup>					

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits<sup>(1)</sup>

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits<sup>(1)</sup>

11111-00000 = The interrupt vector that is presented to the CPU

**Note 1:** This value should only be used when the interrupt controller is configured for Single Vector mode.

**REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits

Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

## 10.1 USB Control Registers

**TABLE 10-1: USB REGISTER MAP**

Virtual Address (BF88-#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5040	U1OTGIR <sup>(2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTGSTAT <sup>(3)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND <sup>(4)</sup>	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
5200	U1IR <sup>(2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF DETACHIF	0000 0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE DETACHIE	0000 0000
5220	U1EIR <sup>(2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF	PIDEF	0000 0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE EOFEE	PIDEE	0000 0000
5240	U1STAT <sup>(3)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE	SE0	PKTDIS TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN SOFEN	0000 0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<15:9>							—	0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

**2:** This register does not have associated SET and INV registers.

**3:** This register does not have associated CLR, SET and INV registers.

**4:** Reset value for this bit is undefined.



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 10-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	FRMH<2:0>		

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

**REGISTER 10-15: U1TOK: USB TOKEN REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PID<3:0> <sup>(1)</sup>				EP<3:0>			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits<sup>(1)</sup>

1101 = SETUP (TX) token type transaction

1001 = IN (RX) token type transaction

0001 = OUT (TX) token type transaction

**Note:** All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits

The four bit value must specify a valid endpoint.

**Note 1:** All other values are reserved and must not be used.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 11.0 I/O PORTS

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. “I/O Ports”** (DS60001120), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions.

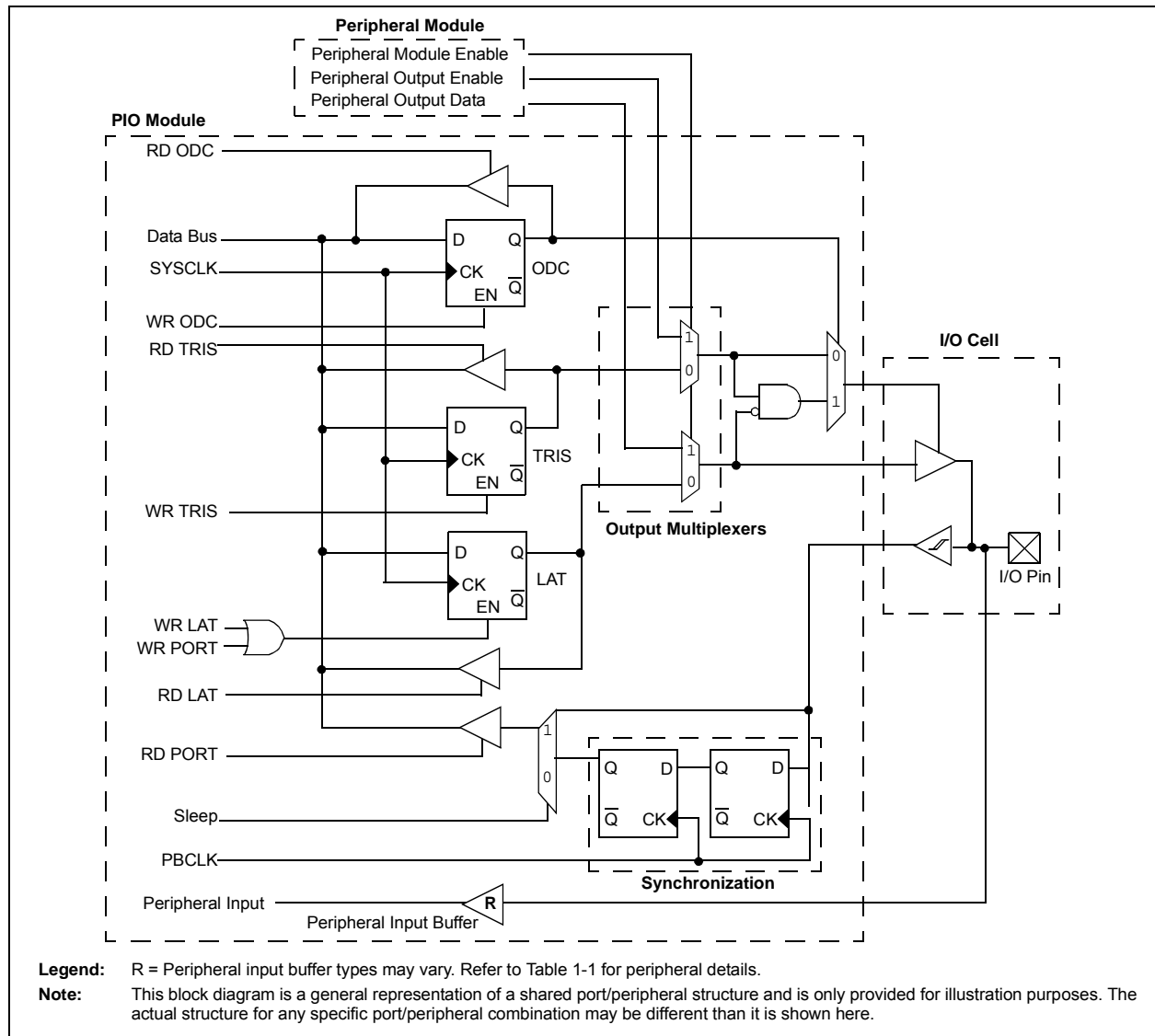
These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Key features of this module include:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 3      **Unimplemented:** Read as '0'
- bit 2      **TSYNC:** Timer External Clock Input Synchronization Selection bit  
When TCS = 1:  
1 = External clock input is synchronized  
0 = External clock input is not synchronized  
When TCS = 0:  
This bit is ignored.
- bit 1      **TCS:** Timer Clock Source Select bit  
1 = External clock from TxCKI pin  
0 = Internal peripheral clock
- bit 0      **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## 18.0 INTER-INTEGRATED CIRCUIT (I<sup>2</sup>C)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I<sup>2</sup>C)”** (DS60001116), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The I<sup>2</sup>C module provides complete hardware support for both Slave and Multi-Master modes of the I<sup>2</sup>C serial communication standard. Figure 18-1 illustrates the I<sup>2</sup>C module block diagram.

Each I<sup>2</sup>C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I<sup>2</sup>C module offers the following key features:

- I<sup>2</sup>C interface supporting both master and slave operation
- I<sup>2</sup>C Slave mode supports 7-bit and 10-bit addressing
- I<sup>2</sup>C Master mode supports 7-bit and 10-bit addressing
- I<sup>2</sup>C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I<sup>2</sup>C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I<sup>2</sup>C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 19-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5     **ABAUD**: Auto-Baud Enable bit  
          1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55);  
              cleared by hardware upon completion  
          0 = Baud rate measurement disabled or completed
- bit 4     **RXINV**: Receive Polarity Inversion bit  
          1 = UxRX Idle state is '0'  
          0 = UxRX Idle state is '1'
- bit 3     **BRGH**: High Baud Rate Enable bit  
          1 = High-Speed mode – 4x baud clock enabled  
          0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1   **PDSEL<1:0>**: Parity and Data Selection bits  
          11 = 9-bit data, no parity  
          10 = 8-bit data, odd parity  
          01 = 8-bit data, even parity  
          00 = 8-bit data, no parity
- bit 0     **STSEL**: Stop Selection bit  
          1 = 2 Stop bits  
          0 = 1 Stop bit

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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NOTES:

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON <sup>(1)</sup>	COE	CPOL <sup>(2)</sup>	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit<sup>(1)</sup>

1 = Module is enabled. Setting this bit does not affect the other bits in this register

0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is driven on the output CxOUT pin

0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit<sup>(2)</sup>

1 = Output is inverted

0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit

1 = Output of the Comparator is a '1'

0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits

11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output

10 = Comparator interrupt is generated on a high-to-low transition of the comparator output

01 = Comparator interrupt is generated on a low-to-high transition of the comparator output

00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit

1 = Comparator non-inverting input is connected to the internal CVREF

0 = Comparator non-inverting input is connected to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator

11 = Comparator inverting input is connected to the IVREF

10 = Comparator inverting input is connected to the CxIND pin

01 = Comparator inverting input is connected to the CxINC pin

00 = Comparator inverting input is connected to the CxINB pin

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

## 25.1 CTMU Control Registers

TABLE 25-1: CTMU REGISTER MAP

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits														All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2		17/1	16/0
A200	CTMUCON	31:16	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
		15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	ITRIM<5:0>				IRNG<1:0>		0000		

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.



**TABLE 26-2: PERIPHERAL MODULE DISABLE REGISTER MAP**

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F240	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CVRMD	—	—	—	CTMUMD	—	—	—	—	—	—	—	AD1MD	0000
F250	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F260	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	OC5MD	OC4MD	OC3MD	0000
F270	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F280	PMD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F290	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-6: DC CHARACTERISTICS: IDLE CURRENT (I<sub>IDLE</sub>)**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Parameter No.	Typical <sup>(2)</sup>	Max.	Units	Conditions		
Idle Current (I <sub>IDLE</sub> ): Core Off, Clock on Base Current (Notes 1, 4)						
DC30a	1	1.5	mA	4 MHz (Note 3)		
DC31a	2	3	mA	10 MHz		
DC32a	4	6	mA	20 MHz (Note 3)		
DC33a	5.5	8	mA	30 MHz (Note 3)		
DC34a	7.5	11	mA	40 MHz		
DC37a	100	—	μA	-40°C	3.3V	LPRC (31 kHz) (Note 3)
DC37b	250	—	μA	+25°C		
DC37c	380	—	μA	+85°C		

**Note 1:** The test conditions for I<sub>IDLE</sub> current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
  - OSC2/CLKO is configured as an I/O input pin
  - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
  - CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
  - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
  - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
  - All I/O pins are configured as inputs and pulled to V<sub>SS</sub>
  - MCLR = V<sub>DD</sub>
  - RTCC and JTAG are disabled
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** This parameter is characterized, but not tested in manufacturing.
- 4:** I<sub>IDLE</sub> electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-12: DC CHARACTERISTICS: PROGRAM MEMORY**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
<b>Program Flash Memory<sup>(3)</sup></b>							
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
	TWW	Word Write Cycle Time	—	411	—	FRC Cycles	See <b>Note 4</b>
D136	TRW	Row Write Cycle Time	—	6675	—		See <b>Note 2,4</b>
D137	TPE	Page Erase Cycle Time	—	20011	—		See <b>Note 4</b>
	TCE	Chip Erase Cycle Time	—	80180	—		See <b>Note 4</b>

**Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

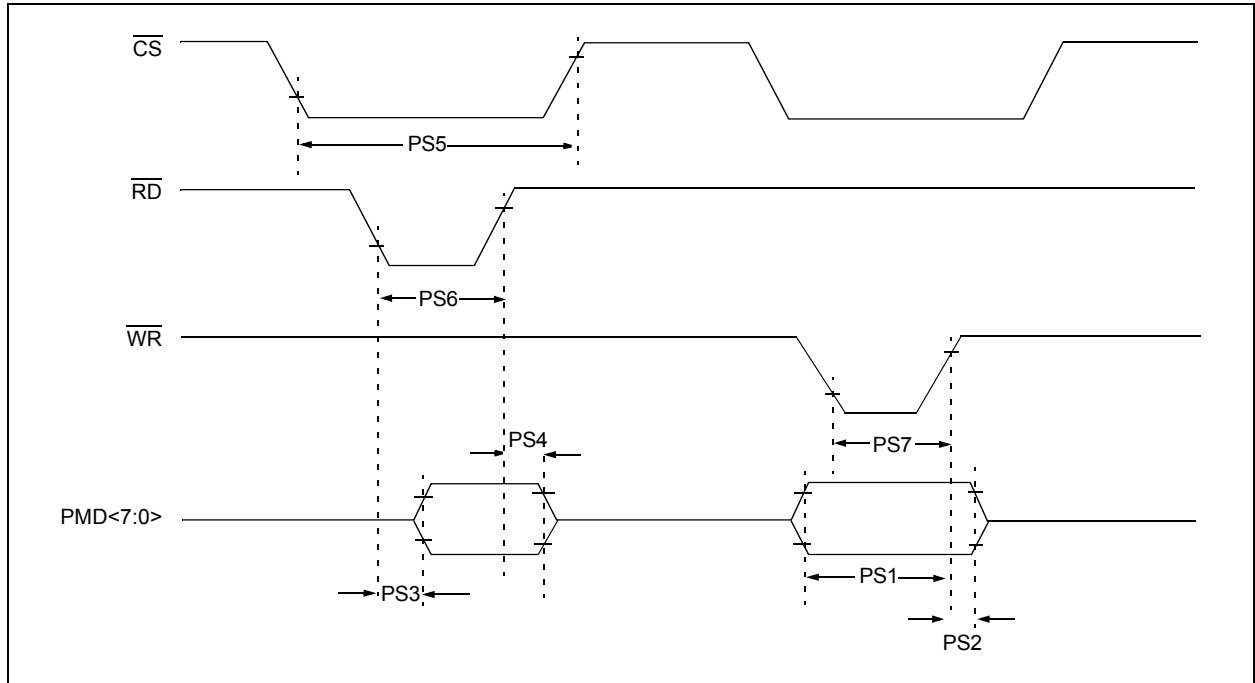
**2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the “PIC32 Flash Programming Specification” (DS60001145) for operating conditions during programming and erase cycles.

**4:** This parameter depends on FRC accuracy (See Table 30-19) and FRC tuning values (See Register 8-2).

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FIGURE 30-20: PARALLEL SLAVE PORT TIMING



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## Revision E (October 2012)

All singular pin diagram occurrences of CVREF were changed to: CVREFOUT. In addition, minor text and formatting changes were incorporated throughout the document.

All major changes are referenced by their respective section in Table A-4.

**TABLE A-4: MAJOR SECTION UPDATES**

Section	Update Description
<b>“32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog”</b>	Updated the following feature sections: <ul style="list-style-type: none"><li>• <b>“Operating Conditions”</b></li><li>• <b>“Communication Interfaces”</b></li></ul>
<b>2.0 “Guidelines for Getting Started with 32-bit MCUs”</b>	Removed Section 2.8 “Configuration of Analog and Digital Pins During ICSP Operations”.
<b>3.0 “CPU”</b>	Removed references to GPR shadow registers in <b>3.1 “Features”</b> and <b>3.2.1 “Execution Unit”</b> .
<b>4.0 “Memory Organization”</b>	Updated the BRG bit range in the SPI1 and SPI2 Register Map (see Table 4-8). Added the PWP<6> bit to the Device Configuration Word Summary (see Table 4-17).
<b>5.0 “Flash Program Memory”</b>	Added a note with Flash page size and row size information.
<b>7.0 “Interrupt Controller”</b>	Updated the TPC<2:0> bit definitions (see Register 7-1). Updated the IPTMR<31:0> bit definition (see Register 7-3).
<b>8.0 “Oscillator Configuration”</b>	Updated the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1). Updated the RODIV<14:0> bit definitions (see Register 8-3).
<b>10.0 “USB On-The-Go (OTG)”</b>	Updated the Notes in the USB Interface Diagram (see Figure 10-1).
<b>18.0 “Universal Asynchronous Receiver Transmitter (UART)”</b>	Updated the baud rate range in the list of primary features.
<b>26.0 “Special Features”</b>	Added the PWP<6> bit to the Device Configuration Word 0 (see Register 26-1).
<b>29.0 “Electrical Characteristics”</b>	Added Note 1 to Operating MIPS vs. Voltage (see Table 29-1). Added Note 2 to DC Temperature and Voltage Specifications (see Table 29-4). Updated the Conditions for parameter DC25 in DC Characteristics: Operating Current (IDD) (see Table 29-5). Added Note 2 to Electrical Characteristics: BOR (see Table 29-10). Added Note 4 to Comparator Specifications (see Table 29-12). Added Note 5 to ADC Module Specifications (see Table 29-32). Updated the 10-bit Conversion Rate Parameters and added Note 3 (see Table 29-33). Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 29-34). Added Note 3 to CTMU Current Source Specifications (see Table 29-39).
<b>30.0 “50 MHz Electrical Characteristics”</b>	New chapter with electrical characteristics for 50 MHz devices.
<b>31.0 “Packaging Information”</b>	The 36-pin and 44-pin VTLA packages have been updated.