Microchip Technology - PIC32MX250F128C-50I/TL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128c-50i-tl

TABLE 12: PIN NAMES FOR 44-PIN USB DEVICES

44-PIN TQFP (TOP VIEW)(1,2,3,5)

PIC32MX210F016D
PIC32MX220F032D
PIC32MX230F064D
PIC32MX230F256D
PIC32MX250F128D
PIC32MX270F256D

44

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	VSS	28	VDD
7	VCAP	29	VSS
8	PGED2/RPB10/D+/CTED11/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/D-/RB11	31	OSC2/CLKO/RPA3/RA3
10	VUSB3V3	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4(4)/TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4(4)/TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14	36	AN12/RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVSS	38	RPC5/PMA3/RC5
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	41	RPB5/USBID/RB5
20	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	42	VBUS
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: This pin function is not available on PIC32MX210F016D and PIC32MX220F032D devices.

5: Shaded pins are 5V tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		—	—	27	O	—	Parallel Master Port address (Demultiplexed Master modes)
PMA3		—	—	38	O	—	
PMA4		—	—	37	O	—	
PMA5		—	—	4	O	—	
PMA6		—	—	5	O	—	
PMA7		—	—	13	O	—	
PMA8		—	—	32	O	—	
PMA9		—	—	35	O	—	
PMA10		—	—	12	O	—	
PMCS1	23	26	29	15	O	—	Parallel Master Port Chip Select 1 strobe
PMD0	20(2)	23(2)	26(2)	10(2)	I/O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes)
	1(3)	4(3)	35(3)	21(3)			
PMD1	19(2)	22(2)	25(2)	9(2)	I/O	TTL/ST	
	2(3)	5(3)	36(3)	22(3)			
PMD2	18(2)	21(2)	24(2)	8(2)	I/O	TTL/ST	
	3(3)	6(3)	1(3)	23(3)			
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12(2)	15(2)	16(2)	42(2)	I/O	TTL/ST	
	28(3)	3(3)	34(3)	20(3)			
PMD7	11(2)	14(2)	15(2)	41(2)	I/O	TTL/ST	
	27(3)	2(3)	33(3)	19(3)			
PMRD	21	24	27	11	O	—	Parallel Master Port read strobe
PMWR	22(2)	25(2)	28(2)	14(2)	O	—	Parallel Master Port write strobe
	4(3)	7(3)	2(3)	24(3)			
VBUS	12(3)	15(3)	16(3)	42(3)	I	Analog	USB bus power monitor
VUSB3V3	20(3)	23(3)	26(3)	10(3)	P	—	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22(3)	25(3)	28(3)	14(3)	O	—	USB Host and OTG bus power control output
D+	18(3)	21(3)	24(3)	8(3)	I/O	Analog	USB D+
D-	19(3)	22(3)	25(3)	9(3)	I/O	Analog	USB D-

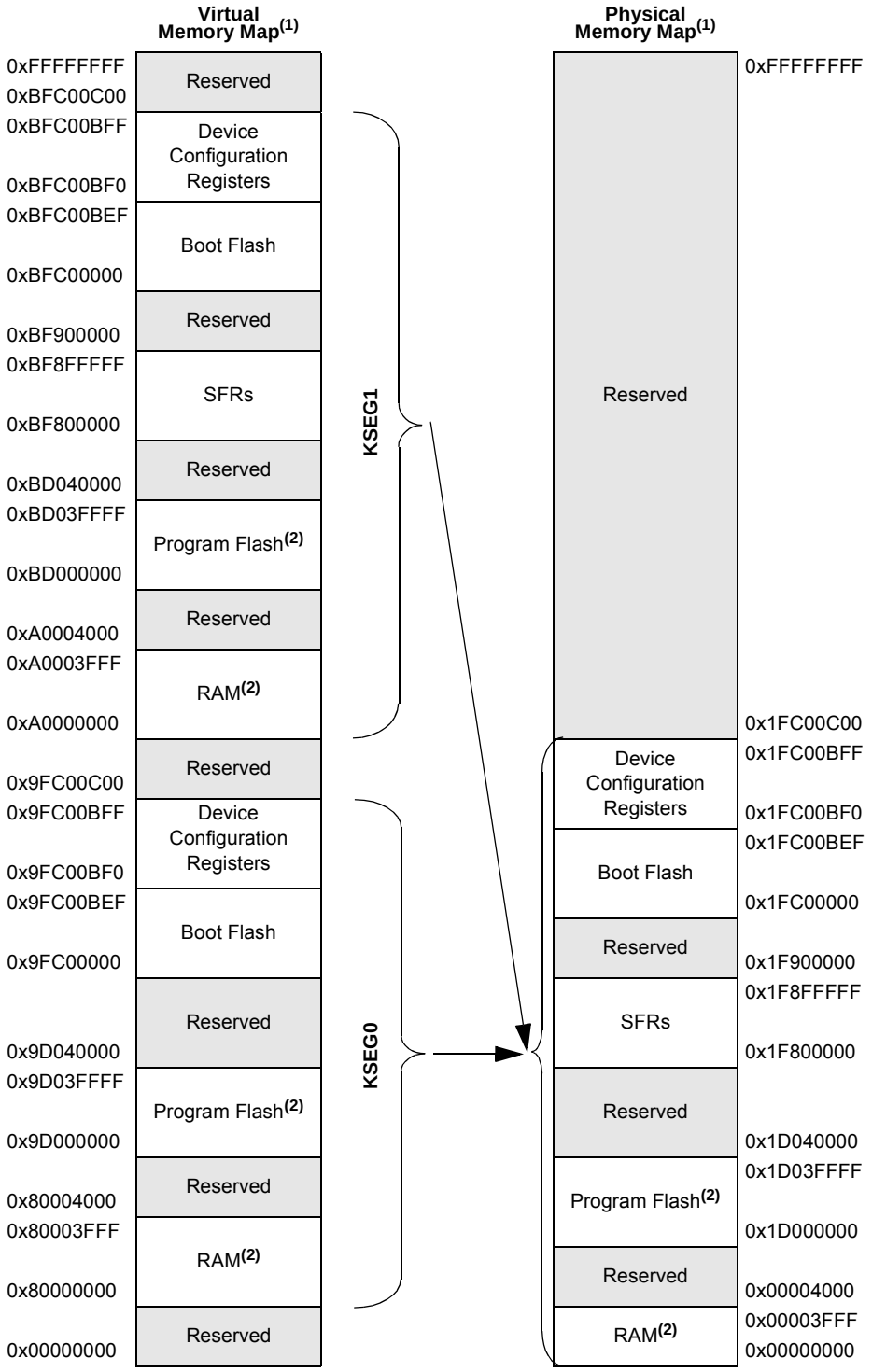
Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 256 KB FLASH)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXPFMSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXPFMSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXPFMSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXPFMSZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXPFMSZ<31:0>:** Program Flash Memory (PFM) Size bits
Static value that indicates the size of the PFM in bytes:
0x00004000 = Device has 16 KB Flash
0x00008000 = Device has 32 KB Flash
0x00010000 = Device has 64 KB Flash
0x00020000 = Device has 128 KB Flash
0x00040000 = Device has 256 KB Flash

REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXBOOTSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXBOOTSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXBOOTSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXBOOTSZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits
Static value that indicates the size of the Boot PFM in bytes:
0x00000C00 = Device has 3 KB boot Flash

REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** Unlock Register bits
These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** Flash Address bits
Bulk/Chip/PFM Erase: Address is ignored.
Page Erase: Address identifies the page to erase.
Row Program: Address identifies the row to program.
Word Program: Address identifies the word to program.

8.0 OSCILLATOR CONFIGURATION

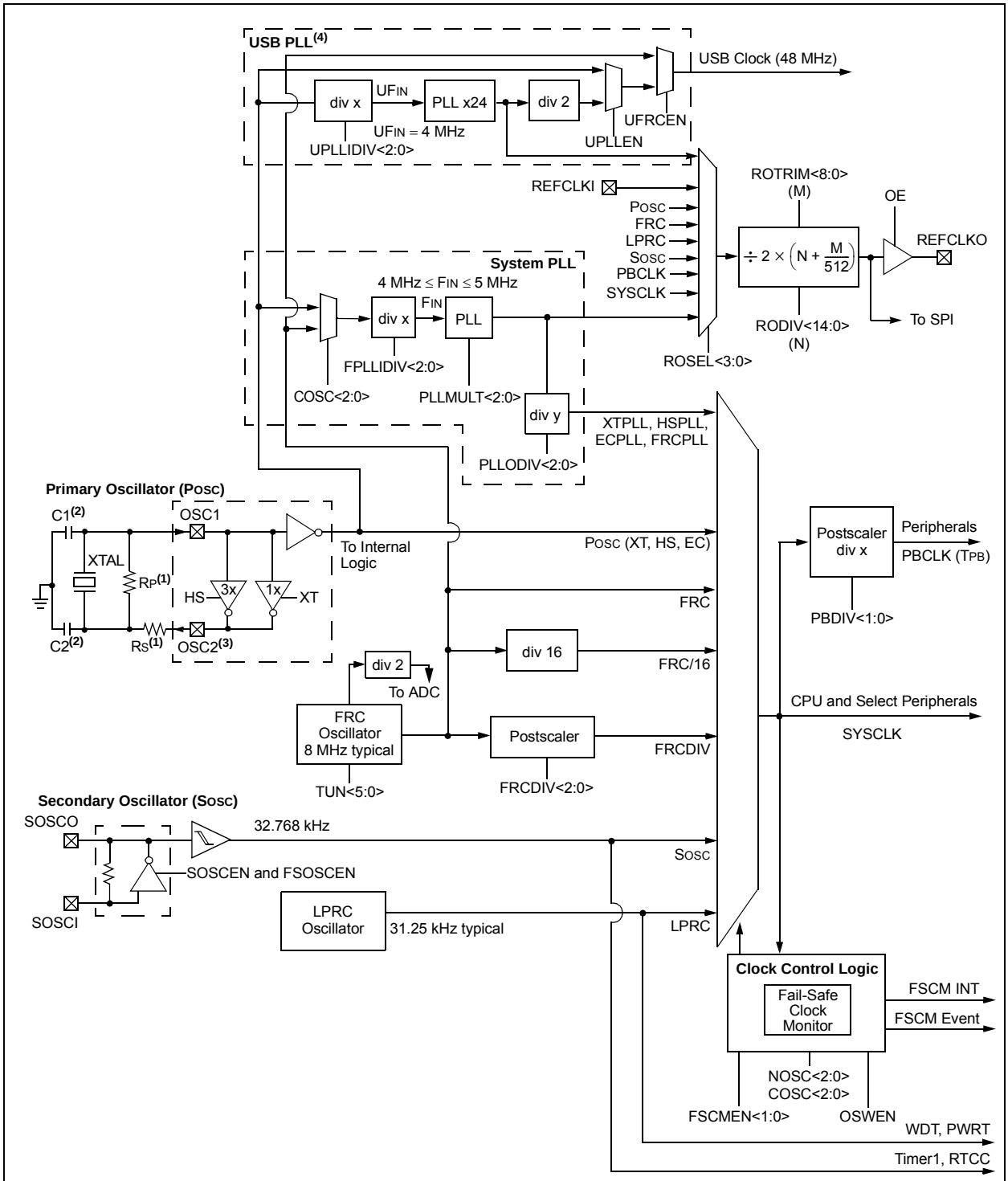
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Oscillator Configuration"** (DS60001112), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MX1XX/2XX 28/36/44-pin Family oscillator system has the following modules and features:

- Four external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

A block diagram of the oscillator system is provided in Figure 8-1.

FIGURE 8-1: OSCILLATOR DIAGRAM



Notes:
1. A series resistor, RS, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP, with a value of 1 MΩ.
2. Refer to **Section 6. "Oscillator Configuration"** (DS60001112) in the "*PIC32 Family Reference Manual*" for help in determining the best oscillator components.
3. The PBCLK out is only available on the OSC2 pin in certain clock modes.
4. The USB PLL is only available on PIC32MX2XX devices.

REGISTER 18-1: I2CxCON: I²C CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:	HC = Cleared in Hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** I²C Enable bit(1)
- 1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins
- 0 = Disables the I²C module; all I²C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
- 1 = Release SCLx clock
- 0 = Hold SCLx clock low (clock stretch)

If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit
- 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
- 0 = Strict I²C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Slave Address bit
- 1 = I2CxADD is a 10-bit slave address
- 0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
- 1 = Slew rate control disabled
- 0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit
- 1 = Enable I/O pin thresholds compliant with SMBus specification
- 0 = Disable SMBus input thresholds

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 19-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved; do not use
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

REGISTER 20-5: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HSC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HSC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HSC = Set by Hardware; Cleared by Software		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
- 0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits
- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CAL<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAL<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON(1,2)	—	SIDL	—	—	—	—	—
7:0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0
	RTSECSEL(3)	RTCCLKON	—	—	RTCWREN(4)	RTCSYNC	HALFSEC(5)	RTCOE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** RTC Drift Calibration bits, which contain a signed 10-bit integer value

0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute
0000000000 = No adjustment
1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute
•
•
•
1000000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute

bit 15 **ON:** RTCC On bit(1,2)

1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Disables the PBCLK to the RTCC when the device enters Idle mode
0 = Continue normal operation when the device enters Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **RTSECSEL:** RTCC Seconds Clock Output Select bit(3)

1 = RTCC Seconds Clock is selected for the RTCC pin
0 = RTCC Alarm Pulse is selected for the RTCC pin

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit

1 = RTCC Clock is actively running
0 = RTCC Clock is not running

Note 1: The ON bit is only writable when RTCWREN = 1.

2: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

3: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

4: The RTCWREN bit can be set only when the write sequence is enabled.

5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

22.1 ADC Control Registers

TABLE 22-1: ADC REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	AD1CON1(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE	0000
9010	AD1CON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG<2:0>			OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000
9020	AD1CON3(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>								0000
9040	AD1CHS(1)	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9050	AD1CSSL(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16	ADC Result Word 0 (ADC1BUF0<31:0>)																0000
		15:0																	0000
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)																0000
		15:0																	0000
9090	ADC1BUF2	31:16	ADC Result Word 2 (ADC1BUF2<31:0>)																0000
		15:0																	0000
90A0	ADC1BUF3	31:16	ADC Result Word 3 (ADC1BUF3<31:0>)																0000
		15:0																	0000
90B0	ADC1BUF4	31:16	ADC Result Word 4 (ADC1BUF4<31:0>)																0000
		15:0																	0000
90C0	ADC1BUF5	31:16	ADC Result Word 5 (ADC1BUF5<31:0>)																0000
		15:0																	0000
90D0	ADC1BUF6	31:16	ADC Result Word 6 (ADC1BUF6<31:0>)																0000
		15:0																	0000
90E0	ADC1BUF7	31:16	ADC Result Word 7 (ADC1BUF7<31:0>)																0000
		15:0																	0000
90F0	ADC1BUF8	31:16	ADC Result Word 8 (ADC1BUF8<31:0>)																0000
		15:0																	0000
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)																0000
		15:0																	0000
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for details.

TABLE 30-9: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(2,5)	mA	This parameter applies to all pins, with the exception of the power pins.
DI60b	IICH	**Input High Injection Current**	0	—	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, and the SOSCI, SOSCO, OSC1, D+, and D- pins.
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and Control pins)**	-20(6)	—	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT)

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 3**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

30.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX 28/36/44-pin Family AC characteristics and timing parameters.

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

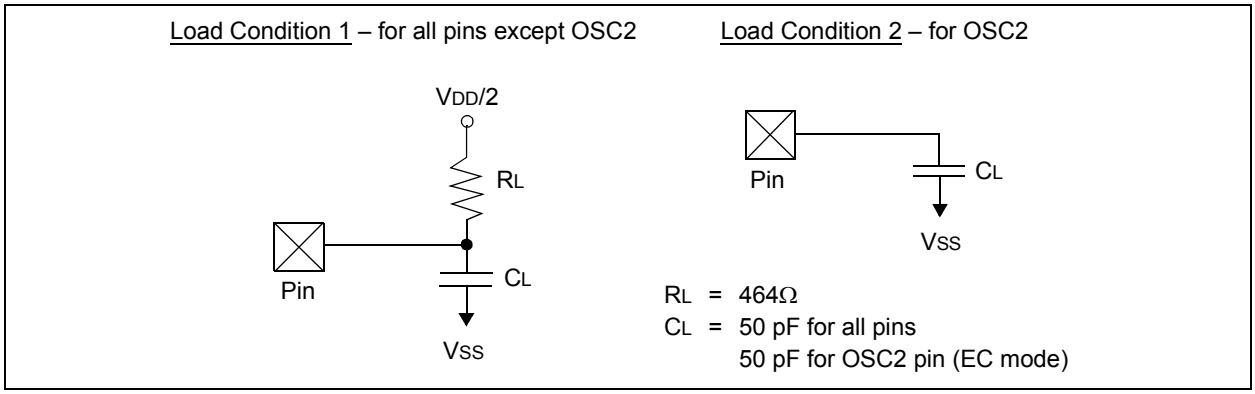


TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO56	CIO	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-2: EXTERNAL CLOCK TIMING

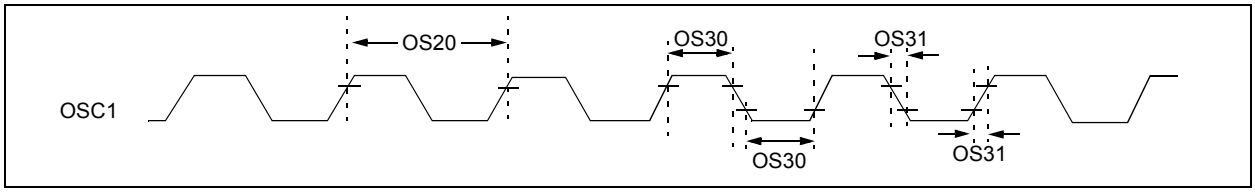
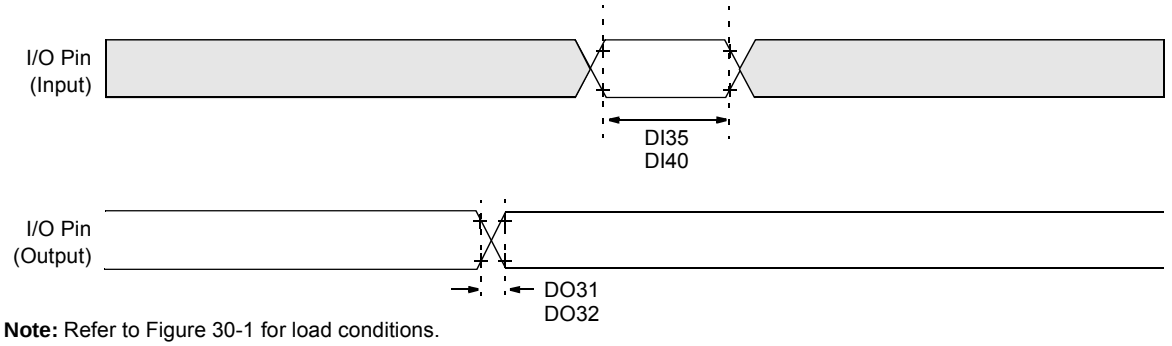


FIGURE 30-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

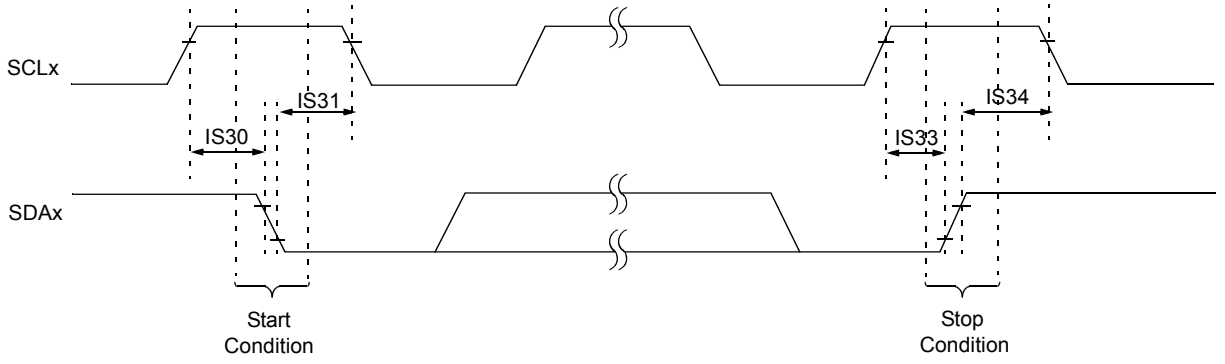
TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	5	15	ns	VDD < 2.5V
			—	5	10	ns	VDD > 2.5V
DO32	TIOF	Port Output Fall Time	—	5	15	ns	VDD < 2.5V
			—	5	10	ns	VDD > 2.5V
DI35	TINP	INTx Pin High or Low Time	10	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TSYSCLK	—

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

FIGURE 30-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 30-1 for load conditions.

FIGURE 30-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

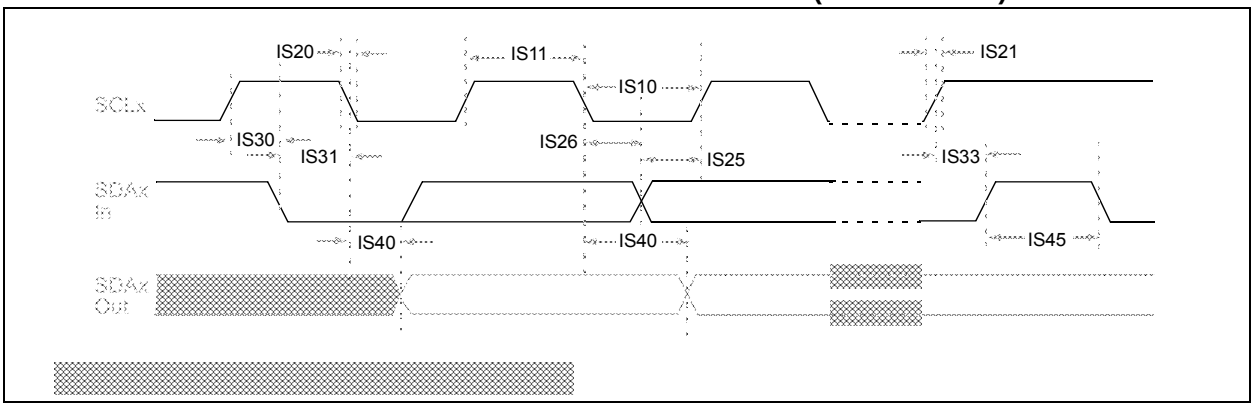


FIGURE 32-6: TYPICAL FRC FREQUENCY @ VDD = 3.3V

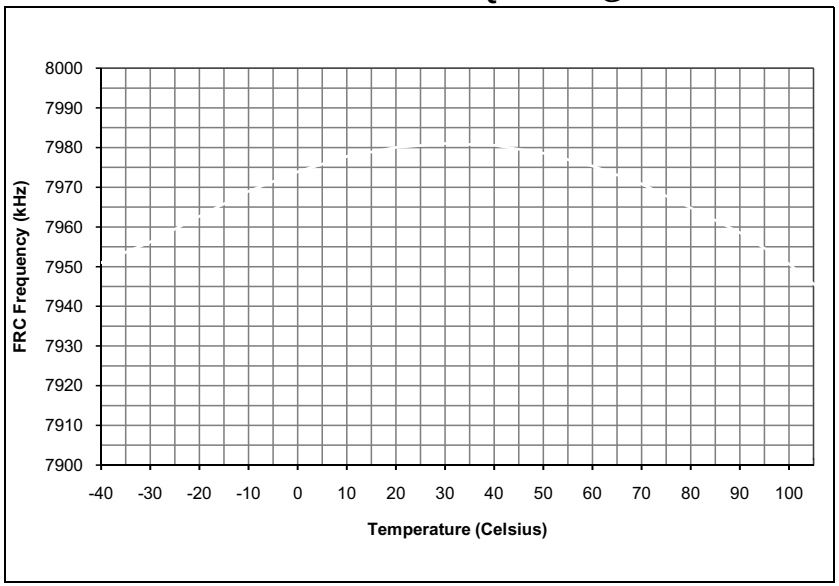


FIGURE 32-7: TYPICAL LPRC FREQUENCY @ VDD = 3.3V

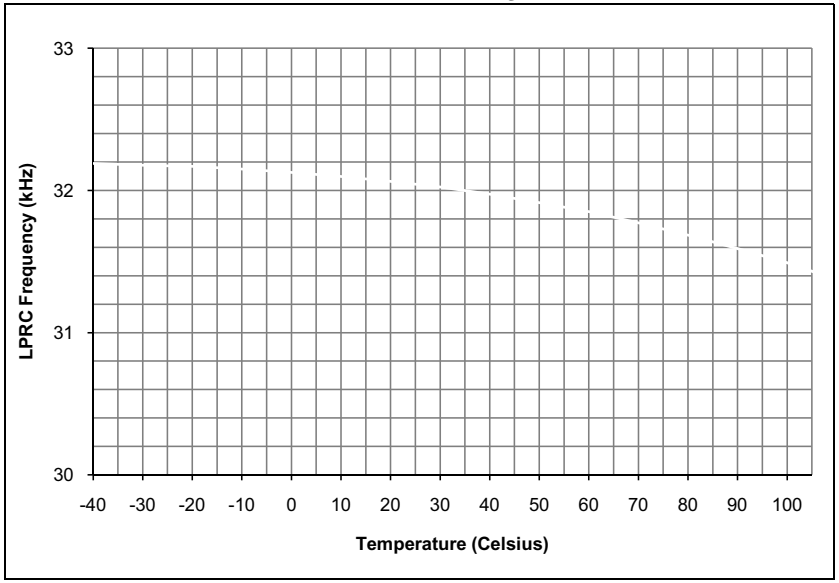
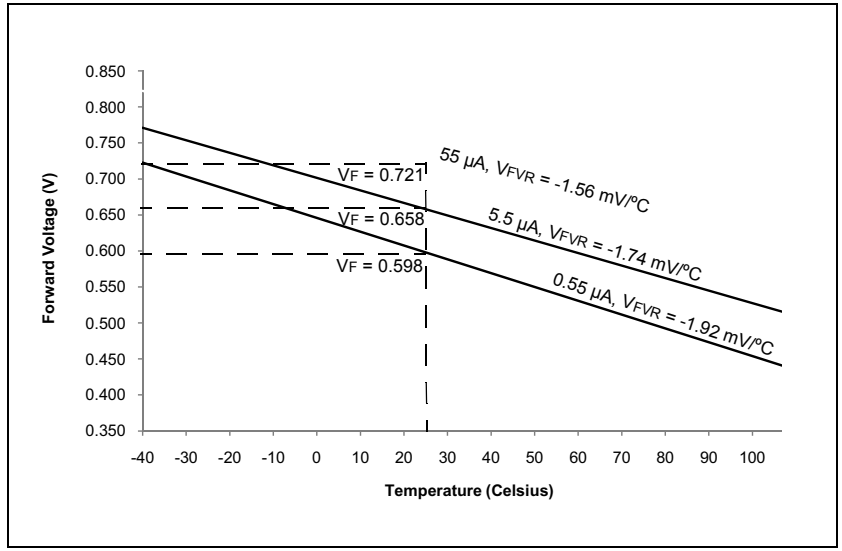


FIGURE 32-8: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE



NOTES:

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section	Update Description
29.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings (removed Voltage on VCORE with respect to VSS). Added the SPDIP specification to the Thermal Packaging Characteristics (see Table 29-2). Updated the Typical values for parameters DC20-DC24 in the Operating Current (IDD) specification (see Table 29-5). Updated the Typical values for parameters DC30a-DC34a in the Idle Current (IIDLE) specification (see Table 29-6). Updated the Typical values for parameters DC40i and DC40n and removed parameter DC40m in the Power-down Current (IPD) specification (see Table 29-7). Removed parameter D320 (VCORE) from the Internal Voltage Regulator Specifications and updated the Comments (see Table 29-13). Updated the Minimum, Typical, and Maximum values for parameter F20b in the Internal FRC Accuracy specification (see Table 29-17). Removed parameter SY01 (TPWRT) and removed all Conditions from Resets Timing (see Table 29-20). Updated all parameters in the CTMU Specifications (see Table 29-39).
31.0 "Packaging Information"	Added the 28-lead SPDIP package diagram information (see **31.1 "Package Marking Information"** and **31.2 "Package Details"**).
"Product Identification System**"**	Added the SPDIP (SP) package definition.

Revision C (November 2011)

All major changes are referenced by their respective section in Table A-2.

TABLE A-2: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog**"**	Revised the source/sink on I/O pins (see **"Input/Output"** on page 1). Added the SPDIP package to the PIC32MX220F032B device in the PIC32MX2XX USB Family Features (see Table 2).
4.0 "Memory Organization"	Removed ANSB6 from the ANSELB register and added the ODCB6, ODCB10, and ODCB11 bits in the PORTB Register Map (see Table 4-20).
29.0 "Electrical Characteristics"	Updated the minimum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 29-16).