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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128c-i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e<sup>®</sup> Support
- · Enhanced JTAG (EJTAG) Controller

### 3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- · 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- · Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

## 3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

# TABLE 3-1:MIPS32<sup>®</sup> M4K<sup>®</sup> PROCESSOR CORE HIGH-PERFORMANCE INTEGERMULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul rt) (div rs)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU,	16 bits	1	1
MSUB/MSUBU	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

### TABLE 4-1: SFR MEMORY MAP

	Virtual Ac	ddress
Peripheral	Base	Offset Start
Watchdog Timer		0x0000
RTCC		0x0200
Timer1-5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
IC1 and IC2		0x5000
SPI1 and SPI2		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC	0xBF80	0x9000
CVREF		0x9800
Comparator		0xA000
CTMU		0xA200
Oscillator		0xF000
Device and Revision ID		0xF220
Peripheral Module Disable		0xF240
Flash Controller		0xF400
Reset		0xF600
PPS		0xFA04
Interrupts		0x1000
Bus Matrix		0x2000
DMA	0xBF88	0x3000
USB		0x5050
PORTA-PORTC		0x6000
Configuration	0xBFC0	0x0BF0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31.24	CHSSA<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:10	CHSSA<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHSSA<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0				CHSSA	<7:0>						

## **REGISTER 9-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER**

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

 bit 31-0
 CHSSA<31:0> Channel Source Start Address bits

 Channel source start address.

 Note: This must be the physical address of the source.

#### **REGISTER 9-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
01.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31:24				CHDSA<	31:24>					
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	CHDSA<23:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CHDSA<15:8>									
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0	CHDSA<7:0>									

Legend:			
R = Readable bit	W = Writable bit U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits Channel destination start address.

 $\ensuremath{\textbf{Note:}}$  This must be the physical address of the destination.

### TABLE 11-4: PORTB REGISTER MAP

ess										Bits									
Virtual Addr (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6100	ANSEL B	31:16	_	—	—	—	-	-	_	—	-	-	—	_	_	—	—	—	0000
0100	,	15:0	ANSB15	ANSB14	ANSB13	ANSB12 <sup>(2)</sup>	_		—	—	_	_	—	—	ANSB3	ANSB2	ANSB1	ANSB0	E00F
6110	TRISB	31:16	_	_	_	—	—	_	—	—	—		—	_	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12(2)	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6(2)	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6120	PORTB	31:16	_		_		_	—	_	_	_		_						0000
		15:0	RB15	RB14	RB13	RB12(2)	RB11	RB10	RB9	RB8	RB7	RC6(2)	RB5	RB4	RB3	RB2	RB1	RB0	XXXX
6130	LATB	31:16		-	-		-	-	—	-			-	-	—	—	-	—	0000
		15:0	LAIB15	LAIB14	LAIB13	LAIB12(2)	LAI B11	LAIB10	LATB9	LAI B8	LAIB7	LAIB6(2)	LAI B5	LAI B4	LATB3	LATB2	LAIB1	LAIBO	XXXX
6140	ODCB	31:16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB1	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCR0	0000
6150	CNPUB	31:16																	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12-	CNPUBIT	CNPUBIU	CNPUB9	CNPUB8	CNPUB/	CNPUB6-	CNP0B5	CNPUB4	CNP0B3	CNP0B2	CNPUBI	CNPUBU	0000
6160	CNPDB	31:10																	0000
		15.0	CNPDB15	CINPUB14	CNPDB13	CNPDB12	CNPDBT	CNPDBIU	CNPDB9	CNPDBo	CNPDB/	CNPDB0-	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDBI	CNPDBU	0000
6170	CNCONB	15.0			SIDI														0000
		31.16																	0000
6180	CNENB	15.0	CNIEB15	CNIEB14	CNIEB13	CNIEB11(2)	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6(2)	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
		31:16	_	_	_	_	_	_				_							0000
6190	CNSTATB		CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	CN	
		15:0	STATB15	STATB14	STATB13	STATB12(2)	STATB11	STATB10	STATB9	STATB8	STATB7	STATB6 <sup>(2)</sup>	STATB5	STATB4	STATB3	STATB2	STATB1	STATB0	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: This bit is not available on PIC32MX2XX devices. The reset value for the TRISB register when this bit is not available is 0x0000EFBF.

## 13.0 TIMER2/3, TIMER4/5

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a freerunning interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- · Synchronous external 16-bit timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

- Synchronous internal 32-bit timer
- · Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

Note:	In this chapter, references to registers,
	TxCON, TMRx and PRx, use 'x' to
	represent Timer2 through Timer5 in 16-bit
	modes. In 32-bit modes, 'x' represents
	Timer2 or Timer4 and 'y' represents
	Timer3 or Timer5.

## **13.1 Additional Supported Features**

- · Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 in 16-bit mode, Timer2/3 in 32-bit mode)
- Fast bit manipulation using CLR, SET and INV registers

Figure 13-1 and Figure 13-2 illustrate block diagrams of Timer2/3 and Timer4/5.

## FIGURE 13-1: TIMER2-TIMER5 BLOCK DIAGRAM (16-BIT)



REGIST	ER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)								
bit 17	SPIFE: Frame Sync Pulse Edge Select bit (Framed SPI mode only)								
	1 = Frame synchronization pulse coincides with the first bit clock								
bit 16	<b>ENHBLIE</b> : Enhanced Buffer Enable bit <sup>(2)</sup>								
Sit 10	1 = Enhanced Buffer mode is enabled								
	0 = Enhanced Buffer mode is disabled								
bit 15	ON: SPI Peripheral On bit <sup>(1)</sup>								
	1 = SPI Peripheral is enabled								
hit 14	Unimplemented: Read as '0'								
bit 13	SIDL: Stop in Idle Mode bit								
	1 = Discontinue module operation when the device enters Idle mode								
	0 = Continue module operation when the device enters Idle mode								
bit 12	<b>DISSDO:</b> Disable SDOx pin bit								
	1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register $0 = SDOx pin is controlled by the module$								
bit 11-10	MODE<32.16>: 32/16-Bit Communication Select bits								
	When AUDEN = 1:								
	MODE32 MODE16 Communication								
	1 1 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame								
	1 0 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame								
	0 0 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame								
	When AUDEN = 0:								
	MODE32 MODE16 Communication								
	1   x   32-bit								
	0 0 <b>8-bit</b>								
bit 9	SMP: SPI Data Input Sample Phase bit								
	Master mode (MSTEN = 1):								
	<ul> <li>Input data sampled at end of data output time</li> <li>Input data sampled at middle of data output time</li> </ul>								
	Slave mode (MSTEN = 0):								
	SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.								
	To write a '1' to this bit, the MSTEN value = 1 must first be written.								
bit 8	CKE: SPI Clock Edge Select bit <sup>(3)</sup>								
	1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit) 0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)								
bit 7	SSEN: Slave Select Enable (Slave mode) bit								
bit i	$1 = \overline{SSx}$ pin used for Slave mode								
	$0 = \overline{SSx}$ pin not used for Slave mode, pin controlled by port function.								
bit 6	CKP: Clock Polarity Select bit <sup>(4)</sup>								
	1 = 1 dle state for clock is a high level; active state is a low level 0 = 1 dle state for clock is a low level; active state is a high level								
Note 1:	When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in								
	the SYSCLK cycle immediately following the instruction that clears the module's ON bit.								
2:	This bit can only be written when the ON bit = 0.								
3:	I his bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).								
4:	When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value								
	of CKP.								

2

## REGISTER 19-1: UXMODE: UARTX MODE REGISTER (CONTINUED)

bit 5	<ul> <li>ABAUD: Auto-Baud Enable bit</li> <li>1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion</li> <li>0 = Baud rate measurement disabled or completed</li> </ul>
bit 4	RXINV: Receive Polarity Inversion bit 1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	BRGH: High Baud Rate Enable bit 1 = High-Speed mode – 4x baud clock enabled 0 = Standard Speed mode – 16x baud clock enabled
bit 2-1	PDSEL<1:0>: Parity and Data Selection bits 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	<b>STSEL:</b> Stop Selection bit 1 = 2 Stop bits 0 = 1 Stop bit

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

#### REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED) bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bit 11 = Reserved; do not use 10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters) 01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters) 00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character) bit 5 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect. 0 = Address Detect mode is disabled bit 4 **RIDLE:** Receiver Idle bit (read-only) 1 =Receiver is Idle 0 = Data is being received PERR: Parity Error Status bit (read-only) bit 3 1 = Parity error has been detected for the current character 0 = Parity error has not been detected bit 2 FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character 0 = Framing error has not been detected **OERR:** Receive Buffer Overrun Error Status bit. bit 1 This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state. 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)

- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

### REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 ARPT<7:0>: Alarm Repeat Counter Value bits<sup>(2)</sup> 11111111 = Alarm will trigger 256 times

> 00000000 = Alarm will trigger one time The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
  - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
  - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

# 26.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to enabled or disabled peripherals:

- Control register lock sequence
- · Configuration bit select lock

#### 26.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the Configuration bit, PMDLOCK (CFGCON<12>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes.

To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 6.** "**Oscillator**" (DS60001112) in the "*PIC32 Family Reference Manual*" for details.

### 26.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The Configuration bit, PMDL1WAY (DEVCFG3<28>), blocks the PMDLOCK bit from being cleared after it has been set once. If PMDLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

## 28.0 INSTRUCTION SET

The PIC32MX1XX/2XX family instruction set complies with the MIPS32<sup>®</sup> Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- · Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

**Note:** Refer to *"MIPS32<sup>®</sup> Architecture for Programmers Volume II: The MIPS32<sup>®</sup> Instruction Set"* at www.imgtec.com for more information. NOTES:

## 30.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX 28/36/44-pin Family AC characteristics and timing parameters.

### FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



#### TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

АС СНА	RACTERI	STICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions		
DO56	Сю	All I/O pins and OSC2		_	50	pF	EC mode		
DO58	Св	SCLx, SDAx		—	400	pF	In I <sup>2</sup> C mode		

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

#### FIGURE 30-2: EXTERNAL CLOCK TIMING



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY





## TABLE 30-31: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature } -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical <sup>(2)</sup>	Max.	Units	Conditions
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance (Note 4)	5	_	25	ns	_
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	Тscк + 20	_	_	ns	_
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	—	25	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.

AC CHARA	S <sup>(2)</sup>	$\begin{tabular}{ l l l l l l l l l l l l l l l l l l l$			
ADC Speed	TAD Min.	Sampling Time Min.	Rs Max.	Vdd	ADC Channels Configuration
1 Msps to 400 ksps <sup>(1)</sup>	65 ns	132 ns	500Ω	3.0V to 3.6V	ANX CHX ADC
Up to 400 ksps	200 ns	200 ns	5.0 κΩ	2.5V to 3.6V	ANX CHX ANX OF VREF-

### TABLE 30-35:10-BIT CONVERSION RATE PARAMETERS

**Note 1:** External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.

**3:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

## 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			INCHES		
Dimensior	n Limits	MIN	NOM	MAX		
Number of Pins	Ν					
Pitch		.100 BSC				
Top to Seating Plane	Α	-	-	.200		
Molded Package Thickness	A2	.120	.135	.150		
Base to Seating Plane	A1	.015	-	-		
Shoulder to Shoulder Width	E	.290	.310	.335		
Molded Package Width	E1	.240	.285	.295		
Overall Length	D	1.345	1.365	1.400		
Tip to Seating Plane	L	.110	.130	.150		
Lead Thickness	с	.008	.010	.015		
Upper Lead Width	b1	.040	.050	.070		
Lower Lead Width	b	.014	.018	.022		
Overall Row Spacing §		-	-	.430		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

## **Revision E (October 2012)**

All singular pin diagram occurrences of CVREF were changed to: CVREFOUT. In addition, minor text and formatting changes were incorporated throughout the document.

All major changes are referenced by their respective section in Table A-4.

TABLE A-4:	MAJOR SECTION UPDATES
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Section	Update Description				
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Updated the following feature sections: <ul> <li>"Operating Conditions"</li> <li>"Communication Interfaces"</li> </ul>				
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Removed Section 2.8 "Configuration of Analog and Digital Pins During ICSP Operations".				
3.0 "CPU"	Removed references to GPR shadow registers in <b>3.1 "Features"</b> and <b>3.2.1 "Execution Unit"</b> .				
4.0 "Memory Organization"	Updated the BRG bit range in the SPI1 and SPI2 Register Map (see Table 4-8). Added the PWP<6> bit to the Device Configuration Word Summary (see Table 4-17).				
5.0 "Flash Program Memory"	Added a note with Flash page size and row size information.				
7.0 "Interrupt Controller"	Updated the TPC<2:0> bit definitions (see Register 7-1). Updated the IPTMR<31:0> bit definition (see Register 7-3).				
8.0 "Oscillator Configuration"	Updated the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1). Updated the RODIV<14:0> bit definitions (see Register 8-3).				
10.0 "USB On-The-Go (OTG)"	Updated the Notes in the USB Interface Diagram (see Figure 10-1).				
18.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the baud rate range in the list of primary features.				
26.0 "Special Features"	Added the PWP<6> bit to the Device Configuration Word 0 (see Register 26-1).				
29.0 "Electrical Characteristics"	<ul> <li>Added Note 1 to Operating MIPS vs. Voltage (see Table 29-1).</li> <li>Added Note 2 to DC Temperature and Voltage Specifications (see Table 29-4).</li> <li>Updated the Conditions for parameter DC25 in DC Characteristics: Operating Current (IDD) (see Table 29-5).</li> <li>Added Note 2 to Electrical Characteristics: BOR (see Table 29-10).</li> <li>Added Note 4 to Comparator Specifications (see Table 29-12).</li> <li>Added Note 5 to ADC Module Specifications (see Table 29-32).</li> <li>Updated the 10-bit Conversion Rate Parameters and added Note 3 (see Table 29-33).</li> <li>Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 29-34).</li> <li>Added Note 3 to CTMU Current Source Specifications (see Table 29-39).</li> </ul>				
30.0 "50 MHz Electrical Characteristics"	New chapter with electrical characteristics for 50 MHz devices.				
31.0 "Packaging Information"	The 36-pin and 44-pin VTLA packages have been updated.				

## **Revision F (February 2014)**

This revision includes the addition of the following devices:

In addition, this revision includes the following major changes as described in Table A-5, as well as minor updates to text and formatting, which were incorporated throughout the document.

- PIC32MX170F256B PIC32MX270F256B
- PIC32MX170F256D
   PIC32MX270F256D

## TABLE A-5: MAJOR SECTION UPDATES

Section	Update Description				
32-bit Microcontrollers (up to 256	Added new devices to the family features (see Table 1 and Table 2).				
KB Flash and 64 KB SRAM) with	Updated pin diagrams to include new devices (see "Pin Diagrams").				
Audio and Graphics Interfaces, USB, and Advanced Analog					
1.0 "Device Overview"	Added Note 3 reference to the following pin names: VBUS, VUSB3V3, VBUSON,				
	D+, D-, and USBID.				
2.0 "Guidelines for Getting	Replaced Figure 2-1: Recommended Minimum Connection.				
Started with 32-bit MCUs"	Updated Figure 2-2: MCLR Pin Connections.				
	Added 2.9 "Sosc Design Recommendation".				
4.0 "Memory Organization"	Added memory tables for devices with 64 KB RAM (see Table 4-4 through Table 4-5).				
	Changed the Virtual Addresses for all registers and updated the PWP bits in the DEVCFG: Device Configuration Word Summary (see Table 4-17).				
	Updated the ODCA, ODCB, and ODCC port registers (see Table 4-19, Table 4-20, and Table 4-21).				
	The RTCTIME, RTCDATE, ALRMTIME, and ALRMDATE registers were updated (see Table 4-25).				
	Added Data Ram Size value for 64 KB RAM devices (see Register 4-5).				
	Added Program Flash Size value for 256 KB Flash devices (see Register 4-5).				
12.0 "Timer1"	The Timer1 block diagram was updated to include the 16-bit data bus (see Figure 12-1).				
13.0 "Timer2/3, Timer4/5"	The Timer2-Timer5 block diagram (16-bit) was updated to include the 16-bit data bus (see Figure 13-1).				
	The Timer2/3, Timer4/5 block diagram (32-bit) was updated to include the 32- bit data bus (see Figure 13-1).				
19.0 "Parallel Master Port (PMP)"	The CSF<1:0> bit value definitions for '00' and '01' were updated (see Register 19-1).				
	Bit 14 in the Parallel Port Address register (PMADDR) was updated (see Register 19-3).				
20.0 "Real-Time Clock and	The following registers were updated:				
Calendar (RTCC)"	RTCTIME (see Register 20-3)				
	RTCDATE (see Register 20-4)				
	ALRMTIME (see Register 20-5)				
	ALRMDATE (see Register 20-6)				
26.0 "Special Features"	Updated the PWP bits (see Register 26-1).				
29.0 "Electrical Characteristics"	Added parameters DO50 and DO50a to the Capacitive Loading Requirements on Output Pins (see Table 29-14).				
	Added Note 5 to the IDD DC Characteristics (see Table 29-5).				
	Added Note 4 to the IIDLE DC Characteristics (see Table 29-6).				
	Added Note 5 to the IPD DC Characteristics (see Table 29-7).				
	Updated the conditions for parameters USB321 (VOL) and USB322 (VOH) in the OTG Electrical Specifications (see Table 29-38).				
Product Identification System	Added 40 MHz speed information.				

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ISBN:978-1-5224-0471-2