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Microchip Technology - PIC32MX250F128CT-50I/TL Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128ct-50i-tl

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		Pin Nu	mber ⁽¹⁾				
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		_	_	27	0	_	Parallel Master Port address
PMA3				38	0	—	(Demultiplexed Master modes)
PMA4				37	0	—	
PMA5		_	_	4	0	_	
PMA6		_	_	5	0	_	
PMA7				13	0	—	
PMA8		_	_	32	0	_	
PMA9		_	_	35	0	_	
PMA10		_	_	12	0	_	
PMCS1	23	26	29	15	0	_	Parallel Master Port Chip Select 1 strobe
	20 ⁽²⁾	23 ⁽²⁾	26 ⁽²⁾	10 ⁽²⁾	1/0	TTI /CT	Parallel Master Port data (Demultiplexed
	1 ⁽³⁾	4 ⁽³⁾	35 ⁽³⁾	21 ⁽³⁾	1/0	111/31	Master mode) or address/data
	19 (2)	22 ⁽²⁾	25 ⁽²⁾	9 (2)	1/0	TTI /CT	(Multiplexed Master modes)
	2 ⁽³⁾	5 ⁽³⁾	36 ⁽³⁾	22 ⁽³⁾	1/0	111/31	
	18 ⁽²⁾	21 ⁽²⁾	24 ⁽²⁾	8 ⁽²⁾	1/0	TTI /ST	
	ვ(3)	6 ⁽³⁾	1 ⁽³⁾	23 ⁽³⁾	1/0	116/01	
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12 ⁽²⁾	15 ⁽²⁾	16 ⁽²⁾	42 ⁽²⁾	1/0	TTI /CT	1
	28 ⁽³⁾	3(3)	34 (3)	20 ⁽³⁾	1/0	111/31	
PMD7	11(2)	14 ⁽²⁾	15 (2)	41 ⁽²⁾	1/0	TTI /ST	
	27 ⁽³⁾	2 ⁽³⁾	33 (3)	19 ⁽³⁾	1/0	112/01	
PMRD	21	24	27	11	0	—	Parallel Master Port read strobe
	22 ⁽²⁾	25 ⁽²⁾	28 ⁽²⁾	14 ⁽²⁾	0		Parallel Master Port write strope
	4 ⁽³⁾	7 ⁽³⁾	2 ⁽³⁾	24 ⁽³⁾	Ŭ		T arallel master Fort while strobe
VBUS	12 ⁽³⁾	15 ⁽³⁾	16 (3)	42 ⁽³⁾	Ι	Analog	USB bus power monitor
VUSB3V3	20 ⁽³⁾	23 ⁽³⁾	26 ⁽³⁾	10 ⁽³⁾	Р	_	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22 ⁽³⁾	25 ⁽³⁾	28 ⁽³⁾	14 ⁽³⁾	0		USB Host and OTG bus power control output
D+	18 ⁽³⁾	21 ⁽³⁾	24 ⁽³⁾	8 ⁽³⁾	I/O	Analog	USB D+
D-	19 ⁽³⁾	22 ⁽³⁾	25 ⁽³⁾	9(3)	I/O	Analog	USB D-
Legend:	CMOS = C	MOS compa	atible input	or output		Analog =	Analog input P = Power
	ST = Schmi	tt Trigger in	put with CN	NOS levels		O = Outp	but I=Input
	L = L	nput buffer				PPS = P	eripheral Pin Select — = N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2.** "CPU" (DS60001113), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). Resources for the MIPS32[®] M4K[®] Processor Core are available at: www.imgtec.com.

The MIPS32[®] M4K[®] Processor Core is the heart of the PIC32MX1XX/2XX family processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the destinations.

3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2)
 - Multiply-accumulate and multiply-subtract instructions
 - Targeted multiply instruction
 - Zero/One detect instructions
 - WAIT instruction
 - Conditional move instructions (MOVN, MOVZ)
 - Vectored interrupts
 - Programmable exception vector base
 - Atomic interrupt enable/disable
 - Bit field manipulation instructions

- MIPS16e[®] code compression
 - 16-bit encoding of 32-bit instructions to improve code density
 - Special PC-relative instructions for efficient loading of addresses and constants
 - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
 - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- · Simple dual bus interface
 - Independent 32-bit address and data buses
 - Transactions can be aborted to improve interrupt latency
- · Autonomous multiply/divide unit
 - Maximum issue rate of one 32x16 multiply per clock
 - Maximum issue rate of one 32x32 multiply every other clock
 - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (*rs*) sign extension-dependent)
- Power control
 - Minimum frequency: 0 MHz
 - Low-Power mode (triggered by WAIT instruction)
 - Extensive use of local gated clocks
- EJTAG debug and instruction trace
 - Support for single stepping
 - Virtual instruction and data address/value
 - Breakpoints

FIGURE 3-1: MIPS32[®] M4K[®] PROCESSOR CORE BLOCK DIAGRAM



5.1 Flash Controller Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

ess		Ċ,								Bit	s								
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E400		31:16		—	—	—	—		—	—	—	—	—	_	—	—			0000
1400		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	_	_	_	_	_	_			NVMO	P<3:0>		0000
E410		31:16									/~21.0>								0000
1410		15:0									S1.02								0000
E420		31:16									D-21.05								0000
F420	NVINADUR' /	15:0								INVIVIADD	K~31.0~								0000
E420		31:16									A 221:05								0000
F430	NVINDATA	15:0								NVIVIDAL	AS1.02								0000
E440		31:16							N		21.05								0000
F440	NVIVISRCADDR	15:0	NVMSRCADDR<31:0>							0000									

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	_	_	_		IP03<2:0>		IS03	<1:0>
22.16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	—	—	—		IP02<2:0>	_	IS02	<1:0>
15.9	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	—	—	—		IP01<2:0>		IS01·	<1:0>
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0		_			IP00<2:0>		IS00-	<1:0>

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 31-29 Unimplemented: Read as '0'
- bit 28-26 IP03<2:0>: Interrupt Priority bits
- 111 = Interrupt priority is 7 010 = Interrupt priority is 2 001 = Interrupt priority is 1 000 = Interrupt is disabled bit 25-24 IS03<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0 bit 23-21 Unimplemented: Read as '0' bit 20-18 IP02<2:0>: Interrupt Priority bits 111 = Interrupt priority is 7 010 = Interrupt priority is 2 001 = Interrupt priority is 1 000 = Interrupt is disabled bit 17-16 IS02<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0 bit 15-13 Unimplemented: Read as '0' bit 12-10 IP01<2:0>: Interrupt Priority bits 111 = Interrupt priority is 7 010 = Interrupt priority is 2 001 = Interrupt priority is 1
 - 000 = Interrupt is disabled
- **Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

ess										Bi	ts								
Virtual Addre (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3170	DCH1SSIZ	31:16	_	—		_	_	_	—	—		_	—	_	_	_	_	—	0000
0170	DOITIOOIZ	15:0		i		i			i	CHSSIZ	2<15:0>		t					i	0000
3180	DCH1DSIZ	31:16		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0.00	50115012	15:0								CHDSIZ	Z<15:0>								0000
3190	DCH1SPTR	31:16				_		_		—	—	—	—	—	_	—	—		0000
		15:0								CHSPTI	≺<15:0>								0000
31A0	DCH1DPTR	31:16				_		_				_	_	_	_	_	_		0000
		10.0									~~15.0>								0000
31B0	DCH1CSIZ	15.0				_	_			CHCSIZ	 7<15:0>		_						0000
		31:16	_		_	_	_	_		_		_	_	_	_	_	_		0000
31C0	DCH1CPTR	15:0								CHCPTI	R<15:0>								0000
	DOLUDAT	31:16	_		_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
31D0	DCH1DAT	15:0	_	_	_	_	_	_	_	_				CHPDA	T<7:0>				0000
2150		31:16	_	_	_	—	_	_	—	_	_	_	_	_	_	_	_	_	0000
SIEU	DCH2CON	15:0	CHBUSY	—	—	—	—	-	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	-	CHEDET	CHPR	l<1:0>	0000
31E0	DCH2ECON	31:16	—	_	—	—	—	—	_	—			1	CHAIR	Q<7:0>				OOFF
011 0	DONZEOON	15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—		FF00
3200	DCH2INT	31:16				_	_		—		CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	_		—	—	—	—		—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3210	DCH2SSA	31:16								CHSSA	<31:0>								0000
		15:0																	0000
3220	DCH2DSA	15.0								CHDSA	<31:0>								0000
		31.16	_			_	_	_		_		_		_	_	_	_		0000
3230	DCH2SSIZ	15.0								CHSSIZ	/<15:0>								0000
		31:16	_	_		_	_	_		_	_	_	_	_	_	_	_	_	0000
3240	DCH2DSIZ	15:0								CHDSIZ	Z<15:0>								0000
0050	DOLIGODITO	31:16	_	_	_	—	_	_		_	_	_	_	_	_	_	_		0000
3250	DCH2SPTR	15:0								CHSPTI	R<15:0>								0000
3260		31:16	—	—	—	—	—	-	—	_	_		_	_	-	-		_	0000
5200		15:0	5:0 CHDPTR<15:0> 0000						0000										
3270	DCH2CSI7	31:16		—	—	—	_	—		—	—	—	—	—	—	—	—		0000
00	_ 5.12001L	15:0								CHCSIZ	Z<15:0>								0000

Legend:

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	_		—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
15:8	0N ⁽¹⁾	—	_	SUSPEND	DMABUSY	—	—	—
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	_	_	_	_	_

REGISTER 9-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ON: DMA On bit⁽¹⁾
 - 1 = DMA module is enabled
 - 0 = DMA module is disabled
- bit 14-13 **Unimplemented:** Read as '0'
- bit 12 SUSPEND: DMA Suspend bit
 - 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
 - 0 = DMA operates normally

bit 11 DMABUSY: DMA Module Busy bit

- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data
- bit 10-0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

INE OIOT										
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
51.24	—	—	—	—	—	—		—		
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	-	—		
15.9	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15.0	—	—	—	—	—	—		—		
7.0	R/WC-0, HS	U-0	R/WC-0, HS							
7:0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF		VBUSVDIF		

REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable b	pit
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 **IDIF:** ID State Change Indicator bit
 - 1 = A change in the ID state was detected
 - 0 = No change in the ID state was detected
- bit 6 T1MSECIF: 1 Millisecond Timer bit
 - 1 = 1 millisecond timer has expired
 - 0 = 1 millisecond timer has not expired

bit 5 LSTATEIF: Line State Stable Indicator bit

- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms
- bit 4 ACTVIF: Bus Activity Indicator bit
 - 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
 - 0 = Activity has not been detected
- bit 3 SESVDIF: Session Valid Change Indicator bit
 - 1 = VBUS voltage has dropped below the session end level
 - 0 = VBUS voltage has not dropped below the session end level
- bit 2 SESENDIF: B-Device VBUS Change Indicator bit
 - 1 = A change on the session end input was detected
 - 0 = No change on the session end input was detected
- bit 1 Unimplemented: Read as '0'
- bit 0 VBUSVDIF: A-Device VBUS Change Indicator bit
 - 1 = A change on the session valid input was detected
 - 0 = No change on the session valid input was detected

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0						
31:24	—	—	—	—	—	—	—	—
22:16	U-0	U-0						
23:10	—	—	—	—	—	—	—	_
45.0	U-0	U-0						
15:8	—	—	—	—	—	—	—	—
	R/W-0	R/W-0						
7:0	BTSEE	BMYEE		BTOEE			CRC5EE ⁽¹⁾	DIDEE
	DIGLE	DIVIALL	DIVIALL	DIOLL	DINOLL	ONCIDEL	EOFEE ⁽²⁾	

REGISTER 10-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7	BTSEE: Bit Stuff Error Interrupt Enable bit 1 = BTSEF interrupt is enabled 0 = BTSEF interrupt is disabled
bit 6	BMXEE: Bus Matrix Error Interrupt Enable bit
	1 = BMXEF interrupt is enabled0 = BMXEF interrupt is disabled
bit 5	DMAEE: DMA Error Interrupt Enable bit
	1 = DMAEF interrupt is enabled0 = DMAEF interrupt is disabled
bit 4	BTOEE: Bus Turnaround Time-out Error Interrupt Enable bit
	1 = BTOEF interrupt is enabled0 = BTOEF interrupt is disabled
bit 3	DFN8EE: Data Field Size Error Interrupt Enable bit
	1 = DFN8EF interrupt is enabled
	0 = DFN8EF interrupt is disabled

- bit 2 CRC16EE: CRC16 Failure Interrupt Enable bit
 - 1 = CRC16EF interrupt is enabled
 - 0 = CRC16EF interrupt is disabled
- bit 1 CRC5EE: CRC5 Host Error Interrupt Enable bit⁽¹⁾
 - 1 = CRC5EF interrupt is enabled
 - 0 = CRC5EF interrupt is disabled
 - EOFEE: EOF Error Interrupt Enable bit⁽²⁾
 - 1 = EOF interrupt is enabled
 - 0 = EOF interrupt is disabled
- bit 0 PIDEE: PID Check Failure Interrupt Enable bit
 - 1 = PIDEF interrupt is enabled
 - 0 = PIDEF interrupt is disabled
- Note 1: Device mode.
 - 2: Host mode.

Note: For an interrupt to propagate the USBIF register, the UERRIE (U1IE<1>) bit must be set.

TABLE 11-5: PORTC REGISTER MAP

ess	_											Bits							(0
Virtual Addr (BF88_#)	Register Name ^{(1,2})	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6200		31:16	_	—	—	—	—	—	—	—	—	—	—	—	—	—	_	—	0000
0200	ANSELC	15:0	_	—	_	—	—	—		—	—	—	—	—	ANSC3 ⁽⁴⁾	ANSC2 ⁽³⁾	ANSC1	ANSC0	000F
6210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	_	—	0000
0210	11100	15:0	_	—		—	—	—	TRISC9	TRISC8 ⁽³⁾	TRISC7 ⁽³⁾	TRISC6 ⁽³⁾	TRISC5 ⁽³⁾	TRISC4 ⁽³⁾	TRISC3	TRISC2 ⁽³⁾	TRISC1	TRISC0	03FF
6220	PORTO	31:16	_	—		—	—	—		—	—	—	—						0000
0220	FURIC	15:0	_	—		—	—	—	RC9	RC8 ⁽³⁾	RC7 ⁽³⁾	RC6 ⁽³⁾	RC5 ⁽³⁾	RC4 ⁽³⁾	RC3	RC2 ⁽³⁾	RC1	RC0	xxxx
6230	LATC	31:16	_	—		—	—	—		—	—	—	—	—	—	—		—	0000
0200		15:0	_	—		—	—	—	LATC9	LATC8 ⁽³⁾	LATC7 ⁽³⁾	LATC6 ⁽³⁾	LATC5 ⁽³⁾	LATC4 ⁽³⁾	LATC3	LATC2 ⁽³⁾	LATC1	LATC0	xxxx
6240	ODCC	31:16	_	—		—	—	—		—	—	—	—	—	—	—		—	0000
0240	ODCC	15:0	_	—		—	—	—	ODCC9	ODCC8 ⁽³⁾	ODCC7 ⁽³⁾	ODCC6 ⁽³⁾	ODCC5 ⁽³⁾	ODCC4 ⁽³⁾	ODCC3	ODCC2 ⁽³⁾	ODCC1	ODCC0	0000
6250	CNDUC	31:16	_	—		—	—	—		—	—	—	—	—	—	—		—	0000
0230	CINFUC	15:0	_	—		—	—	—	CNPUC9	CNPUC8 ⁽³⁾	CNPUC7 ⁽³⁾	CNPUC6 ⁽³⁾	CNPUC5 ⁽³⁾	CNPUC4 ⁽³⁾	CNPUC3	CNPUC2 ⁽³⁾	CNPUC1	CNPUC0	0000
6260		31:16	_	—	—	—	—	—		_	—	—	—	_	_		_	—	0000
0200	CINFDC	15:0	_	—	—	—	—	—	CNPDC9	CNPDC8 ⁽³⁾	CNPDC7 ⁽³⁾	CNPDC6 ⁽³⁾	CNPDC5 ⁽³⁾	CNPDC4 ⁽³⁾	CNPDC3	CNPDC2 ⁽³⁾	CNPDC1	CNPDC0	0000
6270	CNCONC	31:16	_	—	—	—	—	—		_	—	_	—	_	_		_	—	0000
0270	CINCOINC	15:0	ON	—	SIDL	—	—	—		_	—	_	—	_	_		_	—	0000
6000		31:16		_	_	_	—	—	—	—	—	—	—	—	_	—		_	0000
0200	CINEINC	15:0	-	—	—	—	—	—	CNIEC9	CNIEC8 ⁽³⁾	CNIEC7 ⁽³⁾	CNIEC6 ⁽³⁾	CNIEC5 ⁽³⁾	CNIEC4 ⁽³⁾	CNIEC3	CNIEC2 ⁽³⁾	CNIEC1	CNIEC0	0000
6200	CNOTATO	31:16		_	—	_	_	—	_	—	—	—	_	—	_	_	_		0000
6290	CINSTATC	15:0		_	—	_	_	—	CNSTATC9	CNSTATC8(3)	CNSTATC7(3)	CNSTATC6(3)	CNSTATC5(3)	CNSTATC4(3)	CNSTATC3	CNSTATC2(3)	CNSTATC1	CNSTATCO	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: PORTC is not available on 28-pin devices.

3: This bit is only available on 44-pin devices.

4: This bit is only available on USB-enabled devices with 36 or 44 pins.

13.0 TIMER2/3, TIMER4/5

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a freerunning interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- · Synchronous external 16-bit timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

- Synchronous internal 32-bit timer
- · Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

Note:	In this chapter, references to registers,
	TxCON, TMRx and PRx, use 'x' to
	represent Timer2 through Timer5 in 16-bit
	modes. In 32-bit modes, 'x' represents
	Timer2 or Timer4 and 'y' represents
	Timer3 or Timer5.

13.1 Additional Supported Features

- · Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 in 16-bit mode, Timer2/3 in 32-bit mode)
- Fast bit manipulation using CLR, SET and INV registers

Figure 13-1 and Figure 13-2 illustrate block diagrams of Timer2/3 and Timer4/5.

FIGURE 13-1: TIMER2-TIMER5 BLOCK DIAGRAM (16-BIT)



16.1 Output Compare Control Registers

TABLE 16-1: OUTPUT COMPARE 1-OUTPUT COMPARE 5 REGISTER MAP

ess										В	its								6
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3000	00100	31:16	—	—	—	—	—	—	—	_	—	—	—	—	—		—	_	0000
0000	001001	15:0	ON	—	SIDL	—	—	—		—	—	—	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3010	OC1R	31:16 15:0								OC1R	<31:0>								xxxx
3020	OC1RS	31:16 15:0								OC1RS	\$<31:0>								XXXX
0000	00000	31:16	—	_	_	_	_	_		_	—	—	_	—	_	_	—	—	0000
3200	UC2CON	15:0	ON	_	SIDL	_	_	_	_	_	_	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
2210	0028	31:16								0020	~21.0>								XXXX
3210	UCZR	15:0								UCZR	<31.0>								xxxx
3220	00288	31:16								00200	2-31-05								XXXX
3220	00283	15:0								UCZRO	5<31.02								XXXX
3400	003000	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_		—		0000
3400	003001	15:0	ON	_	SIDL	_	_	_	_	_	-	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3410	OC3R	31:16 15:0								OC3R	<31:0>								XXXX XXXX
2420	00200	31:16								00000	221.05								XXXX
3420	00383	15:0								UCSRC	5-51.0-								XXXX
3600		31:16	—	_	_	_	_	_	_	_	—	—	_	—	—	_	—	_	0000
3000	004001	15:0	ON	_	SIDL	_	_	_	_	_	-	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3610	OC4R	31:16								OC4R	<31.0>								XXXX
3010	0041	15:0								0041	-01.02								xxxx
3620	OC4RS	31:16									221.05								xxxx
3020	00410	15:0								00400	0-01.0-								xxxx
3800		31:16	-	_	—	_	_	_	_	_	-	_	—	—	—		—		0000
3000	000001	15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3810	OC5R	31:16								00.5R	<31.0>								xxxx
3010										xxxx									
3820	OC5RS	31:16																	xxxx
3020	00010	15 [.] 0								00000	-01.02								xxxx

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Legend: x = unknown value on Reset; -- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0			
31:24	—	—	—		RXBUFELM<4:0>						
00.10	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0			
23:10	—	—	—	TXBUFELM<4:0>							
45.0	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0			
15:8	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR			
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0			
	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF			

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER

Legend:	C = Clearable bit	HS = Set in hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 31-29 Unimplemented: Read as '0'
- bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 23-21 Unimplemented: Read as '0'
- bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 15-13 Unimplemented: Read as '0'
- bit 12 **FRMERR:** SPI Frame Error status bit
 - 1 = Frame error detected
 - 0 = No Frame error detected
 - This bit is only valid when FRMEN = 1.
- bit 11 SPIBUSY: SPI Activity Status bit
 - 1 = SPI peripheral is currently busy with some transactions
 - 0 = SPI peripheral is currently idle
- bit 10-9 Unimplemented: Read as '0'
- bit 8 SPITUR: Transmit Under Run bit
 - 1 = Transmit buffer has encountered an underrun condition
 - 0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.

- bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
 - 1 = When SPI module shift register is empty
 - 0 = When SPI module shift register is not empty
- bit 6 SPIROV: Receive Overflow Flag bit
 - 1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
 - 0 = No overflow has occurred

This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.

- bit 5 SPIRBE: RX FIFO Empty bit (valid only when ENHBUF = 1) 1 = RX FIFO is empty (CRPTR = SWPTR)
 - 0 = RX FIFO is not empty (CRPTR \neq SWPTR)
- bit 4 Unimplemented: Read as '0'

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

- bit 4 Unimplemented: Read as '0' CS1P: Chip Select 0 Polarity bit⁽²⁾ bit 3 1 = Active-high (PMCS1) $0 = \text{Active-low}(\overline{PMCS1})$ bit 2 Unimplemented: Read as '0' bit 1 WRSP: Write Strobe Polarity bit For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10): 1 = Write strobe active-high (PMWR) 0 = Write strobe active-low (PMWR) For Master mode 1 (MODE<1:0> = 11): 1 = Enable strobe active-high (PMENB) 0 = Enable strobe active-low (PMENB) bit 0 RDSP: Read Strobe Polarity bit For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10): 1 = Read Strobe active-high (PMRD) $0 = \text{Read Strobe active-low}(\overline{PMRD})$ For Master mode 1 (MODE<1:0> = 11): 1 = Read/write strobe active-high (PMRD/PMWR)
 - 0 = Read/write strobe active-low (PMRD/PMWR)
 - **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - 2: These bits have no effect when their corresponding pins are used as address lines.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	-	_	_	_	—	_	—
45.0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
15:8	BUSY	IRQM	<1:0>	INCM	<1:0>	—	MODE	=<1:0>
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB	<1:0>(1)		WAITM	<3:0>(1)		WAITE<1:0>(1)	

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **BUSY:** Busy bit (Master mode only)
 - 1 = Port is busy
 - 0 = Port is not busy

bit 14-13 IRQM<1:0>: Interrupt Request Mode bits

- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

bit 12-11 INCM<1:0>: Increment Mode bits

- 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾
- 01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾
- 00 = No increment or decrement of address
- bit 10 Unimplemented: Read as '0'
- bit 9-8 MODE<1:0>: Parallel Port Mode Select bits
 - 11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)
 - 10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)
 - 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
 - 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)
- bit 7-6 WAITB<1:0>: Data Setup to Read/Write Strobe Wait States bits⁽¹⁾
 - 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
 - 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
 - 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
 - 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

bit 5-2 WAITM<3:0>: Data Read/Write Strobe Wait States bits⁽¹⁾

- 1111 = Wait of 16 Трв •
- . 0001 = Wait of 2 Трв 0000 = Wait of 1 Трв (default)
- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	_	—	-
00.40	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:10	—	—	—	— MONTH10 MONTH01<3:0>				
45.0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15:8	—	—	DAY1	0<1:0>	DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	_	_	_	_	_	V	VDAY01<2:0:	>

REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER

Legend:

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 Unimplemented: Read as '0'

bit 20 MONTH10: Binary Coded Decimal value of months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9 bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 DAY10<1:0>: Binary Coded Decimal value of days bits, 10s place digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 Unimplemented: Read as '0'

bit 2-0 WDAY01<2:0>: Binary Coded Decimal value of weekdays bits; contains a value from 0 to 6

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	—	—	—	—	—	—	—	—		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0		

REGISTER 22-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Legend:

Logena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CSSL<15:0>: ADC Input Pin Scan Selection bits^(1,2)

1 = Select ANx for input scan

0 = Skip ANx for input scan

- **Note 1:** CSSL = ANx, where 'x' = 0-12; CSSL13 selects CTMU input for scan; CSSL14 selects IVREF for scan; CSSL15 selects Vss for scan.
 - 2: On devices with less than 13 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

- bit 10 EDGSEQEN: Edge Sequence Enable bit 1 = Edge1 must occur before Edge2 can occur 0 = No edge sequence is needed IDISSEN: Analog Current Source Control bit⁽²⁾ bit 9 1 = Analog current source output is grounded 0 = Analog current source output is not grounded bit 8 **CTTRIG:** Trigger Control bit 1 = Trigger output is enabled 0 = Trigger output is disabled bit 7-2 ITRIM<5:0>: Current Source Trim bits 011111 = Maximum positive change from nominal current 011110 000001 = Minimum positive change from nominal current 000000 = Nominal current output specified by IRNG<1:0> 111111 = Minimum negative change from nominal current 100010 100001 = Maximum negative change from nominal current bit 1-0 IRNG<1:0>: Current Range Select bits⁽³⁾ 11 = 100 times base current 10 = 10 times base current
 - 01 = Base current level
 - 00 = 1000 times base current⁽⁴⁾
- Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - Refer to the CTMU Current Source Specifications (Table 30-41) in Section 30.0 "Electrical 3: Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	R/P	r-1	r-1	r-1	R/P
	—	—	—	CP	—	—	—	BWP
23:16	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	—	—	—	—	—	PWP<8:6> ⁽³⁾		
15:8	R/P	R/P	R/P	R/P	R/P	R/P	r-1	r-1
	PWP<5:0>						—	—
7:0	r-1	r-1	r-1	R/P	R/P	R/P	R/P	R/P
		—	—	ICESEL	<1:0> (2)	JTAGEN ⁽¹⁾	DEBUG<1:0>	

REGISTER 27-1: DEVCFG0: DEVICE CONFIGURATION WORD 0

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 Reserved: Write '0'

bit 30-29 Reserved: Write '1'

- bit 28 **CP:** Code-Protect bit
 - Prevents boot and program Flash memory from being read or modified by an external programming device. 1 = Protection is disabled

0 = Protection is enabled

bit 27-25 Reserved: Write '1'

bit 24 **BWP:** Boot Flash Write-Protect bit

Prevents boot Flash memory from being modified during code execution.

1 = Boot Flash is writable

0 = Boot Flash is not writable

- bit 23-19 Reserved: Write '1'
- **Note 1:** This bit sets the value for the JTAGEN bit in the CFGCON register.
 - 2: The PGEC4/PGED4 pin pair is not available on all devices. Refer to the "**Pin Diagrams**" section for availability.
 - 3: The PWP<8:7> bits are only available on devices with 256 KB Flash.

TABLE 31-8:SPIX MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Conditions
MSP70	TscL	SCKx Input Low Time (Note 1,2)	Tsck/2		I	ns	—
MSP71	TscH	SCKx Input High Time (Note 1,2)	Tsck/2			ns	—
MSP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance (Note 2)	5		25	ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns.

TABLE 31-9: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time (Note 1,2)	Tsck/2	_	—	ns	_
SP71	TscH	SCKx Input High Time (Note 1,2)	Tsck/2		—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns.

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS				
Dimension	n Limits	MIN	NOM	MAX		
Number of Pins	Ν	28				
Pitch	е	0.65 BSC				
Overall Height	Α	0.80	0.90	1.00		
Standoff	A1	0.00	0.02	0.05		
Contact Thickness	A3	0.20 REF				
Overall Width	E	6.00 BSC				
Exposed Pad Width	E2	3.65	3.70	4.20		
Overall Length	D	6.00 BSC				
Exposed Pad Length	D2	3.65	3.70	4.20		
Contact Width	b	0.23	0.30	0.35		
Contact Length		0.50	0.55	0.70		
Contact-to-Exposed Pad	K	0.20	_	_		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B