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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128dt-50i-pt

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FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX110/210 DEVICES (4 KB RAM, 16 KB FLASH)

NOTES:

FIGURE 8-1: OSCILLATOR DIAGRAM



 Refer to Section 6. "Oscillator Configuration" (DS60001112) in the "PIC32 Family Reference Manual" for help in determinin best oscillator components.

3. The PBCLK out is only available on the OSC2 pin in certain clock modes.

4. The USB PLL is only available on PIC32MX2XX devices.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

- bit 18-16 **PLLMULT<2:0>:** Phase-Locked Loop (PLL) Multiplier bits
 - 111 = Clock is multiplied by 24
 - 110 = Clock is multiplied by 21
 - 101 = Clock is multiplied by 20
 - 100 = Clock is multiplied by 19
 - 011 = Clock is multiplied by 18
 - 010 = Clock is multiplied by 17
 - 001 = Clock is multiplied by 16
 - 000 = Clock is multiplied by 15
- bit 15 Unimplemented: Read as '0'
- bit 14-12 COSC<2:0>: Current Oscillator Selection bits
 - 111 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (OSCCON<26:24>)
 - 110 = Internal Fast RC (FRC) Oscillator divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (Posc) (XT, HS or EC)
 - 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast RC (FRC) Oscillator
- bit 11 Unimplemented: Read as '0'
- bit 10-8 NOSC<2:0>: New Oscillator Selection bits
 - 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC Oscillator (FRC) divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (XT, HS or EC)
 - 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

bit 7 CLKLOCK: Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):

- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):

Clock and PLL selections are never locked and may be modified.

- bit 6 ULOCK: USB PLL Lock Status bit⁽¹⁾
 - 1 = The USB PLL module is in lock or USB PLL module start-up timer is satisfied
 - 0 =The USB PLL module is out of lock or USB PLL module start-up timer is in progress or the USB PLL is disabled
- bit 5 SLOCK: PLL Lock Status bit
 - 1 = The PLL module is in lock or PLL module start-up timer is satisfied
 - 0 = The PLL module is out of lock, the PLL start-up timer is running, or the PLL is disabled
- bit 4 SLPEN: Sleep Mode Enable bit
 - 1 = The device will enter Sleep mode when a WAIT instruction is executed
 - 0 = The device will enter Idle mode when a WAIT instruction is executed
- **Note 1:** This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	
31:24	—	—	BYTC)<1:0>	WBO ⁽¹⁾	—	—	BITO	
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:10	—	—	—	—	—	—	—	_	
45.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	—	—	—			PLEN<4:0>			
7.0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
7:0	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	_	(CRCCH<2:0>		

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

- bit 29-28 BYTO<1:0>: CRC Byte Order Selection bits
 - 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
 - 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
 - 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
 - 00 = No swapping (i.e., source byte order)
- bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾
 - 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
 - 0 = Source data is written to the destination unaltered
- bit 26-25 Unimplemented: Read as '0'
- bit 24 BITO: CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode):

- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 Unimplemented: Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits

<u>When CRCTYP (DCRCCON<15>) = 1</u> (CRC module is in IP Header mode): These bits are unused.

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode): Denotes the length of the polynomial -1.

- bit 7 CRCEN: CRC Enable bit
 - 1 = CRC module is enabled and channel transfers are routed through the CRC module
 - 0 = CRC module is disabled and channel transfers proceed normally
- Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0							
31:24	—	—	—	—	—	—	—	—	
22:16	U-0	U-0							
23:10	—	—	—	—	—	—	—	_	
45.0	U-0	U-0							
15:8	—	—	—	—	—	—	—	-	
	R/W-0	R/W-0							
7:0	BTSEE			PTOEE			CRC5EE ⁽¹⁾	DIDEE	
	DIGLE	DIVIALL	DIVIALL	DIOLL	DINOLL	ONCIDEL	EOFEE ⁽²⁾	FIDEE	

REGISTER 10-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7	BTSEE: Bit Stuff Error Interrupt Enable bit 1 = BTSEF interrupt is enabled 0 = BTSEF interrupt is disabled
bit 6	BMXEE: Bus Matrix Error Interrupt Enable bit
	1 = BMXEF interrupt is enabled0 = BMXEF interrupt is disabled
bit 5	DMAEE: DMA Error Interrupt Enable bit
	1 = DMAEF interrupt is enabled0 = DMAEF interrupt is disabled
bit 4	BTOEE: Bus Turnaround Time-out Error Interrupt Enable bit
	1 = BTOEF interrupt is enabled0 = BTOEF interrupt is disabled
bit 3	DFN8EE: Data Field Size Error Interrupt Enable bit
	1 = DFN8EF interrupt is enabled
	0 = DFN8EF interrupt is disabled

- bit 2 CRC16EE: CRC16 Failure Interrupt Enable bit
 - 1 = CRC16EF interrupt is enabled
 - 0 = CRC16EF interrupt is disabled
- bit 1 CRC5EE: CRC5 Host Error Interrupt Enable bit⁽¹⁾
 - 1 = CRC5EF interrupt is enabled
 - 0 = CRC5EF interrupt is disabled
 - EOFEE: EOF Error Interrupt Enable bit⁽²⁾
 - 1 = EOF interrupt is enabled
 - 0 = EOF interrupt is disabled
- bit 0 PIDEE: PID Check Failure Interrupt Enable bit
 - 1 = PIDEF interrupt is enabled
 - 0 = PIDEF interrupt is disabled
- Note 1: Device mode.
 - 2: Host mode.

Note: For an interrupt to propagate the USBIF register, the UERRIE (U1IE<1>) bit must be set.

REGISTER 10-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—		—	—	—	—	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	-	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	-	—	—	—	—	—
7.0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
7:0		ENDP.	T<3:0>		DIR	PPBI	_	_

Legend:

· J· ·			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits (Represents the number of the Buffer Descriptor Table, updated by the last USB transfer.)
 - 1111 = Endpoint 15 1110 = Endpoint 14 . . 0001 = Endpoint 1 0000 = Endpoint 0
- bit 3 **DIR:** Last Buffer Descriptor Direction Indicator bit
 - 1 = Last transaction was a transmit (TX) transfer
 - 0 = Last transaction was a receive (RX) transfer
- bit 2 **PPBI:** Ping-Pong Buffer Descriptor Pointer Indicator bit
 - 1 = The last transaction was to the ODD Buffer Descriptor bank
 - 0 = The last transaction was to the EVEN Buffer Descriptor bank
- bit 1-0 Unimplemented: Read as '0'

Note: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF (U1IR<3>) bit is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

TABLE 11-1: INPUT PIN SELECTION

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[<i>pin name</i>]R Value to RPn Pin Selection
INT4	INT4R	INT4R<3:0>	0000 = RPA0 0001 = RPB3
T2CK	T2CKR	T2CKR<3:0>	0010 = RPB4 0011 = RPB15 0100 = RPB7
IC4	IC4R	IC4R<3:0>	$0101 = RPC7^{(2)}$ $0110 = RPC0^{(1)}$ $0111 = RPC5^{(2)}$
SS1	SS1R	SS1R<3:0>	1000 = Reserved
REFCLKI	REFCLKIR	REFCLKIR<3:0>	: 1111 = Reserved
INT3	INT3R	INT3R<3:0>	0000 = RPA1 0001 = RPB5
ТЗСК	T3CKR	T3CKR<3:0>	0010 = RPB1 0011 = RPB11
IC3	IC3R	IC3R<3:0>	0100 = RPB8 $0101 = RPA8^{(2)}$
U1CTS	U1CTSR	U1CTSR<3:0>	$0110 = RPC8^{(2)}$ $0111 = RPA9^{(2)}$
U2RX	U2RXR	U2RXR<3:0>	•
SDI1	SDI1R	SDI1R<3:0>	• 1111 = Reserved
INT2	INT2R	INT2R<3:0>	0000 = RPA2
T4CK	T4CKR	T4CKR<3:0>	
IC1	IC1R	IC1R<3:0>	0011 = RPB13
IC5	IC5R	IC5R<3:0>	$0101 = \text{RPC6}^{(2)}$
U1RX	U1RXR	U1RXR<3:0>	$-0110 = \text{RPC1}^{(1)}$ 0111 = RPC3(1)
U2CTS	U2CTSR	U2CTSR<3:0>	1000 = Reserved
SDI2	SDI2R	SDI2R<3:0>	
OCFB	OCFBR	OCFBR<3:0>	• 1111 = Reserved
INT1	INT1R	INT1R<3:0>	0000 = RPA3 0001 = RPB14
T5CK	T5CKR	T5CKR<3:0>	0010 = RPB0 0011 = RPB10 0100 = RPB9
IC2	IC2R	IC2R<3:0>	$0101 = RPC9^{(1)}$ $0110 = RPC2^{(2)}$ $0111 = PPC4^{(2)}$
SS2	SS2R	SS2R<3:0>	1000 = Reserved
OCFA	OCFAR	OCFAR<3:0>	1111 = Reserved

Note 1: This pin is not available on 28-pin devices.

2: This pin is only available on 44-pin devices.

NOTES:

17.1 SPI Control Registers

TABLE 17-1: SPI1 AND SPI2 REGISTER MAP

ess		6								Bi	ts								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FI	RMCNT<2:	0>	MCLKSEL	—	_	—	—	—	SPIFE	ENHBUF	0000
3000	SFILCON	15:0	ON	-	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISE	EL<1:0>	SRXISI	EL<1:0>	0000
E010	QDI1QTAT	31:16	_	_	_		RXE	BUFELM<4:	:0>		_	_	_		TX	BUFELM<4	:0>		0000
0100	SFIISTAI	15:0	—	—	—	FRMERR	SPIBUSY	-	_	SPITUR	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	0008
5020	SDI1BUE	31:16									31.05								0000
5620		15:0								DAIA	51.04								0000
5830	SPI1BRG	31:16	—		—	—	—	—	—	—	—	—	—	—	-	—	—	—	0000
3030		15:0	—	—	—						E	3RG<12:0>							0000
		31:16	_	—	—	—	—	_	—	—	—	—	—	—	—	—	-	—	0000
5840	SPI1CON2	15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMO	DC<1:0>	0000
	SDISCON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FI	RMCNT<2:	0>	MCLKSEL	_	_	_	_	_	SPIFE	ENHBUF	0000
5AUU	SFIZCON	15:0	ON	_	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISE	EL<1:0>	SRXISI	EL<1:0>	0000
	CDIPCTAT	31:16		—	—		RXE	BUFELM<4:	:0>		—	_	_		TX	BUFELM<4	:0>		0000
5A10	3F1231AI	15:0		—	—	FRMERR	SPIBUSY	_	—	SPITUR	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	8000
E A 20		31:16									0000								
5AZU	3F12D01	15:0								DAIA	51.0~								0000
EA 20	SDISEDC	31:16	_	—	—	_	_	_	—	—	_	—	—	—	—	—	_	—	0000
5A30		15:0	—		—			-			E	3RG<12:0>		-		-			0000
		31:16	—	-	—	—	-	—	—	-	-	-	—	—	-	—	—	—	0000
5A40	SPI2CON2	15:0	SPI SGNEXT	-	_	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	_	-	_	AUD MONO	_	AUDMO)D<1:0>	0000

Legend: x = unknown value on Reset; -- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	IREN	RTSMD	—	UEN	<1:0>
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL	<1:0>	STSEL

REGISTER 19-1: UXMODE: UARTX MODE REGISTER

Legend:

Logonal			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ON: UARTx Enable bit⁽¹⁾
 - 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by the UEN<1:0> and UTXEN control bits.
 - 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal.
- bit 14 Unimplemented: Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode
- bit 12 IREN: IrDA Encoder and Decoder Enable bit
 - 1 = IrDA is enabled
 - 0 = IrDA is disabled
- bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit
 - 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
 - $0 = \overline{\text{UxRTS}}$ pin is in Flow Control mode
- bit 10 Unimplemented: Read as '0'
- bit 9-8 UEN<1:0>: UARTx Enable bits
 - 11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
 - 10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used
 - 01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
 - 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register
- bit 7 WAKE: Enable Wake-up on Start bit Detect During Sleep Mode bit
 - 1 = Wake-up enabled
 - 0 = Wake-up disabled
- bit 6 LPBACK: UARTx Loopback Mode Select bit
 - 1 = Loopback mode is enabled
 - 0 = Loopback mode is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	_	—	-
00.40	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:10	—	—	—	MONTH10	MONTH01<3:0>			
45.0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15:8	—	—	DAY1	0<1:0>		DAY01	<3:0>	
7.0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
7:0	_	_	_	_	_	V	VDAY01<2:0:	>

REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER

Legend:

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 Unimplemented: Read as '0'

bit 20 MONTH10: Binary Coded Decimal value of months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9 bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 DAY10<1:0>: Binary Coded Decimal value of days bits, 10s place digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 Unimplemented: Read as '0'

bit 2-0 WDAY01<2:0>: Binary Coded Decimal value of weekdays bits; contains a value from 0 to 6

27.3 On-Chip Voltage Regulator

All PIC32MX1XX/2XX 28/36/44-pin Family devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX1XX/2XX 28/36/44-pin Family family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 30.1 "DC Characteristics"**.

Note:	It is important that the low-ESR capacitor
	is placed as close as possible to the VCAP
	pin.

27.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

27.3.2 ON-CHIP REGULATOR AND BOR

PIC32MX1XX/2XX 28/36/44-pin Family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 30.1 "DC Characteristics"**.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



27.4 **Programming and Diagnostics**

PIC32MX1XX/2XX 28/36/44-pin Family devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming[™] (ICSP[™]) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

Figure 27-2 illustrates a block diagram of the programming, debugging, and trace ports.





			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)					
			$\begin{array}{ll} \mbox{Operating temperature} & -40^{\circ} \mbox{C} \leq \mbox{Ta} \leq +85^{\circ} \mbox{C for Industrial} \\ & -40^{\circ} \mbox{C} \leq \mbox{Ta} \leq +105^{\circ} \mbox{C for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions	
	VIL	Input Low Voltage						
DI10		I/O Pins with PMP	Vss	—	0.15 Vdd	V		
		I/O Pins	Vss	—	0.2 Vdd	V		
DI18		SDAx, SCLx	Vss	_	0.3 Vdd	V	SMBus disabled (Note 4)	
DI19		SDAx, SCLx	Vss	_	0.8	V	SMBus enabled (Note 4)	
	VIH	Input High Voltage						
DI20		I/O Pins not 5V-tolerant ⁽⁵⁾	0.65 VDD	_	Vdd	V	(Note 4,6)	
		I/O Pins 5V-tolerant with PMP ⁽⁵⁾	0.25 VDD + 0.8V	_	5.5	V	(Note 4,6)	
		I/O Pins 5V-tolerant ⁽⁵⁾	0.65 VDD	—	5.5	V		
DI28		SDAx, SCLx	0.65 VDD	_	5.5	V	SMBus disabled (Note 4,6)	
DI29		SDAx, SCLx	2.1	_	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 (Note 4,6)	
DI30	ICNPU	Change Notification Pull-up Current	—	—	-50	μA	VDD = 3.3V, VPIN = VSS (Note 3,6)	
DI31	ICNPD	Change Notification Pull-down Current ⁽⁴⁾	—	—	-50	μA	VDD = 3.3V, VPIN = VDD	
	lı∟	Input Leakage Current (Note 3)						
DI50		I/O Ports	_	—	<u>+</u> 1	μA	Vss \leq VPIN \leq VDD, Pin at high-impedance	
DI51		Analog Input Pins	_	_	<u>+</u> 1	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance	
DI55		MCLR(2)	_	—	<u>+</u> 1	μA	$VSS \leq VPIN \leq VDD$	
DI56		OSC1	_	_	<u>+</u> 1	μA	$\label{eq:VSS} \begin{split} &V{\sf SS} \leq V{\sf PIN} \leq V{\sf DD}, \\ &X{\sf T} \text{ and }H{\sf S} \text{ modes} \end{split}$	

TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: See the "Pin Diagrams" section for the 5V-tolerant pins.
- 6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the userselectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.



ABLE	ABLE 30-22: RESETS TIMING										
AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industria $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp							
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions				
SY00	Τρυ	Power-up Period Internal Voltage Regulator Enabled		400	600	μS	_				
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.		1 μs + 8 SYSCLK cycles	_		_				
SY20	TMCLR	MCLR Pulse Width (low)	2	_	_	μS	_				
SY30	TBOR	BOR Pulse Width (low)	_	1	_	μS	_				

These parameters are characterized, but not tested in manufacturing. Note 1:

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

TABLE 30-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standar (unless Operatir	d Operating Condition otherwise stated) ng temperature -40°C -40°C	I IS: 2.3V C ≤ TA ≤ C ≤ TA ≤	/ to 3.6 (+85°C (+105°	V 5 for Industrial C for V-temp	
Param. No.	Symbol	Cha	Characteristics ⁽¹⁾		Min.	Max.	Units	Condi	tions
TB10	ТтхН	TxCK High Time	Synchron prescaler	ous, with	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8,
TB11	ΤτχL	TxCK Low Time	Synchron prescaler	ous, with	[(12.5 ns or 1 ТРВ)/N] + 25 ns	_	ns	Must also meet parameter TB15	16, 32, 64, 256)
TB15	T⊤xP	TxCK Input	Synchron prescaler	ous, with	[(Greater of [(25 ns or 2 Трв)/N] + 30 ns	_	ns	VDD > 2.7V	
		Period			[(Greater of [(25 ns or 2 Трв)/N] + 50 ns	_	ns	VDD < 2.7V	
TB20	TCKEXTMRL	Delay from Clock Edge	External T e to Timer I	xCK ncrement	—	1	Трв	_	-

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 30-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



TABLE 30-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard O (unless oth Operating te	$\begin{array}{ll} \mbox{perating Conditions: 2.3V} \\ \mbox{erwise stated}) \\ \mbox{ermperature} & -40^{\circ}C \leq TA \leq + \\ -40^{\circ}C \leq TA \leq + \end{array}$	to 3.6V 85°C foi 105°C fo	^r Industri or V-tem	al p	
Param. No.	Symbol	Charac	cteristics ⁽¹⁾	Min.	Max.	Units	Con	ditions
IC10	TccL	ICx Input	t Low Time	[(12.5 ns or 1 ТРВ)/N] + 25 ns	_	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	ТссН	ICx Input	t High Time	[(12.5 ns or 1 ТРВ)/N] + 25 ns	_	ns	Must also meet parameter IC15.	
IC15	TCCP	ICx Input	t Period	[(25 ns or 2 Трв)/N] + 50 ns	_	ns	_	

Note '	1:	These	parameters a	are charac	terized, bu	it not f	tested in	manufacturing	
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TABLE 30-31: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance (Note 4)	5	_	25	ns	_
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	Тѕск + 20	_	_	ns	_
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	—	25	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns.

4: Assumes 50 pF load on all SPIx pins.

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units				
Dimension	n Limits	MIN	NOM	MAX	
Number of Pins	Ν		28		
Pitch	е		0.65 BSC		
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3		0.20 REF		
Overall Width	E		6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.20	
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.20	
Contact Width	b	0.23	0.30	0.35	
Contact Length	L	0.50	0.55	0.70	
Contact-to-Exposed Pad	K	0.20	_	_	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

TABLE A-1:	MAJOR SECTION UPDATES	(CONTINUED)	
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Section	Update Description
29.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings (removed Voltage on VCORE with respect to Vss).
	Added the SPDIP specification to the Thermal Packaging Characteristics (see Table 29-2).
	Updated the Typical values for parameters DC20-DC24 in the Operating Current (IDD) specification (see Table 29-5).
	Updated the Typical values for parameters DC30a-DC34a in the Idle Current (IIDLE) specification (see Table 29-6).
	Updated the Typical values for parameters DC40i and DC40n and removed parameter DC40m in the Power-down Current (IPD) specification (see Table 29-7).
	Removed parameter D320 (VCORE) from the Internal Voltage Regulator Specifications and updated the Comments (see Table 29-13).
	Updated the Minimum, Typical, and Maximum values for parameter F20b in the Internal FRC Accuracy specification (see Table 29-17).
	Removed parameter SY01 (TPWRT) and removed all Conditions from Resets Timing (see Table 29-20).
	Updated all parameters in the CTMU Specifications (see Table 29-39).
31.0 "Packaging Information"	Added the 28-lead SPDIP package diagram information (see 31.1 " Package Marking Information " and 31.2 " Package Details ").
"Product Identification System"	Added the SPDIP (SP) package definition.

Revision C (November 2011)

All major changes are referenced by their respective section in Table A-2.

TABLE A-2:	MAJOR SECTION UPDATES
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Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Revised the source/sink on I/O pins (see "Input/Output" on page 1). Added the SPDIP package to the PIC32MX220F032B device in the PIC32MX2XX USB Family Features (see Table 2).
4.0 "Memory Organization"	Removed ANSB6 from the ANSELB register and added the ODCB6, ODCB10, and ODCB11 bits in the PORTB Register Map (see Table 4-20).
29.0 "Electrical Characteristics"	Updated the minimum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 29-16).

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