



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128dt-50i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

		Pin Nu	mber ⁽¹⁾				
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		_	_	27	0	_	Parallel Master Port address
PMA3				38	0	—	(Demultiplexed Master modes)
PMA4				37	0	—	
PMA5		_	_	4	0	_	
PMA6		_	_	5	0	_	
PMA7				13	0	—	
PMA8		_	_	32	0	_	
PMA9		_	_	35	0	_	
PMA10		_	_	12	0	_	
PMCS1	23	26	29	15	0	_	Parallel Master Port Chip Select 1 strobe
	20 ⁽²⁾	23 ⁽²⁾	26 ⁽²⁾	10 ⁽²⁾	1/0	TTI /CT	Parallel Master Port data (Demultiplexed
	1 ⁽³⁾	4 ⁽³⁾	35 ⁽³⁾	21 ⁽³⁾	1/0	111/31	Master mode) or address/data
	19 (2)	22 ⁽²⁾	25 ⁽²⁾	9 (2)	1/0	TTI /CT	(Multiplexed Master modes)
	2 ⁽³⁾	5 ⁽³⁾	36 ⁽³⁾	22 ⁽³⁾	1/0	111/31	
	18 ⁽²⁾	21 ⁽²⁾	24 ⁽²⁾	8 ⁽²⁾	1/0	TTI /ST	
	ვ(3)	6 ⁽³⁾	1 ⁽³⁾	23 ⁽³⁾	1/0	116/01	
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12 ⁽²⁾	15 ⁽²⁾	16 ⁽²⁾	42 ⁽²⁾	1/0	TTI /CT	1
	28 ⁽³⁾	3(3)	34 (3)	20 ⁽³⁾	1/0	111/31	
PMD7	11(2)	14 ⁽²⁾	15 (2)	41 ⁽²⁾	1/0	TTI /ST	
	27 ⁽³⁾	2 ⁽³⁾	33 (3)	19 ⁽³⁾	1/0	112/01	
PMRD	21	24	27	11	0	—	Parallel Master Port read strobe
	22 ⁽²⁾	25 ⁽²⁾	28 ⁽²⁾	14 ⁽²⁾	0		Parallel Master Port write strope
	4 ⁽³⁾	7 ⁽³⁾	2 ⁽³⁾	24 ⁽³⁾	Ŭ		T arallel master Fort while strobe
VBUS	12 ⁽³⁾	15 ⁽³⁾	16 (3)	42 ⁽³⁾	Ι	Analog	USB bus power monitor
VUSB3V3	20 ⁽³⁾	23 ⁽³⁾	26 ⁽³⁾	10 ⁽³⁾	Р	_	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22 ⁽³⁾	25 ⁽³⁾	28 ⁽³⁾	14 ⁽³⁾	0		USB Host and OTG bus power control output
D+	18 ⁽³⁾	21 ⁽³⁾	24 ⁽³⁾	8 ⁽³⁾	I/O	Analog	USB D+
D-	19 ⁽³⁾	22 ⁽³⁾	25 ⁽³⁾	9(3)	I/O	Analog	USB D-
Legend:	CMOS = C	MOS compa	atible input	or output		Analog =	Analog input P = Power
	ST = Schmi	tt Trigger in	put with CN	NOS levels		O = Outp	but I=Input
	TTL = TTL input buffer					PPS = P	eripheral Pin Select — = N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

Exception	Description
Reset	Assertion MCLR or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Вр	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

TABLE 3-3: MIPS32[®] M4K[®] PROCESSOR CORE EXCEPTION TYPES

3.3 Power Management

The MIPS M4K processor core offers many power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see Section 26.0 "Power-Saving Features".

3.4 EJTAG Debug Support

The MIPS M4K processor core provides an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

4.2 Bus Matrix Control Registers

TABLE 4-2: BUS MATRIX REGISTER MAP

ess)		ø										Bits							
Virtual Addr (BF88_#	Register Name	Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000		31:16	_		_	_	—	_		_	_	—	_	BMXERRIXI	BMXERRICD	BMXERRDMA	BMXERRDS	BMXERRIS	001F
2000	BINIXCON	15:0		_	_	_	_	-		—	_	BMXWSDRM	_	_	—	BI	MXARB<2:0>		0041
2010		31:16	_		_		_	_		_	_	_	_	_	—	_	_	_	0000
2010	DIVIADAPDA'	15:0									BN	IXDKPBA<15:0>	>						0000
2020		31:16	_					_		—	_	—	—	_	—		_		0000
2020	BINIADODBA	15:0									BM	XDUDBA<15:0	>						0000
2030		31:16	—	_	_		_	—	_	—	—	—	—	—	—	—	—	-	0000
2000		15:0									BN	IXDUPBA<15:0>	>						0000
2040	BMXDRMS7	31:16		BMXDRMSZ<31:0>										xxxx					
2040	DIVINDI (IVIOZ	15:0		BMADKMSZ<31:0>										xxxx					
2050		31:16	—	—				—	_	—	—		_	_		BMXPUPBA	<19:16>		0000
2000		15:0									BN	IXPUPBA<15:0>	>						0000
2060	BMYDEMS7	31:16									BM								xxxx
2000									xxxx										
2070	BMXBOOTS7	31:16									BW	XBOOTS7<31-0							0000
2070 BMXBOOTSZ		15:0									DIVI	ADOUT32531.0	~						0C00

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

5.1 Flash Controller Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

ess		Ċ,		Bits															
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E400		31:16		—	—	—	—		—	—	—	—	—	_	_	—			0000
1400		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	_	_	_	_	_	_			NVMO	P<3:0>		0000
E410		31:16									/~21.0>								0000
1410		15:0									S1.02								0000
E420		31:16									D-21.05								0000
F420	NVINADUR' /	15:0								INVIVIADD	K~31.0~								0000
E420		31:16									A 221:05								0000
F430	NVINDATA	15:0								NVIVIDAL	AS1.02								0000
E440		31:16							N		21.05								0000
F440	NVIVISRCADDR	15:0	5:0 NVMSRCADDR<31:0>										0000						

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	_	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
10.0	—	—	—	—	—	5	6RIPL<2:0> ⁽¹⁾	
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	—	—			VEC	<5:0> ⁽¹⁾		

REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 Unimplemented: Read as '0'

- bit 10-8 SRIPL<2:0>: Requested Priority Level bits⁽¹⁾
 - 111-000 = The priority level of the latest interrupt presented to the CPU
- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 VEC<5:0>: Interrupt Vector bits⁽¹⁾ 11111-00000 = The interrupt vector that is presented to the CPU
- Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31.24	IPTMR<31:24>									
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	IPTMR<23:16>									
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15.0	IPTMR<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7.0				IPTM	IR<7:0>					

REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

REGIST	ER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)
bit 9-8	IS01<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0
bit 7-5	Unimplemented: Read as '0'
bit 4-2	IP00<2:0>: Interrupt Priority bits
	<pre>111 = Interrupt priority is 7</pre>
	010 = Interrupt priority is 2 001 = Interrupt priority is 1 000 = Interrupt is disabled
bit 1-0	IS00<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0
Note:	This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bir definitions.

FIGURE 8-1: OSCILLATOR DIAGRAM



 Refer to Section 6. "Oscillator Configuration" (DS60001112) in the "PIC32 Family Reference Manual" for help in determinin best oscillator components.

3. The PBCLK out is only available on the OSC2 pin in certain clock modes.

4. The USB PLL is only available on PIC32MX2XX devices.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—		_	_	_	-	_	_
45.0	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_			TUN<	5:0> (1)		

REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Legend:

Logonal			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 Unimplemented: Read as '0'

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	—			R)<2017<20	1,3)		
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16				RODIV<	:7:0> (1,3)		Bit 25/17/9/1 R/W-0 R/W-0, HC DIVSWEN R/W-0 L<3:0>(1)	
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
15:8	ON	_	SIDL	OE	RSLP ⁽²⁾	-	DIVSWEN	ACTIVE
	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0		_	_	_		ROSEL	<3:0>(1)	

REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

Legend:	HC = Hardware Clearable	HS = Hardware Settable	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 Unimplemented: Read as '0'

bit 30-16	RODIV<14:0> Reference Clock Divider bits ^(1,3)
	The value selects the reference clock divider bits. See Figure 8-1 for information.
bit 15	ON: Output Enable bit
	1 = Reference Oscillator module is enabled
	0 = Reference Oscillator module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Peripheral Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
 - 0 =Continue module operation when the device enters lide mode
- bit 12 **OE:** Reference Clock Output Enable bit
 - 1 = Reference clock is driven out on REFCLKO pin
 - 0 = Reference clock is not driven out on REFCLKO pin
- bit 11 RSLP: Reference Oscillator Module Run in Sleep bit⁽²⁾
 - 1 = Reference Oscillator module output continues to run in Sleep
 - 0 = Reference Oscillator module output is disabled in Sleep
- bit 10 Unimplemented: Read as '0'
- bit 9 DIVSWEN: Divider Switch Enable bit
 - 1 = Divider switch is in progress
 - 0 = Divider switch is complete
- bit 8 ACTIVE: Reference Clock Request Status bit
 - 1 = Reference clock request is active
 - 0 = Reference clock request is not active
- bit 7-4 Unimplemented: Read as '0'
- **Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
 - **2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
 - 3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0						
31.24	—	—	—	—	—	—	—	—
22:16	U-0	U-0						
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0						
15.0	—	—	—	—	—	—	—	—
	R/WC-0, HS	R/WC-0, HS						
7:0	BISEE						CRC5EF ⁽⁴⁾	DIDEE
	DIGLI	DIVIALI		DIOLI		GINGTOLI	EOFEF ^(3,5)	

REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

- bit 31-8 Unimplemented: Read as '0'
- bit 7 BTSEF: Bit Stuff Error Flag bit
 - 1 = Packet rejected due to bit stuff error
 - 0 = Packet accepted
- bit 6 BMXEF: Bus Matrix Error Flag bit
 - 1 = The base address, of the Buffer Descriptor Table, or the address of an individual buffer pointed to by a Buffer Descriptor Table entry, is invalid.
 - 0 = No address error
- bit 5 DMAEF: DMA Error Flag bit⁽¹⁾
 - 1 = USB DMA error condition detected
 - 0 = No DMA error
- bit 4 BTOEF: Bus Turnaround Time-Out Error Flag bit⁽²⁾
 - 1 = Bus turnaround time-out has occurred
 - 0 = No bus turnaround time-out
- bit 3 **DFN8EF:** Data Field Size Error Flag bit
 - 1 = Data field received is not an integral number of bytes
 - 0 = Data field received is an integral number of bytes
- bit 2 CRC16EF: CRC16 Failure Flag bit
 - 1 = Data packet rejected due to CRC16 error
 - 0 = Data packet accepted
- **Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
 - **2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
 - **3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
 - 4: Device mode.
 - 5: Host mode.

		•••••						
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—		—	—			—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	—		_	_			_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	-	—	—		-	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0				BDTPTR	H<23:16>			

REGISTER 10-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **BDTPTRH<23:16>:** Buffer Descriptor Table Base Address bits This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	—	_	—	—	_	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0				BDTPTR	U<31:24>			

REGISTER 10-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **BDTPTRU<31:24>:** Buffer Descriptor Table Base Address bits This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	—	FEDGE	C32
7.0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
7:0	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>	

REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unkno	own)	P = Programmable bit	r = Reserved bit

bit 31-16	Unimplemented: Read as '0'
bit 15	ON: Input Capture Module Enable bit ⁽¹⁾
	1 = Module is enabled
	0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Stop in Idle Control bit
	1 = Halt in Idle mode0 = Continue to operate in Idle mode
bit 12-10	Unimplemented: Read as '0'
bit 9	FEDGE: First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
	1 = Capture rising edge first
	0 = Capture falling edge first
bit 8	C32: 32-bit Capture Select bit
	1 = 32-bit timer resource capture
	0 = 16-bit timer resource capture
bit 7	ICTMR: Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
	0 = Timer3 is the counter source for capture
DIT 6-5	ICI<1:0>: Interrupt Control bits
	10 = Interrupt on every tourth capture event
	01 = Interrupt on every second capture event
	00 = Interrupt on every capture event
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
	1 = Input capture overflow has occurred
	0 = No input capture overflow has occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	 1 = Input capture buffer is not empty; at least one more capture value can be read 0 = Input capture buffer is empty
Note 1:	When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the
	STOCEN Gyole infinediately following the instruction that deals the module's ON bit.

REGISTER 18-2: I2CxSTAT: I²C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	-	—	_	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	_	—	—	—	—
45.0	R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
15:8	ACKSTAT	TRSTAT	—	-	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
7:0	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF

Legend:	HS = Set in hardware	HSC = Hardware set/cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit	

bit 31-16 Unimplemented: Read as '0'

bit 15 ACKSTAT: Acknowledge Status bit (when operating as I²C master, applicable to master transmit operation) 1 = Acknowledge was not received from slave 0 = Acknowledge was received from slave Hardware set or clear at end of slave Acknowledge. bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK) 0 = Master transmit is not in progress Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge. bit 13-11 Unimplemented: Read as '0' bit 10 BCL: Master Bus Collision Detect bit 1 = A bus collision has been detected during a master operation 0 = No collisionHardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module. bit 9 GCSTAT: General Call Status bit 1 = General call address was received 0 = General call address was not received Hardware set when address matches general call address. Hardware clear at Stop detection. bit 8 ADD10: 10-bit Address Status bit 1 = 10-bit address was matched 0 = 10-bit address was not matched Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 IWCOL: Write Collision Detect bit

1 = An attempt to write the I2C>	TRN register failed because the I ² C module is busy
0 = No collision	

Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

- bit 6 I2COV: Receive Overflow Flag bit
 - 1 = A byte was received while the I2CxRCV register is still holding the previous byte 0 = No overflow

Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I²C slave)

- 1 = Indicates that the last byte received was data
- 0 = Indicates that the last byte received was device address

Hardware clear at device address match. Hardware set by reception of slave byte.

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)

- 1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
 - 0 = Normal operation, buffer contents will be overwritten by the next conversion sequence
- bit 3 Unimplemented: Read as '0'
- bit 2 **ASAM:** ADC Sample Auto-Start bit

1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.

- 0 = Sampling begins when SAMP bit is set
- bit 1 SAMP: ADC Sample Enable bit⁽²⁾

1 = The ADC sample and hold amplifier is sampling

0 = The ADC sample/hold amplifier is holding

When ASAM = 0, writing '1' to this bit starts sampling.

When SSRC = 000, writing '0' to this bit will end sampling and start conversion.

- bit 0 DONE: Analog-to-Digital Conversion Status bit⁽³⁾
 1 = Analog-to-digital conversion is done
 0 = Analog-to-digital conversion is not done or has not started Clearing this bit will not affect any operation in progress.
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

23.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer Section 19. to "Comparator" (DS60001110), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Analog Comparator module contains three comparators that can be configured in a variety of ways.

Following are some of the key features of this module:

- Selectable inputs available include:
 - Analog inputs multiplexed with I/O pins
 - On-chip internal absolute voltage reference (IVREF)
 - Comparator voltage reference (CVREF)
- · Outputs can be Inverted
- Selectable interrupt generation

A block diagram of the comparator module is provided in Figure 23-1.



TABLE 30-14: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	_	_	10	μs	See Note 1
D313	DACREFH	EFH CVREF Input Voltage	AVss	—	AVDD	V	CVRSRC with CVRSS = 0
	Reference Range	VREF-	—	VREF+	V	CVRSRC with CVRSS = 1	
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24	-	CVRCON <cvrr> = 1</cvrr>
			_	—	DACREFH/32	_	CVRCON <cvrr> = 0</cvrr>
D316	DACACC	Absolute Accuracy ⁽²⁾		_	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>
			—	_	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 30-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D321	Cefc	External Filter Capacitor Value	8	10	_	μF	Capacitor must be low series resistance (1 ohm). Typical voltage on the VCAP pin is 1.8V.



TYPICAL FRC FREQUENCY @ VDD = 3.3V



FIGURE 32-6:

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimensi	Dimension Limits		NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- Product Support Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- General Technical Support Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- Business of Microchip Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV — ISO/TS 16949—

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

 $\ensuremath{\mathsf{SQTP}}$ is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2011-2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN:978-1-5224-0471-2