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#### Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f128dt-v-tl

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		Pin Nu	mber <sup>(1)</sup>				
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
OC1	PPS	PPS	PPS	PPS	0	_	Output Compare Output 1
OC2	PPS	PPS	PPS	PPS	0	—	Output Compare Output 2
OC3	PPS	PPS	PPS	PPS	0	—	Output Compare Output 3
OC4	PPS	PPS	PPS	PPS	0	—	Output Compare Output 4
OC5	PPS	PPS	PPS	PPS	0	—	Output Compare Output 5
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault B Input
INT0	13	16	17	43	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4
RA0	27	2	33	19	I/O	ST	PORTA is a bidirectional I/O port
RA1	28	3	34	20	I/O	ST	1
RA2	6	9	7	30	I/O	ST	1
RA3	7	10	8	31	I/O	ST	1
RA4	9	12	10	34	I/O	ST	1
RA7	_	_	_	13	I/O	ST	1
RA8	_	_	_	32	I/O	ST	
RA9	_	_	_	35	I/O	ST	1
RA10	_	_	_	12	I/O	ST	
RB0	1	4	35	21	I/O	ST	PORTB is a bidirectional I/O port
RB1	2	5	36	22	I/O	ST	7
RB2	3	6	1	23	I/O	ST	7
RB3	4	7	2	24	I/O	ST	
RB4	8	11	9	33	I/O	ST	
RB5	11	14	15	41	I/O	ST	
RB6	12 <sup>(2)</sup>	15 <b>(2)</b>	16 <b>(2)</b>	42 <sup>(2)</sup>	I/O	ST	
RB7	13	16	17	43	I/O	ST	
RB8	14	17	18	44	I/O	ST	
RB9	15	18	19	1	I/O	ST	
RB10	18	21	24	8	I/O	ST	
RB11	19	22	25	9	I/O	ST	
RB12	20 <sup>(2)</sup>	23 <sup>(2)</sup>	26 <sup>(2)</sup>	10 <sup>(2)</sup>	I/O	ST	1
RB13	21	24	27	11	I/O	ST	1
RB14	22	25	28	14	I/O	ST	1
RB15	23	26	29	15	I/O	ST	
Legend:	CMOS = C	MOS compa	atible input	or output		Analog =	Analog input P = Power
	SI = Schmi	tt Irigger in	put with CN	VIOS levels		O = Outp	orinhoral Din Solart
Note 1.			lod for rofo	ronco only	See the	"Pin Diag	$m_{\text{rem}} = N/A$

#### DINOUT I/O DESCRIPTIONS (CONTINUED)

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

		Pin Nu	mber <sup>(1)</sup>				
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		_	_	27	0	_	Parallel Master Port address
PMA3				38	0	—	(Demultiplexed Master modes)
PMA4				37	0	—	
PMA5		_	_	4	0	_	
PMA6		_	_	5	0	_	
PMA7				13	0	—	
PMA8		_	_	32	0	_	
PMA9		_	_	35	0	_	
PMA10		_	_	12	0	_	
PMCS1	23	26	29	15	0	_	Parallel Master Port Chip Select 1 strobe
	20 <sup>(2)</sup>	23 <sup>(2)</sup>	26 <sup>(2)</sup>	10 <sup>(2)</sup>	1/0	TTI /CT	Parallel Master Port data (Demultiplexed
	1 <sup>(3)</sup>	4 <sup>(3)</sup>	35 <sup>(3)</sup>	21 <sup>(3)</sup>	1/0	111/31	Master mode) or address/data
	19 <b>(2)</b>	22 <sup>(2)</sup>	25 <sup>(2)</sup>	9 <b>(2)</b>	1/0	TTI /CT	(Multiplexed Master modes)
	2 <sup>(3)</sup>	5 <sup>(3)</sup>	36 <sup>(3)</sup>	22 <sup>(3)</sup>	1/0	111/31	
	18 <sup>(2)</sup>	21 <sup>(2)</sup>	24 <sup>(2)</sup>	8 <sup>(2)</sup>	1/0	TTI /ST	
	ვ( <b>3</b> )	6 <sup>(3)</sup>	1 <sup>(3)</sup>	23 <sup>(3)</sup>	1/0	116/01	
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12 <sup>(2)</sup>	15 <sup>(2)</sup>	16 <sup>(2)</sup>	42 <sup>(2)</sup>	1/0	TTI /CT	1
	28 <sup>(3)</sup>	3(3)	34 <b>(3)</b>	20 <sup>(3)</sup>	1/0	111/31	
PMD7	11(2)	14 <sup>(2)</sup>	15 <b>(2)</b>	41 <sup>(2)</sup>	1/0	TTI /ST	
	27 <sup>(3)</sup>	2 <sup>(3)</sup>	33 <b>(3)</b>	19 <sup>(3)</sup>	1/0	112/01	
PMRD	21	24	27	11	0	—	Parallel Master Port read strobe
	22 <sup>(2)</sup>	25 <sup>(2)</sup>	28 <sup>(2)</sup>	14 <sup>(2)</sup>	0		Parallel Master Port write strope
	4 <sup>(3)</sup>	7 <sup>(3)</sup>	2 <sup>(3)</sup>	24 <sup>(3)</sup>	Ŭ		T arallel master Fort while strobe
VBUS	12 <sup>(3)</sup>	15 <sup>(3)</sup>	16 <b>(3)</b>	42 <sup>(3)</sup>	Ι	Analog	USB bus power monitor
VUSB3V3	20 <sup>(3)</sup>	23 <sup>(3)</sup>	26 <sup>(3)</sup>	10 <sup>(3)</sup>	Р	_	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22 <sup>(3)</sup>	25 <sup>(3)</sup>	28 <sup>(3)</sup>	14 <sup>(3)</sup>	0		USB Host and OTG bus power control output
D+	18 <sup>(3)</sup>	21 <sup>(3)</sup>	24 <sup>(3)</sup>	8 <sup>(3)</sup>	I/O	Analog	USB D+
D-	19 <sup>(3)</sup>	22 <sup>(3)</sup>	25 <sup>(3)</sup>	9(3)	I/O	Analog	USB D-
Legend:	CMOS = C	MOS compa	atible input	or output		Analog =	Analog input P = Power
	ST = Schmi	tt Trigger in	put with CN	NOS levels		O = Outp	but I=Input
	L  =   L	nput buffer				PPS = P	eripheral Pin Select — = N/A

#### 

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

#### TABLE 4-1: SFR MEMORY MAP

	Virtual Ac	ddress
Peripheral	Base	Offset Start
Watchdog Timer		0x0000
RTCC		0x0200
Timer1-5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
IC1 and IC2		0x5000
SPI1 and SPI2		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC	0xBF80	0x9000
CVREF		0x9800
Comparator		0xA000
CTMU		0xA200
Oscillator		0xF000
Device and Revision ID		0xF220
Peripheral Module Disable		0xF240
Flash Controller		0xF400
Reset		0xF600
PPS		0xFA04
Interrupts		0x1000
Bus Matrix		0x2000
DMA	0xBF88	0x3000
USB		0x5050
PORTA-PORTC		0x6000
Configuration	0xBFC0	0x0BF0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
31:24	—	—	_	—	—		—	—				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
23:10	—	—	_	—	—	—	—	—				
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0				
15:8		BMXDUPBA<15:8>										
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0				
7:0		BMXDUPBA<7:0>										

# REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER

# Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUPBA<15:10>: DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** Read-Only bits This value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	_	—	_		_	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R-0	R-0	R-0	U-0	U-0	U-0
15:8	WR	WREN	WRERR <sup>(1)</sup>	LVDERR <sup>(1)</sup>	LVDSTAT <sup>(1)</sup>	—	_	—
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_		_	NVMOP<3:0>			

#### REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	id as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15	WR: Write Control bit
	This bit is writable when WREN = 1 and the unlock sequence is followed.
	<ul> <li>1 = Initiate a Flash operation. Hardware clears this bit when the operation completes</li> <li>0 = Flash operation is complete or inactive</li> </ul>
bit 14	WREN: Write Enable bit
	This is the only bit in this register reset by a device Reset.
	<ul> <li>1 = Enable writes to WR bit and enables LVD circuit</li> <li>0 = Disable writes to WR bit and disables LVD circuit</li> </ul>
bit 13	WRERR: Write Error bit <sup>(1)</sup>
	This bit is read-only and is automatically set by hardware.
	<ul> <li>1 = Program or erase sequence did not complete successfully</li> <li>0 = Program or erase sequence completed normally</li> </ul>
bit 12	LVDERR: Low-Voltage Detect Error bit (LVD circuit must be enabled) <sup>(1)</sup>
	This bit is read-only and is automatically set by hardware.
	<ul> <li>1 = Low-voltage detected (possible data corruption, if WRERR is set)</li> <li>0 = Voltage level is acceptable for programming</li> </ul>
bit 11	LVDSTAT: Low-Voltage Detect Status bit (LVD circuit must be enabled) <sup>(1)</sup>
	This bit is read-only and is automatically set and cleared by the hardware.
	1 = Low-voltage event is active
	0 = Low-voltage event is not active
bit 10-4	Unimplemented: Read as '0'
bit 3-0	NVMOP<3:0>: NVM Operation bits
	These bits are writable when WREN = 0.
	1111 = Reserved
	•
	0111 = Reserved
	0110 = No operation
	<ul> <li>0101 = Program Flash Memory (PFM) erase operation: erases PFM, if all pages are not write-protected</li> <li>0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected</li> <li>0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected</li> </ul>
	0010 = No operation
	0000 = No operation

**Note 1:** This bit is cleared by setting NVMOP == `b0000, and initiating a Flash operation (i.e., WR).

# TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

(1)	IRQ Vector Interrupt Bit Location				Persistent		
Interrupt Source <sup>(1)</sup>	#	#	Flag	Enable	Priority	Sub-priority	Interrupt
		Highes	st Natural O	rder Priority	,		
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1E – SPI1 Fault	36	31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1TX – SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24 — RODI					DDIV<14:8>(1,3)						
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:16		RODIV<7:0> <sup>(1,3)</sup>									
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC			
15:8	ON	_	SIDL	OE	RSLP <sup>(2)</sup>	-	DIVSWEN	ACTIVE			
	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0		_	_	_	ROSEL<3:0> <sup>(1)</sup>						

#### **REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

Legend:	HC = Hardware Clearable			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31 Unimplemented: Read as '0'

bit 30-16	RODIV<14:0> Reference Clock Divider bits <sup>(1,3)</sup>
	The value selects the reference clock divider bits. See Figure 8-1 for information.
bit 15	ON: Output Enable bit
	1 = Reference Oscillator module is enabled
	0 = Reference Oscillator module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Peripheral Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
  - 0 =Continue module operation when the device enters lide mode
- bit 12 **OE:** Reference Clock Output Enable bit
  - 1 = Reference clock is driven out on REFCLKO pin
  - 0 = Reference clock is not driven out on REFCLKO pin
- bit 11 RSLP: Reference Oscillator Module Run in Sleep bit<sup>(2)</sup>
  - 1 = Reference Oscillator module output continues to run in Sleep
  - 0 = Reference Oscillator module output is disabled in Sleep
- bit 10 Unimplemented: Read as '0'
- bit 9 DIVSWEN: Divider Switch Enable bit
  - 1 = Divider switch is in progress
    - 0 = Divider switch is complete
- bit 8 ACTIVE: Reference Clock Request Status bit
  - 1 = Reference clock request is active
  - 0 = Reference clock request is not active
- bit 7-4 Unimplemented: Read as '0'
- **Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
  - **2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
  - 3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

# 11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

# 11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

# 11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digitalonly peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I<sup>2</sup>C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin.

Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

#### 11.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

# 11.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

#### FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



#### TABLE 11-5: PORTC REGISTER MAP

ess	_											Bits							(0
Virtual Addr (BF88_#)	Register Name <sup>(1,2</sup> )	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6200		31:16	_	—	—	—	—	—	—	—	—	—	—	—	—	—	_	—	0000
0200	ANOLLO	15:0	_	—	_	—	—	—	—	—	—	—	—	—	ANSC3 <sup>(4)</sup>	ANSC2 <sup>(3)</sup>	ANSC1	ANSC0	000F
6210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	_	—	0000
0210	11100	15:0	_	—		—	—	—	TRISC9	TRISC8 <sup>(3)</sup>	TRISC7 <sup>(3)</sup>	TRISC6 <sup>(3)</sup>	TRISC5 <sup>(3)</sup>	TRISC4 <sup>(3)</sup>	TRISC3	TRISC2 <sup>(3)</sup>	TRISC1	TRISC0	03FF
6220	PORTO	31:16	_	—		—	—	—		—	—	—	—						0000
0220	1 OKTO	15:0	_	—		—	—	—	RC9	RC8 <sup>(3)</sup>	RC7 <sup>(3)</sup>	RC6 <sup>(3)</sup>	RC5 <sup>(3)</sup>	RC4 <sup>(3)</sup>	RC3	RC2 <sup>(3)</sup>	RC1	RC0	xxxx
6230	LATC	31:16	_	—		—	—	—		—	—	—	—	—	—			—	0000
0200		15:0	_	—		—	—	—	LATC9	LATC8 <sup>(3)</sup>	LATC7 <sup>(3)</sup>	LATC6 <sup>(3)</sup>	LATC5 <sup>(3)</sup>	LATC4 <sup>(3)</sup>	LATC3	LATC2 <sup>(3)</sup>	LATC1	LATC0	xxxx
6240	ODCC	31:16	_	—		—	—	—		—	—	—	—	—	—			—	0000
0240	ODCC	15:0	_	—		—	—	—	ODCC9	ODCC8 <sup>(3)</sup>	ODCC7 <sup>(3)</sup>	ODCC6 <sup>(3)</sup>	ODCC5 <sup>(3)</sup>	ODCC4 <sup>(3)</sup>	ODCC3	ODCC2 <sup>(3)</sup>	ODCC1	ODCC0	0000
6250	CNDUC	31:16	_	—		—	—	—		—	—	—	—	—	—			—	0000
0230	CINFUC	15:0	_	—		—	—	—	CNPUC9	CNPUC8 <sup>(3)</sup>	CNPUC7 <sup>(3)</sup>	CNPUC6 <sup>(3)</sup>	CNPUC5 <sup>(3)</sup>	CNPUC4 <sup>(3)</sup>	CNPUC3	CNPUC2 <sup>(3)</sup>	CNPUC1	CNPUC0	0000
6260		31:16	_	—	—	—	—	—		_	—	_	—	_	_		_	—	0000
0200	CINFDC	15:0	_	—	—	—	—	—	CNPDC9	CNPDC8 <sup>(3)</sup>	CNPDC7 <sup>(3)</sup>	CNPDC6 <sup>(3)</sup>	CNPDC5 <sup>(3)</sup>	CNPDC4 <sup>(3)</sup>	CNPDC3	CNPDC2 <sup>(3)</sup>	CNPDC1	CNPDC0	0000
6270	CNCONC	31:16	_	—	—	—	—	—		_	—	_	—	_	_		_	—	0000
0270	CINCOINC	15:0	ON	—	SIDL	—	—	—		_	—	_	—	_	_		_	—	0000
6000		31:16		_	_	_	—	—	—	—	—	—	—	—	_	—		_	0000
0200	CINEINC	15:0	-	_	—	—	—	—	CNIEC9	CNIEC8 <sup>(3)</sup>	CNIEC7 <sup>(3)</sup>	CNIEC6 <sup>(3)</sup>	CNIEC5 <sup>(3)</sup>	CNIEC4 <sup>(3)</sup>	CNIEC3	CNIEC2 <sup>(3)</sup>	CNIEC1	CNIEC0	0000
6200	CNOTATO	31:16		_	_	_	_	—	_	—	—	—	_	—	_	_	_		0000
6290	CINSTATC	15:0		_	_	_	_	—	CNSTATC9	CNSTATC8(3)	CNSTATC7(3)	CNSTATC6(3)	CNSTATC5(3)	CNSTATC4(3)	CNSTATC3	CNSTATC2(3)	CNSTATC1	CNSTATCO	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: PORTC is not available on 28-pin devices.

3: This bit is only available on 44-pin devices.

4: This bit is only available on USB-enabled devices with 36 or 44 pins.

#### TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP

SS			Bits																
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
EBOO		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	_	0000
1 800	NEAUN	15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPAC	<3:0>		0000
FB04	RPA1R	31:16	_	_	—	—	—	_		—			_	—	—		—	—	0000
1 004	NAIN	15:0	_	_	—	—	—	_		—			_	—		RPA1	<3:0>		0000
FB08	RPA2R	31:16	_		—	—	—	—	—	_			—	_	—	—	—	—	0000
1 000		15:0	_		—	—	—	—	—	_			—	_		RPA2	<3:0>		0000
FB0C	RPA3R	31:16	—	—	—	—	—	—	-	—	—	—	—	—	—	—	—	—	0000
1 800		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPA3	<3:0>		0000
FB10	RPA4R	31:16	—	-	—	—	—	-	-	—	—	—	-	—	—	—	—	—	0000
1 0 10		15:0	—	-	—	—	—	-	-	—	—	—	-	—		RPA4	<3:0>		0000
FB20	RPA8R(1)	31:16			—	—	—			—			—	—	—	—	—	—	0000
1 020		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPA8	<3:0>		0000
FB24	RPA9R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—			—	0000
1 02 1		15:0			—	—	—			—			—	—		RPAS	<3:0>		0000
FB2C	RPB0R	31:16	_		—	—	—			—	_	_		—	—	—	—	—	0000
. 520		15:0	_		—	—	—			—	_	_		—		RPBC	<3:0>		0000
FB30	RPB1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—					0000
		15:0	—	—	—			—	—	—	—	—	—	—		RPB1	<3:0>		0000
FB34	RPB2R	31:16	—		—					—	—	—		—	—	—	—	—	0000
		15:0	—	—		—	—	—		—	—	—		—		RPB2	2<3:0>		0000
FB38	RPB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—					0000
		15:0	—		—					—	—	—		—		RPB3	<3:0>		0000
FB3C	RPB4R	31:16	—		—					—	—	—		—	—	—	—	—	0000
		15:0	—		—					—	—	—		—		RPB4	<3:0>		0000
FB40	RPB5R	31:16	_		_					—				—	—		—	—	0000
		15:0	—		—					—	—	—		—		RPB5	5<3:0>		0000
FB44	RPB6R <sup>(2)</sup>	31:16	—		—					—	—	—		—	—		_	—	0000
		15:0	—	-	—	-	-	-	-	—	—	—	-	—		RPB6	6<3:0>		0000
FB48	RPB7R	31:16	—	-	—	-	-	-	-	—	—	—	-	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	1	RPB7	'<3:0>		0000

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x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

This register is only available on 44-pin devices. Note 1:

2: This register is only available on PIC32MX1XX devices.

3: This register is only available on 36-pin and 44-pin devices. PIC32MX1XX/2XX 28/36/44-PIN FAMILY

# REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 3 Unimplemented: Read as '0'
  bit 2 TSYNC: Timer External Clock Input Synchronization Selection bit When TCS = 1: 1 = External clock input is synchronized 0 = External clock input is not synchronized When TCS = 0: This bit is ignored.
  bit 1 TCS: Timer Clock Source Select bit 1 = External clock from TxCKI pin
  - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

# REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

- bit 3 T32: 32-Bit Timer Mode Select bit<sup>(2)</sup>
  - 1 = Odd numbered and even numbered timers form a 32-bit timer
  - 0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2 Unimplemented: Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit<sup>(3)</sup>
  - 1 = External clock from TxCK pin
  - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
  - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
  - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

#### **Input Capture Control Registers** 15.1

AB	LE 15-1:	IN	PUT CA	PTURE	E 1-INPU		URE 5	REGIST	ER MA	2							
ess										Bi	ts						
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1
2000		31:16				—	—		—		—		—	—	—	_	_
2000	IC ICON.	15:0	ON	—	SIDL	—	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2010	IC1BUF	31:16 15:0								IC1BUF	<31:0>						
2200		31:16	_	—	_	_	—	_	—	—	—	-	_	—	—	—	_
2200	1020011	15:0	ON	ON - SIDL FEDGE C32 ICTMR ICI<1:0> ICOV ICBNE ICM<2:0													
2210	IC2BUF	31:16 15:0								IC2BUF	<31:0>						
2400		31:16	—	—	_	_	_	_	_	—	—	—	_	—	_	—	—
2400	IC3CON /	15:0	ON	—	SIDL	_	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2410	IC3BUF	31:16 15:0								IC3BUF	<31:0>						
2600		31:16	_	—	_	_	-	_	—	—	—			—	—	—	—
2000	104001	15:0	ON	_	SIDL	—		—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2610	IC4BUF	31:16 15:0	IC4BUF<31:0>														
2000		31:16	_	_	_	_	—	_	_	_	_		_	—	_	—	_
2800	ICSCON.	15:0	ON	—	SIDL	—	-	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2810	IC5BUF	31:16 15:0								IC5BUF	<31:0>						

# 

Legend:

This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information. Note 1:

All Resets

0000

0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx

16/0

—

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	
15:8	ON <sup>(1)</sup>	—	SIDL	—	—	—	FEDGE	C32	
7.0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	
7:0	ICTMR	ICI<	1:0>	ICOV	ICBNE	ICM<2:0>			

# REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unkno	own)	P = Programmable bit	r = Reserved bit

bit 31-16	Unimplemented: Read as '0'
bit 15	<b>ON:</b> Input Capture Module Enable bit <sup>(1)</sup>
	1 = Module is enabled
	0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Stop in Idle Control bit
	<ul><li>1 = Halt in Idle mode</li><li>0 = Continue to operate in Idle mode</li></ul>
bit 12-10	Unimplemented: Read as '0'
bit 9	FEDGE: First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
	1 = Capture rising edge first
	0 = Capture falling edge first
bit 8	C32: 32-bit Capture Select bit
	1 = 32-bit timer resource capture
	0 = 16-bit timer resource capture
bit 7	ICTMR: Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
	0 = Timer3 is the counter source for capture
DIT 6-5	ICI<1:0>: Interrupt Control bits
	10 = Interrupt on every tourth capture event
	01 = Interrupt on every second capture event
	00 = Interrupt on every capture event
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
	1 = Input capture overflow has occurred
	0 = No input capture overflow has occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	<ul> <li>1 = Input capture buffer is not empty; at least one more capture value can be read</li> <li>0 = Input capture buffer is empty</li> </ul>
Note 1:	When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the
	STOCEN Gyole infinediately following the instruction that deals the module's ON bit.

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# FIGURE 18-1: I<sup>2</sup>C BLOCK DIAGRAM



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	—	—	_		
00.10	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:10	—	—	—	—	—	—	—	—		
	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0		
15:8	_	CS1 <sup>(1)</sup> ADDR14 <sup>(2)</sup>	_	—	—	ADDR<10:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	ADDR<7:0>									

#### REGISTER 20-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

# Legend:

- 3			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 31-15 **Unimplemented:** Read as '0'
- bit 14 **CS1:** Chip Select 1 bit<sup>(1)</sup>
  - 1 = Chip Select 1 is active
  - 0 = Chip Select 1 is inactive
- bit 14 ADDR<14>: Destination Address bit 14<sup>(2)</sup>
- bit 13-11 Unimplemented: Read as '0'
- bit 10-0 ADDR<10:0>: Destination Address bits
- Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10.
  - **2:** When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	_	—	—	—	_	—	—			
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	—	—			
45.0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	ALRMEN <sup>(1,2)</sup>	CHIME <sup>(2)</sup>	PIV <sup>(2)</sup>	ALRMSYNC <sup>(3)</sup>	AMASK<3:0>(2)						
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0		ARPT<7:0> <sup>(2)</sup>									

#### REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 ALRMEN: Alarm Enable bit<sup>(1,2)</sup>
  - 1 = Alarm is enabled
  - 0 = Alarm is disabled

#### bit 14 CHIME: Chime Enable bit<sup>(2)</sup>

- 1 = Chime is enabled ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled ARPT<7:0> stops once it reaches 0x00

#### bit 13 **PIV:** Alarm Pulse Initial Value bit<sup>(2)</sup>

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse. When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

## bit 12 ALRMSYNC: Alarm Sync bit<sup>(3)</sup>

- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

#### bit 11-8 AMASK<3:0>: Alarm Mask Configuration bits<sup>(2)</sup>

- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved; do not use
- 1011 = Reserved; do not use
- 11xx = Reserved; do not use
- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
  - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
  - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

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АС СНА	ARACTER	ISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 4): 2.5V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$								
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions				
Clock P	Clock Parameters										
AD50	TAD	ADC Clock Period <sup>(2)</sup>	65	_	_	ns	See Table 30-35				
Conver	Conversion Rate										
AD55	TCONV	Conversion Time	—	12 Tad	—		—				
AD56	FCNV Throughput Rate			—	1000	ksps	AVDD = 3.0V to 3.6V				
		(Sampling Speed)		—	400	ksps	AVDD = 2.5V to 3.6V				
AD57	TSAMP	Sample Time	1 Tad	—	—	_	TSAMP must be $\geq$ 132 ns				
Timing	Paramete	rs									
AD60	TPCS	Conversion Start from Sample Trigger <sup>(3)</sup>	_	1.0 Tad	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected				
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 Tad	_	1.5 TAD	—	—				
AD62 TCSS Conversion Completion to Sample Start (ASAM = 1) <sup>(3)</sup>		—	0.5 TAD	—	_	_					
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On <sup>(3)</sup>	_	—	2	μS	_				

# TABLE 30-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

**3:** Characterized by design but not tested.

**4:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.