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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256b-50i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256b-50i-ml</a>

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 5: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES**

<b>28-PIN QFN (TOP VIEW)<sup>(1,2,3,4)</sup></b>  <b>PIC32MX110F016B</b> <b>PIC32MX120F032B</b> <b>PIC32MX130F064B</b> <b>PIC32MX130F256B</b> <b>PIC32MX150F128B</b> <b>PIC32MX170F256B</b>				28	1
Pin #	Full Pin Name	Pin #	Full Pin Name		
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9		
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	16	VSS		
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	17	VCAP		
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	18	PGED2/RPB10/CTED11/PMD2/RB10		
5	VSS	19	PGEC2/TMS/RPB11/PMD1/RB11		
6	OSC1/CLKI/RPA2/RA2	20	AN12/PMD0/RB12		
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13		
8	SOSCI/RPB4/RB4	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14		
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15		
10	VDD	24	AVSS		
11	PGED3/RPB5/PMD7/RB5	25	AVDD		
12	PGEC3/RPB6/PMD6/RB6	26	MCLR		
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0		
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	VREF-/CVREF-/AN1/RPA1/CTED2/RA1		

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
  - 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
  - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
  - 4: Shaded pins are 5V tolerant.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUs

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

### 2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX 28/36/44-pin Family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see 2.2 “Decoupling Capacitors”)
- All AVDD and AVSS pins, even if the ADC module is not used (see 2.2 “Decoupling Capacitors”)
- VCAP pin (see 2.3 “Capacitor on Internal Voltage Regulator (VCAP)”)
- MCLR pin (see 2.4 “Master Clear (MCLR) Pin”)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see 2.5 “ICSP Pins”)
- OSC1 and OSC2 pins, when external oscillator source is used (see 2.7 “External Oscillator Pins”)

The following pins may be required:

- VREF+/VREF- pins – used when external voltage reference for the ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

### 2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1  $\mu\text{F}$  (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01  $\mu\text{F}$  to 0.001  $\mu\text{F}$ . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1  $\mu\text{F}$  in parallel with 0.001  $\mu\text{F}$ .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 3.0 CPU

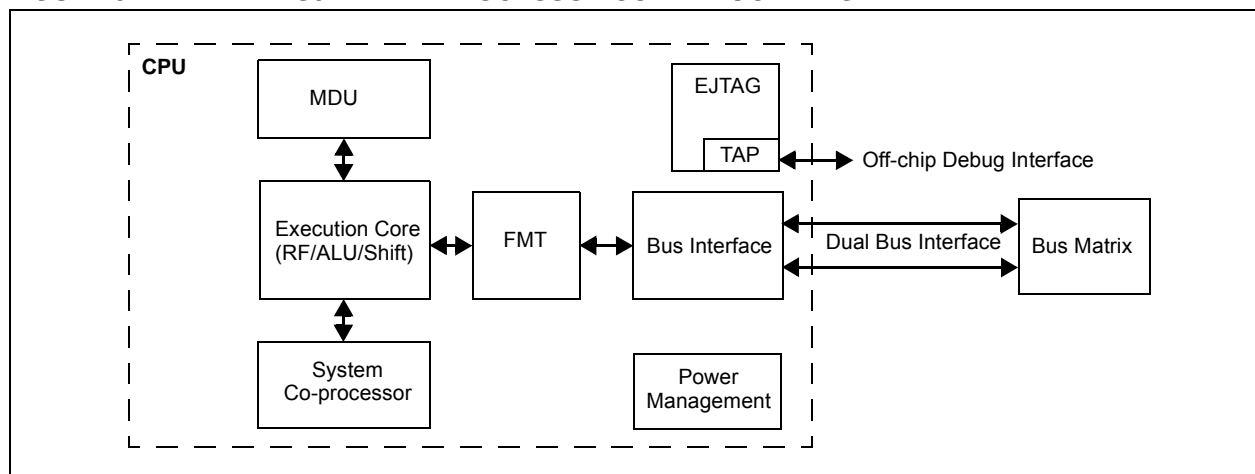
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. “CPU”** (DS60001113), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)). Resources for the MIPS32® M4K® Processor Core are available at: [www.imgtec.com](http://www.imgtec.com).

The MIPS32® M4K® Processor Core is the heart of the PIC32MX1XX/2XX family processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the destinations.

### 3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2)
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - WAIT instruction
  - Conditional move instructions (MOVN, MOVZ)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - Bit field manipulation instructions
- MIPS16e® code compression
  - 16-bit encoding of 32-bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
  - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- Simple dual bus interface
  - Independent 32-bit address and data buses
  - Transactions can be aborted to improve interrupt latency
- Autonomous multiply/divide unit
  - Maximum issue rate of one 32x16 multiply per clock
  - Maximum issue rate of one 32x32 multiply every other clock
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension-dependent)
- Power control
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by WAIT instruction)
  - Extensive use of local gated clocks
- EJTAG debug and instruction trace
  - Support for single stepping
  - Virtual instruction and data address/value
  - Breakpoints

**FIGURE 3-1: MIPS32® M4K® PROCESSOR CORE BLOCK DIAGRAM**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 6-1: RCON: RESET CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
	—	—	—	—	—	—	CMR	VREGS
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR <sup>(1)</sup>	POR <sup>(1)</sup>

<b>Legend:</b>	HS = Set by hardware
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit  
 1 = Configuration mismatch Reset has occurred  
 0 = Configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit  
 1 = Regulator is enabled and is on during Sleep mode  
 0 = Regulator is disabled and is off during Sleep mode

bit 7 **EXTR:** External Reset ( $\overline{\text{MCLR}}$ ) Pin Flag bit  
 1 = Master Clear (pin) Reset has occurred  
 0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit  
 1 = Software Reset was executed  
 0 = Software Reset as not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit  
 1 = WDT Time-out has occurred  
 0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit  
 1 = Device was in Sleep mode  
 0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit  
 1 = Device was in Idle mode  
 0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit<sup>(1)</sup>  
 1 = Brown-out Reset has occurred  
 0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit<sup>(1)</sup>  
 1 = Power-on Reset has occurred  
 0 = Power-on Reset has not occurred

**Note 1:** User software must clear this bit to view next detection.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IP03<2:0>					IS03<1:0>		
23:16	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IP02<2:0>					IS02<1:0>		
15:8	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IP01<2:0>					IS01<1:0>		
7:0	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IP00<2:0>					IS00<1:0>		

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP03<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

•  
•  
•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS03<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP02<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

•  
•  
•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS02<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP01<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

•  
•  
•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-y	R/W-y	R/W-y	R/W-0	R/W-0	R/W-1
	—	—	PLLODIV<2:0>			FRCDIV<2:0>		
23:16	U-0	R-0	R-1	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>		
15:8	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-y	R/W-0
	CLKLOCK	ULOCK <sup>(1)</sup>	SLOCK	SLPEN	CF	UFRocen <sup>(1)</sup>	SOSCEN	OSWEN

**Legend:** y = Value set from Configuration bits on POR  
R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

111 = PLL output divided by 256  
110 = PLL output divided by 64  
101 = PLL output divided by 32  
100 = PLL output divided by 16  
011 = PLL output divided by 8  
010 = PLL output divided by 4  
001 = PLL output divided by 2  
000 = PLL output divided by 1

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

111 = FRC divided by 256  
110 = FRC divided by 64  
101 = FRC divided by 32  
100 = FRC divided by 16  
011 = FRC divided by 8  
010 = FRC divided by 4  
001 = FRC divided by 2 (default setting)  
000 = FRC divided by 1

bit 23 **Unimplemented:** Read as '0'

bit 22 **SOSCRDY:** Secondary Oscillator (Sosc) Ready Indicator bit

1 = The Secondary Oscillator is running and is stable  
0 = The Secondary Oscillator is still warming up or is turned off

bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit

1 = PBDIV<1:0> bits can be written  
0 = PBDIV<1:0> bits cannot be written

bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits

11 = PBCLK is SYSCLK divided by 8 (default)  
10 = PBCLK is SYSCLK divided by 4  
01 = PBCLK is SYSCLK divided by 2  
00 = PBCLK is SYSCLK divided by 1

**Note 1:** This bit is only available on PIC32MX2XX devices.

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the "PIC32 Family Reference Manual" for details.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 10-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/W-0 BTSEE	R/W-0 BMXEE	R/W-0 DMAEE	R/W-0 BTOEE	R/W-0 DFN8EE	R/W-0 CRC16EE	R/W-0 CRC5EE <sup>(1)</sup> EOFEE <sup>(2)</sup>	R/W-0 PIDEE

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit

1 = BTSEF interrupt is enabled

0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit

1 = BMXEF interrupt is enabled

0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit

1 = DMAEF interrupt is enabled

0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit

1 = BTOEF interrupt is enabled

0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit

1 = DFN8EF interrupt is enabled

0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit

1 = CRC16EF interrupt is enabled

0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit<sup>(1)</sup>

1 = CRC5EF interrupt is enabled

0 = CRC5EF interrupt is disabled

**EOFEE:** EOF Error Interrupt Enable bit<sup>(2)</sup>

1 = EOF interrupt is enabled

0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit

1 = PIDEF interrupt is enabled

0 = PIDEF interrupt is disabled

**Note 1:** Device mode.

**2:** Host mode.

**Note:** For an interrupt to propagate the USBIF register, the UERRIE (U1IE<1>) bit must be set.



## 11.4 Ports Control Registers

**TABLE 11-3: PORTA REGISTER MAP**

Virtual Address (BF88..#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSA1	ANSA0	0003
6010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	TRISA10 <sup>(2)</sup>	TRISA9 <sup>(2)</sup>	TRISA8 <sup>(2)</sup>	TRISA7 <sup>(2)</sup>	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
6020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RA10 <sup>(2)</sup>	RA9 <sup>(2)</sup>	RA8 <sup>(2)</sup>	RA7 <sup>(2)</sup>	—	—	RA4	RA3	RA2	RA1	RA0	xxxxx
6030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	LATA10 <sup>(2)</sup>	LATA9 <sup>(2)</sup>	LATA8 <sup>(2)</sup>	LATA7 <sup>(2)</sup>	—	—	LATA4	LATA3	LATA2	LATA1	LATA0	xxxxx
6040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	ODCA10 <sup>(2)</sup>	ODCA9 <sup>(2)</sup>	ODCA8 <sup>(2)</sup>	ODCA7 <sup>(2)</sup>	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
6050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNPUA10 <sup>(2)</sup>	CNPUA9 <sup>(2)</sup>	CNPUA8 <sup>(2)</sup>	CNPUA7 <sup>(2)</sup>	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
6060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNPDA10 <sup>(2)</sup>	CNPDA9 <sup>(2)</sup>	CNPDA8 <sup>(2)</sup>	CNPDA7 <sup>(2)</sup>	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
6070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNIEA10 <sup>(2)</sup>	CNIEA9 <sup>(2)</sup>	CNIEA8 <sup>(2)</sup>	CNIEA7 <sup>(2)</sup>	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
6090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNSTATA10 <sup>(2)</sup>	CNSTATA9 <sup>(2)</sup>	CNSTATA8 <sup>(2)</sup>	CNSTATA7 <sup>(2)</sup>	—	—	CNSTATA4	CNSTATA3	CNSTATA2	CNSTATA1	CNSTATA0	0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.
- 2: This bit is only available on 44-pin devices.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 11-1: [pin name]R: PERIPHERAL PIN SELECT INPUT REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	[pin name]R<3:0>			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **[pin name]R<3:0>**: Peripheral Pin Select Input bits

Where [pin name] refers to the pins that are used to configure peripheral input mapping. See Table 11-1 for input pin selection values.

**Note:** Register values can only be changed if the Configuration bit, IOLOCK (CFGCON<13>), = 0.

**REGISTER 11-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RPnR<3:0>			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **RPnR<3:0>**: Peripheral Pin Select Output bits

See Table 11-2 for output pin selection values.

**Note:** Register values can only be changed if the Configuration bit, IOLOCK (CFGCON<13>), = 0.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
	ON <sup>(1)</sup>	—	SIDL	TWDIS	TWIP	—	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit<sup>(1)</sup>

1 = Timer is enabled

0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit

1 = Writes to Timer1 are ignored until pending write operation completes

0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:

1 = Asynchronous write to the Timer1 register in progress

0 = Asynchronous write to Timer1 register is complete

In Synchronous Timer mode:

This bit is read as '0'.

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits

11 = 1:256 prescale value

10 = 1:64 prescale value

01 = 1:8 prescale value

00 = 1:1 prescale value

**Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 14-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON <sup>(1,2)</sup>	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	—	SWDTPS<4:0>					WDTWINEN	WDTCLR

<b>Legend:</b>	y = Values set from Configuration bits on POR
R = Readable bit	W = Writable bit      U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit<sup>(1,2)</sup>

- 1 = Enables the WDT if it is not enabled by the device configuration
- 0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits  
On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit

- 1 = Enable windowed Watchdog Timer
- 0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit

- 1 = Writing a '1' will clear the WDT
- 0 = Software cannot force this bit to a '0'

- Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
- Note 2:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## 15.1 Input Capture Control Registers

TABLE 15-1: INPUT CAPTURE 1-INPUT CAPTURE 5 REGISTER MAP

Virtual Address (BF80..#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
2000	IC1CON <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		0000
2010	IC1BUF	31:16	IC1BUF<31:0>															xxxx
		15:0	IC1BUF<31:0>															xxxx
2200	IC2CON <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		0000
2210	IC2BUF	31:16	IC2BUF<31:0>															xxxx
		15:0	IC2BUF<31:0>															xxxx
2400	IC3CON <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		0000
2410	IC3BUF	31:16	IC3BUF<31:0>															xxxx
		15:0	IC3BUF<31:0>															xxxx
2600	IC4CON <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		0000
2610	IC4BUF	31:16	IC4BUF<31:0>															xxxx
		15:0	IC4BUF<31:0>															xxxx
2800	IC5CON <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		0000
2810	IC5BUF	31:16	IC5BUF<31:0>															xxxx
		15:0	IC5BUF<31:0>															xxxx

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 20.0 PARALLEL MASTER PORT (PMP)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

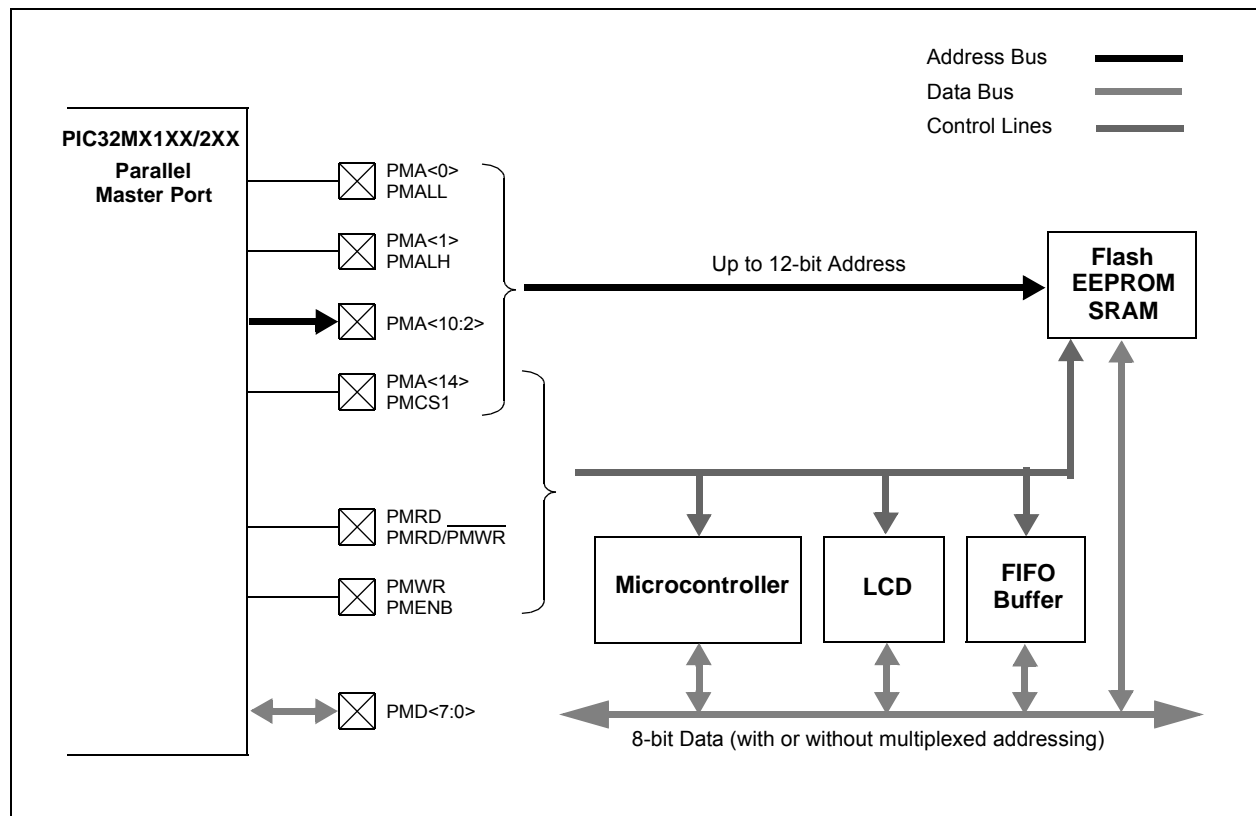
The PMP is a parallel 8-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- Fully multiplexed address/data mode
- Demultiplexed or partially multiplexed address/data mode
  - up to 11 address lines with single Chip Select
  - up to 12 address lines without Chip Select
- One Chip Select line
- Programmable strobe options
  - Individual read and write strobes or;
  - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Legacy parallel slave port support
- Enhanced parallel slave support
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Selectable input voltage levels

Figure 20-1 illustrates the PMP module block diagram.

**FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON <sup>(1)</sup>	COE	CPOL <sup>(2)</sup>	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit<sup>(1)</sup>

1 = Module is enabled. Setting this bit does not affect the other bits in this register

0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is driven on the output CxOUT pin

0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit<sup>(2)</sup>

1 = Output is inverted

0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit

1 = Output of the Comparator is a '1'

0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits

11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output

10 = Comparator interrupt is generated on a high-to-low transition of the comparator output

01 = Comparator interrupt is generated on a low-to-high transition of the comparator output

00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit

1 = Comparator non-inverting input is connected to the internal CVREF

0 = Comparator non-inverting input is connected to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator

11 = Comparator inverting input is connected to the IVREF

10 = Comparator inverting input is connected to the CxIND pin

01 = Comparator inverting input is connected to the CxINC pin

00 = Comparator inverting input is connected to the CxINB pin

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
	—	—	—	—	—	—	FWDTWINSZ<1:0>	
23:16	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

<b>Legend:</b>	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits

11 = Window size is 25%  
 10 = Window size is 37.5%  
 01 = Window size is 50%  
 00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit

1 = Watchdog Timer is enabled and cannot be disabled by software  
 0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit

1 = Watchdog Timer is in non-Window mode  
 0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576  
 10011 = 1:524288  
 10010 = 1:262144  
 10001 = 1:131072  
 10000 = 1:65536  
 01111 = 1:32768  
 01110 = 1:16384  
 01101 = 1:8192  
 01100 = 1:4096  
 01011 = 1:2048  
 01010 = 1:1024  
 01001 = 1:512  
 01000 = 1:256  
 00111 = 1:128  
 00110 = 1:64  
 00101 = 1:32  
 00100 = 1:16  
 00011 = 1:8  
 00010 = 1:4  
 00001 = 1:2  
 00000 = 1:1  
 All other combinations not shown result in operation = 10100

**Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp	
Parameter No.	Typical <sup>(3)</sup>	Max.	Units	Conditions
<b>Operating Current (IDD) (Notes 1, 2, 5)</b>				
DC20	2	3	mA	4 MHz ( <b>Note 4</b> )
DC21	7	10.5	mA	10 MHz
DC22	10	15	mA	20 MHz ( <b>Note 4</b> )
DC23	15	23	mA	30 MHz ( <b>Note 4</b> )
DC24	20	30	mA	40 MHz
DC25	100	150	μA	+25°C, 3.3V LPRC (31 kHz) ( <b>Note 4</b> )

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** This parameter is characterized, but not tested in manufacturing.

**5:** IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-6: DC CHARACTERISTICS: IDLE CURRENT (I<sub>IDLE</sub>)**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Parameter No.	Typical <sup>(2)</sup>	Max.	Units	Conditions		
Idle Current (IDLE): Core Off, Clock on Base Current (Notes 1, 4)						
DC30a	1	1.5	mA	4 MHz (Note 3)		
DC31a	2	3	mA	10 MHz		
DC32a	4	6	mA	20 MHz (Note 3)		
DC33a	5.5	8	mA	30 MHz (Note 3)		
DC34a	7.5	11	mA	40 MHz		
DC37a	100	—	μA	-40°C	3.3V	LPRC (31 kHz) (Note 3)
DC37b	250	—	μA	+25°C		
DC37c	380	—	μA	+85°C		

**Note 1:** The test conditions for I<sub>IDLE</sub> current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
  - OSC2/CLKO is configured as an I/O input pin
  - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
  - CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
  - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
  - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
  - All I/O pins are configured as inputs and pulled to V<sub>SS</sub>
  - MCLR = V<sub>DD</sub>
  - RTCC and JTAG are disabled
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** This parameter is characterized, but not tested in manufacturing.
- 4:** I<sub>IDLE</sub> electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-9: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS**

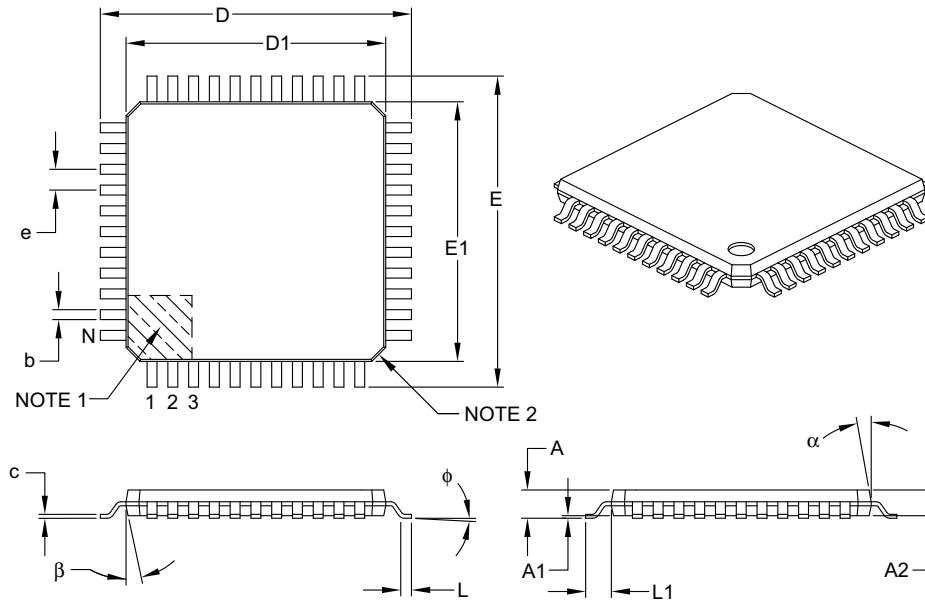
DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typ. <sup>(1)</sup>	Max.	Units	Conditions
DI60a	I <sub>ICL</sub>	Input Low Injection Current	0	—	-5 <sup>(2,5)</sup>	mA	This parameter applies to all pins, with the exception of the power pins.
DI60b	I <sub>ICH</sub>	Input High Injection Current	0	—	+5 <sup>(3,4,5)</sup>	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, and the SOSCI, SOSCO, OSC1, D+, and D- pins.
DI60c	ΣI <sub>ICT</sub>	Total Input Injection Current (sum of all I/O and Control pins)	-20 <sup>(6)</sup>	—	+20 <sup>(6)</sup>	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (   I <sub>ICL</sub> +   I <sub>ICH</sub>   ) ≤ ΣI <sub>ICT</sub> )

- Note 1:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** V<sub>IL</sub> source < (V<sub>SS</sub> - 0.3). Characterized but not tested.
- 3:** V<sub>IH</sub> source > (V<sub>DD</sub> + 0.3) for non-5V tolerant pins only.
- 4:** Digital 5V tolerant pins do not have an internal high side diode to V<sub>DD</sub>, and therefore, cannot tolerate any “positive” input injection current.
- 5:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., V<sub>IH</sub> Source > (V<sub>DD</sub> + 0.3) or V<sub>IL</sub> source < (V<sub>SS</sub> - 0.3)).
- 6:** Any number and/or combination of I/O pins not excluded under I<sub>ICL</sub> or I<sub>ICH</sub> conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, I<sub>ICL</sub> = (((V<sub>SS</sub> - 0.3) - V<sub>IL</sub> source) / R<sub>S</sub>). If **Note 3**, I<sub>ICH</sub> = ((I<sub>ICH</sub> source - (V<sub>DD</sub> + 0.3)) / R<sub>S</sub>). R<sub>S</sub> = Resistance between input source voltage and device pin. If (V<sub>SS</sub> - 0.3) ≤ V<sub>SOURCE</sub> ≤ (V<sub>DD</sub> + 0.3), injection current = 0.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		44		
Lead Pitch	e		0.80 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	$\phi$		0°	3.5°	7°
Overall Width	E		12.00 BSC		
Overall Length	D		12.00 BSC		
Molded Package Width	E1		10.00 BSC		
Molded Package Length	D1		10.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.30	0.37	0.45
Mold Draft Angle Top	$\alpha$		11°	12°	13°
Mold Draft Angle Bottom	$\beta$		11°	12°	13°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## Revision D (February 2012)

All occurrences of VUSB were changed to: VUSB3V3. In addition, text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

Section	Update Description
“32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog”	Corrected a part number error in all pin diagrams.  Updated the DMA Channels (Programmable/Dedicated) column in the PIC32MX1XX General Purpose Family Features (see Table 1).
<b>1.0 “Device Overview”</b>	Added the TQFP and VTLA packages to the 44-pin column heading and updated the pin numbers for the SCL1, SCL2, SDA1, and SDA2 pins in the Pinout I/O Descriptions (see Table 1-1).
<b>7.0 “Interrupt Controller”</b>	Updated the Note that follows the features.  Updated the Interrupt Controller Block Diagram (see Figure 7-1).
<b>29.0 “Electrical Characteristics”</b>	Updated the Maximum values for parameters DC20-DC24, and the Minimum value for parameter DC21 in the Operating Current (IDD) DC Characteristics (see Table 29-5).  Updated all Minimum and Maximum values for the Idle Current (I <sub>IDLE</sub> ) DC Characteristics (see Table 29-6).  Updated the Maximum values for parameters DC40k, DC40l, DC40n, and DC40m in the Power-down Current (IPD) DC Characteristics (see Table 29-7).  Changed the minimum clock period for SCKx from 40 ns to 50 ns in Note 3 of the SPIx Master and Slave Mode Timing Requirements (see Table 29-26 through Table 29-29).
<b>30.0 “DC and AC Device Characteristics Graphs”</b>	Updated the Typical I <sub>IDLE</sub> Current @ VDD = 3.3V graph (see Figure 30-5).