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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256b-50i-sp

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES

28-PIN QFN (TOP VIEW) ^(1,2,3,4)			
PIC32MX210F016B PIC32MX220F032B PIC32MX230F064B PIC32MX230F256B PIC32MX250F128B PIC32MX270F256B		28	1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	16	VSS
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	17	VCAP
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	18	PGED2/RPB10/D+/CTED11/RB10
5	VSS	19	PGEC2/RPB11/D-/RB11
6	OSC1/CLKI/RPA2/RA2	20	VUSB3V3
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/RB4	22	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	VDD	24	AVSS
11	TMS/RPB5/USBID/RB5	25	AVDD
12	VBUS	26	MCLR
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 13: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

<p>44-PIN VTLA (TOP VIEW)^(1,2,3,5)</p> <p>PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D</p>	
44	1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	V _{SS}	28	V _{DD}
7	V _{CAP}	29	V _{SS}
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AV _{SS}	38	RPC5/PMA3/RC5
17	AV _{DD}	39	V _{SS}
18	$\overline{\text{MCLR}}$	40	V _{DD}
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to V_{SS} externally.
 - 4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.
 - 5: Shaded pins are 5V tolerant.

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Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

TABLE 3-3: MIPS32® M4K® PROCESSOR CORE EXCEPTION TYPES

Exception	Description
Reset	Assertion \overline{MCLR} or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input or by setting the <i>EjtagBrk</i> bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of <i>SDBBP</i> instruction).
Sys	Execution of <i>SYSCALL</i> instruction.
Bp	Execution of <i>BREAK</i> instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a <i>CorExtend</i> instruction when <i>CorExtend</i> is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

3.3 Power Management

The MIPS M4K processor core offers many power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the *WAIT* instruction. For more information on power management, see **Section 26.0 “Power-Saving Features”**.

3.4 EJTAG Debug Support

The MIPS M4K processor core provides an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (*DERET*) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

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REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDUPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDUPBA<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUPBA<15:10>:** DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** Read-Only bits

This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.
2: The value in this register must be less than or equal to BMXDRMSZ.

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NOTES:

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REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<31:24>								
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<23:16>								
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<15:8>								
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMKEY<31:0>**: Unlock Register bits
 These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMADDR<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMADDR<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMADDR<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMADDR<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMADDR<31:0>**: Flash Address bits
 Bulk/Chip/PFM Erase: Address is ignored.
 Page Erase: Address identifies the page to erase.
 Row Program: Address identifies the row to program.
 Word Program: Address identifies the word to program.

6.1 Reset Control Registers

TABLE 6-1: RESET CONTROL REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F600	RCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	xxxx ⁽²⁾
F610	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

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REGISTER 9-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>**: Channel Cell Size bits

1111111111111111 = 65,535 bytes transferred on an event
.
.
.
0000000000000010 = 2 bytes transferred on an event
0000000000000001 = 1 byte transferred on an event
0000000000000000 = 65,536 bytes transferred on an event

REGISTER 9-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<15:0>**: Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
.
.
.
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

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REGISTER 10-5: U1PWRC: USB POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	—	—	USLPGRD	USBBUSY ⁽¹⁾	—	USUSPEND	USBPWR

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit

- 1 = USB bus activity has been detected; however, an interrupt is pending, which has yet to be generated
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit

- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit⁽¹⁾

- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit

- 1 = USB module is placed in Suspend mode
(The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit

- 1 = USB module is turned on
- 0 = USB module is disabled
(Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

Note 1: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

TABLE 11-4: PORTB REGISTER MAP

Virtual Address (BF88.#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB15	ANSB14	ANSB13	ANSB12 ⁽²⁾	—	—	—	—	—	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0
6110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12 ⁽²⁾	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6 ⁽²⁾	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12 ⁽²⁾	RB11	RB10	RB9	RB8	RB7	RC6 ⁽²⁾	RB5	RB4	RB3	RB2	RB1	RB0	xxxxx
6130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12 ⁽²⁾	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6 ⁽²⁾	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxxx
6140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12 ⁽²⁾	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
6150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12 ⁽²⁾	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6 ⁽²⁾	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
6160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12 ⁽²⁾	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6 ⁽²⁾	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
6170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB15	CNIEB14	CNIEB13	CNIEB11 ⁽²⁾	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6 ⁽²⁾	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
6190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12 ⁽²⁾	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6 ⁽²⁾	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.

2: This bit is not available on PIC32MX2XX devices. The reset value for the TRISB register when this bit is not available is 0x0000EFBF.

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REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit
 When TCS = 1:
 1 = External clock input is synchronized
 0 = External clock input is not synchronized
 When TCS = 0:
 This bit is ignored.
- bit 1 **TCS:** Timer Clock Source Select bit
 1 = External clock from TxCKI pin
 0 = Internal peripheral clock
- bit 0 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

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NOTES:

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REGISTER 19-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5 **ABAUD**: Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed
- bit 4 **RXINV**: Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'
- bit 3 **BRGH**: High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1 **PDSEL<1:0>**: Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity
- bit 0 **STSEL**: Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

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REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>**: Alarm Repeat Counter Value bits⁽²⁾

11111111 = Alarm will trigger 256 times

.

.

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
- 2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
- 3:** This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

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REGISTER 24-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON ⁽¹⁾	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	U-0 —	R/W-0 CVROE	R/W-0 CVRR	R/W-0 CVRSS	CVR<3:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-16 **Unimplemented:** Read as '0'
- bit 15 **ON:** Comparator Voltage Reference On bit⁽¹⁾
 - 1 = Module is enabled
 - Setting this bit does not affect other bits in the register.
 - 0 = Module is disabled and does not consume current.
 - Clearing this bit does not affect the other bits in the register.
- bit 14-7 **Unimplemented:** Read as '0'
- bit 6 **CVROE:** CVREFOUT Enable bit
 - 1 = Voltage level is output on CVREFOUT pin
 - 0 = Voltage level is disconnected from CVREFOUT pin
- bit 5 **CVRR:** CVREF Range Selection bit
 - 1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size
 - 0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size
- bit 4 **CVRSS:** CVREF Source Selection bit
 - 1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)
 - 0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS
- bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \leq \text{CVR}<3:0> \leq 15$ bits
 - When CVRR = 1:
 $\text{CVREF} = (\text{CVR}<3:0>/24) \cdot (\text{CVRSRC})$
 - When CVRR = 0:
 $\text{CVREF} = 1/4 \cdot (\text{CVRSRC}) + (\text{CVR}<3:0>/32) \cdot (\text{CVRSRC})$

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

TABLE 26-2: PERIPHERAL MODULE DISABLE REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets					
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0						
F240	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000					
		15:0	—	—	—	CVRMD	—	—	—	CTMUMD	—	—	—	—	—	—	—	—	AD1MD	0000				
F250	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000					
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD	0000		
F260	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000					
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
F270	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000					
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	T5MD	T4MD	T3MD	T2MD	T1MD	0000
F280	PMD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000					
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	USB1MD	—	—	—	I2C1MD	I2C1MD
F290	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000					
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPI2MD	SPI1MD	—	—	—	U2MD
F290	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000					
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PMPMD
																			REFOMD	RTCCMD	0000			

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.

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TABLE 30-34: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	Vss	—	AVDD	V	(Note 1)
Reference Inputs							
AD05 AD05a	VREFH	Reference Voltage High	AVSS + 2.0 2.5	— —	AVDD 3.6	V V	(Note 1) VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08 AD08a	IREF	Current Drain	— —	250 —	400 3	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15	—	Leakage Current	—	± 0.001	± 0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 k Ω
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5k	Ω	(Note 1)
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	E _{OFF}	Offset Error	> -1	—	< 1	Lsb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at $V_{BORMIN} < V_{DD} < 2.5\text{V}$, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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Revision G (April 2015)

This revision includes the addition of the following devices:

- PIC32MX130F256B
- PIC32MX230F256B
- PIC32MX130F256D
- PIC32MX230F256D

The title of the document was updated to avoid confusion with the PIC32MX1XX/2XX/5XX 64/100-pin Family data sheet.

All peripheral SFR maps have been relocated from the Memory chapter to their respective peripheral chapters.

In addition, this revision includes the following major changes as described in Table A-6, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-6: MAJOR SECTION UPDATES

Section	Update Description
32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog	Added new devices to the family features (see Table 1 and Table 2). Updated pin diagrams to include new devices (see Pin Diagrams).
2.0 “Guidelines for Getting Started with 32-bit MCUs”	Updated these sections: 2.2 “Decoupling Capacitors” , 2.3 “Capacitor on Internal Voltage Regulator (VCAP)” , 2.4 “Master Clear (MCLR) Pin” , 2.8.1 “Crystal Oscillator Design Consideration”
4.0 “Memory Organization”	Added Memory Map for new devices (see Figure 4-6).
14.0 “Watchdog Timer (WDT)”	New chapter created from content previously located in the Special Features chapter.
30.0 “Electrical Characteristics”	Removed parameter D312 (TSET) from the Comparator Specifications (see Table 30-12). Added the Comparator Voltage Reference Specifications (see Table 30-13). Updated Table 30-12.

Revision H (July 2015)

This revision includes the following major changes as described in Table A-7, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-7: MAJOR SECTION UPDATES

Section	Update Description
2.0 “Guidelines for Getting Started with 32-bit MCUs”	Section 2.9 “Sosc Design Recommendation” was removed.
8.0 “Oscillator Configuration”	The Primary Oscillator (Posc) logic in the Oscillator diagram was updated (see Figure 8-1).
30.0 “Electrical Characteristics”	The Power-Down Current (IPD) DC Characteristics parameter DC40k was updated (see Table 30-7). Table 30-9: “DC Characteristics: I/O Pin Input Injection current Specifications” was added.

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(64 KB RAM, 256 KB Flash)	42	DCHxSPTR (DMA Channel 'x' Source Pointer).....	99
Memory Organization.....	37	DCHxSSA (DMA Channel 'x' Source Start Address)..	97
Microchip Internet Web Site	341	DCHxSSIZ (DMA Channel 'x' Source Size).....	98
MPLAB ASM30 Assembler, Linker, Librarian	254	DCRCCON (DMA CRC Control).....	90
MPLAB Integrated Development Environment Software ..	253	DCRCDATA (DMA CRC Data).....	92
MPLAB PM3 Device Programmer.....	255	DCRCXOR (DMA CRCXOR Enable)	92
MPLAB REAL ICE In-Circuit Emulator System.....	255	DEVCFG0 (Device Configuration Word 0)	241
MPLINK Object Linker/MPLIB Object Librarian	254	DEVCFG1 (Device Configuration Word 1)	243
O		DEVCFG2 (Device Configuration Word 2)	245
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P		DMAADDR (DMA Address).....	89
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AD1CON1 (ADC Control 1)	213	OSCTUN (FRC Tuning).....	79
AD1CON2 (ADC Control 2)	215	PMADDR (Parallel Port Address).....	195
AD1CON3 (ADC Control 3)	216	PMAEN (Parallel Port Pin Enable).....	196
AD1CSSL (ADC Input Scan Select)	218	PMCON (Parallel Port Control).....	191
ALRMDATE (Alarm Date Value)	208	PMMODE (Parallel Port Mode).....	193
ALRMTIME (Alarm Time Value)	207	PMSTAT (Parallel Port Status (Slave Modes Only)..	197
BMXBOOTSZ (Boot Flash (IFM) Size)	51	REFOCON (Reference Oscillator Control)	80
BMXCON (Bus Matrix Configuration)	46	REFOTRIM (Reference Oscillator Trim).....	82
BMXDKPBA (Data RAM Kernel Program		RFPnR (Peripheral Pin Select Output)	141
Base Address)	47	RSWRST (Software Reset).....	62
BMXDRMSZ (Data RAM Size Register).....	50	RTCALRM (RTC Alarm Control).....	203
BMXDUDBA (Data RAM User Data Base Address) ...	48	RTCCON (RTC Control).....	201
BMXDUPBA (Data RAM User Program		RTCDATE (RTC Date Value)	206
Base Address)	49	RTCTIME (RTC Time Value).....	205
BMXPFMSZ (Program Flash (PFM) Size)	51	SPIxCON (SPI Control)	167
BMXPUPBA (Program Flash (PFM) User Program		SPIxCON2 (SPI Control 2)	170
Base Address)	50	SPIxSTAT (SPI Status).....	171
CFGCON (Configuration Control)	248	T1CON (Type A Timer Control).....	145
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DCHxCSIZ (DMA Channel 'x' Cell-Size).....	100	U1EIE (USB Error Interrupt Enable).....	117
DCHxDAT (DMA Channel 'x' Pattern Data).....	101	U1EIR (USB Error Interrupt Status).....	115
DCHxDPTR (Channel 'x' Destination Pointer)	99	U1EP0-U1EP15 (USB Endpoint Control)	126
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Start Address).....	97	U1FRML (USB Frame Number Low).....	121
DCHxDSIZ (DMA Channel 'x' Destination Size)	98	U1IE (USB Interrupt Enable)	114
DCHxECON (DMA Channel 'x' Event Control)	94	U1IR (USB Interrupt)	113
DCHxINT (DMA Channel 'x' Interrupt Control).....	95	U1OTGCON (USB OTG Control)	111
		U1OTGIE (USB OTG Interrupt Enable).....	109
		U1OTGIR (USB OTG Interrupt Status).....	108