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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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#### Details

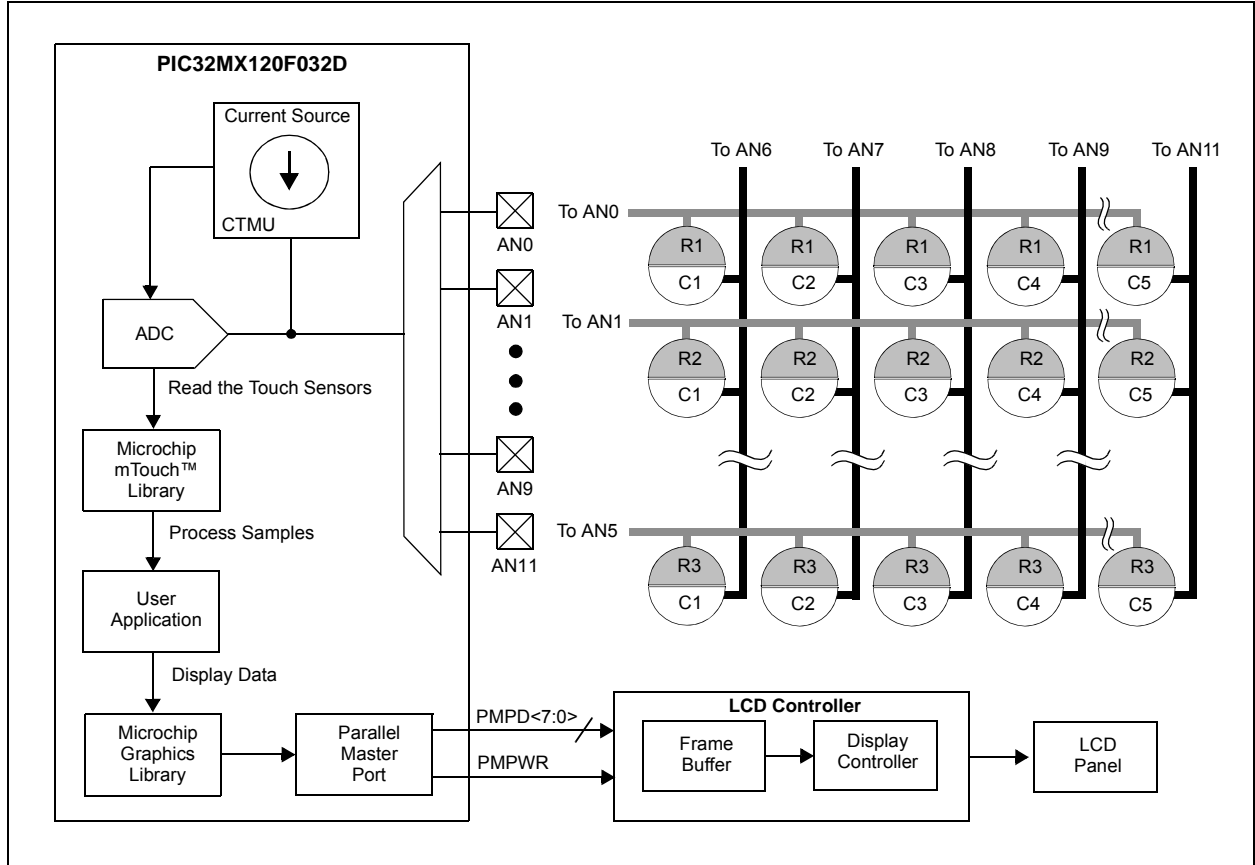
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256b-i-sp">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256b-i-sp</a>

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

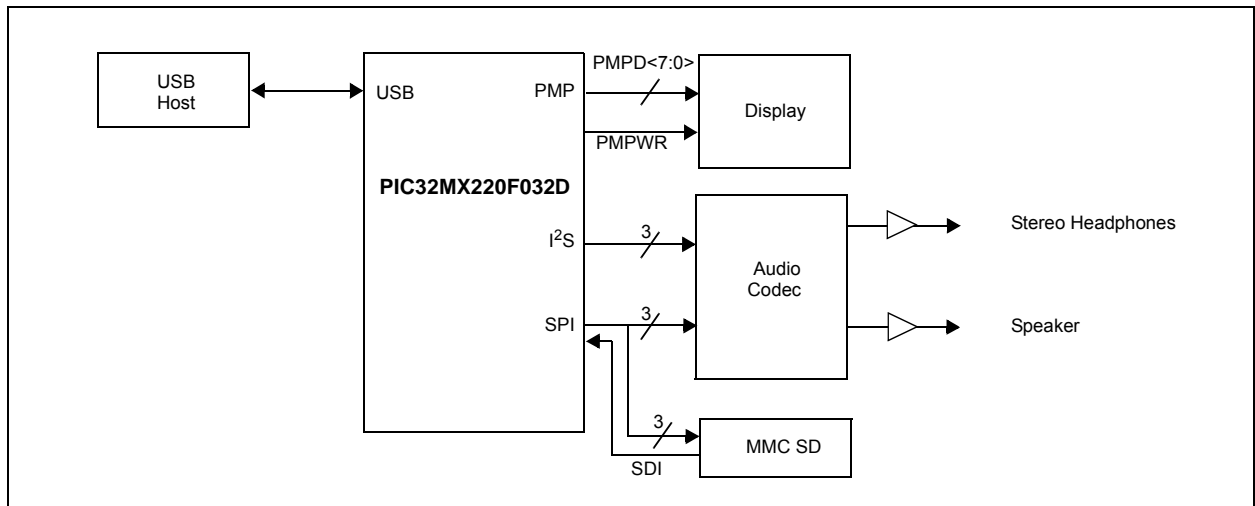
## 2.9 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-5 and Figure 2-6.

**FIGURE 2-5: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION**



**FIGURE 2-6: AUDIO PLAYBACK APPLICATION**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<31:24>								
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<23:16>								
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<15:8>								
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>								

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-0 **NVMKEY<31:0>**: Unlock Register bits  
 These bits are write-only, and read as '0' on any read

**Note:** This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

## REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMADDR<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMADDR<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMADDR<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMADDR<7:0>								

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-0 **NVMADDR<31:0>**: Flash Address bits  
 Bulk/Chip/PFM Erase: Address is ignored.  
 Page Erase: Address identifies the page to erase.  
 Row Program: Address identifies the row to program.  
 Word Program: Address identifies the word to program.

**TABLE 7-2: INTERRUPT REGISTER MAP (CONTINUED)**

Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	Bits														All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2		17/1	16/0
1100	IPC7	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>			—	—	—	USBIP<2:0> <sup>(2)</sup>		USBIS<1:0> <sup>(2)</sup>		0000
		15:0	—	—	—	CMP3IP<2:0>			CMP3IS<1:0>			—	—	—	CMP2IP<2:0>		CMP2IS<1:0>		0000
1110	IPC8	31:16	—	—	—	PMP/IP<2:0>			PMP/IS<1:0>			—	—	—	CNIP<2:0>		CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>			—	—	—	U1IP<2:0>		U1IS<1:0>		0000
1120	IPC9	31:16	—	—	—	CTMUIP<2:0>			CTMUIS<1:0>			—	—	—	I2C2IP<2:0>		I2C2IS<1:0>		0000
		15:0	—	—	—	U2IP<2:0>			U2IS<1:0>			—	—	—	SPI2IP<2:0>		SPI2IS<1:0>		0000
1130	IPC10	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>			—	—	—	DMA2IP<2:0>		DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>			—	—	—	DMA0IP<2:0>		DMA0IS<1:0>		0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.
- 2:** These bits are not available on PIC32MX1XX devices.
- 3:** This register does not have associated CLR, SET, INV registers.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 4     **CHDHIF:** Channel Destination Half Full Interrupt Flag bit  
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)  
0 = No interrupt is pending
- bit 3     **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit  
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs  
0 = No interrupt is pending
- bit 2     **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit  
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)  
0 = No interrupt is pending
- bit 1     **CHTAIF:** Channel Transfer Abort Interrupt Flag bit  
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted  
0 = No interrupt is pending
- bit 0     **CHERIF:** Channel Address Error Interrupt Flag bit  
1 = A channel address error has been detected (either the source or the destination address is invalid)  
0 = No interrupt is pending

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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NOTES:

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1    **PPBRST:** Ping-Pong Buffers Reset bit  
1 = Reset all Even/Odd buffer pointers to the EVEN Buffer Descriptor banks  
0 = Even/Odd buffer pointers are not Reset
- bit 0    **USBEN:** USB Module Enable bit<sup>(4)</sup>  
1 = USB module and supporting circuitry is enabled  
0 = USB module and supporting circuitry is disabled
- SOFEN:** SOF Enable bit<sup>(5)</sup>  
1 = SOF token is sent every 1 ms  
0 = SOF token is disabled

- Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
- 2:** All host control logic is reset any time that the value of this bit is toggled.
- 3:** Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
- 4:** Device mode.
- 5:** Host mode.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 13.0 TIMER2/3, TIMER4/5

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

- Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

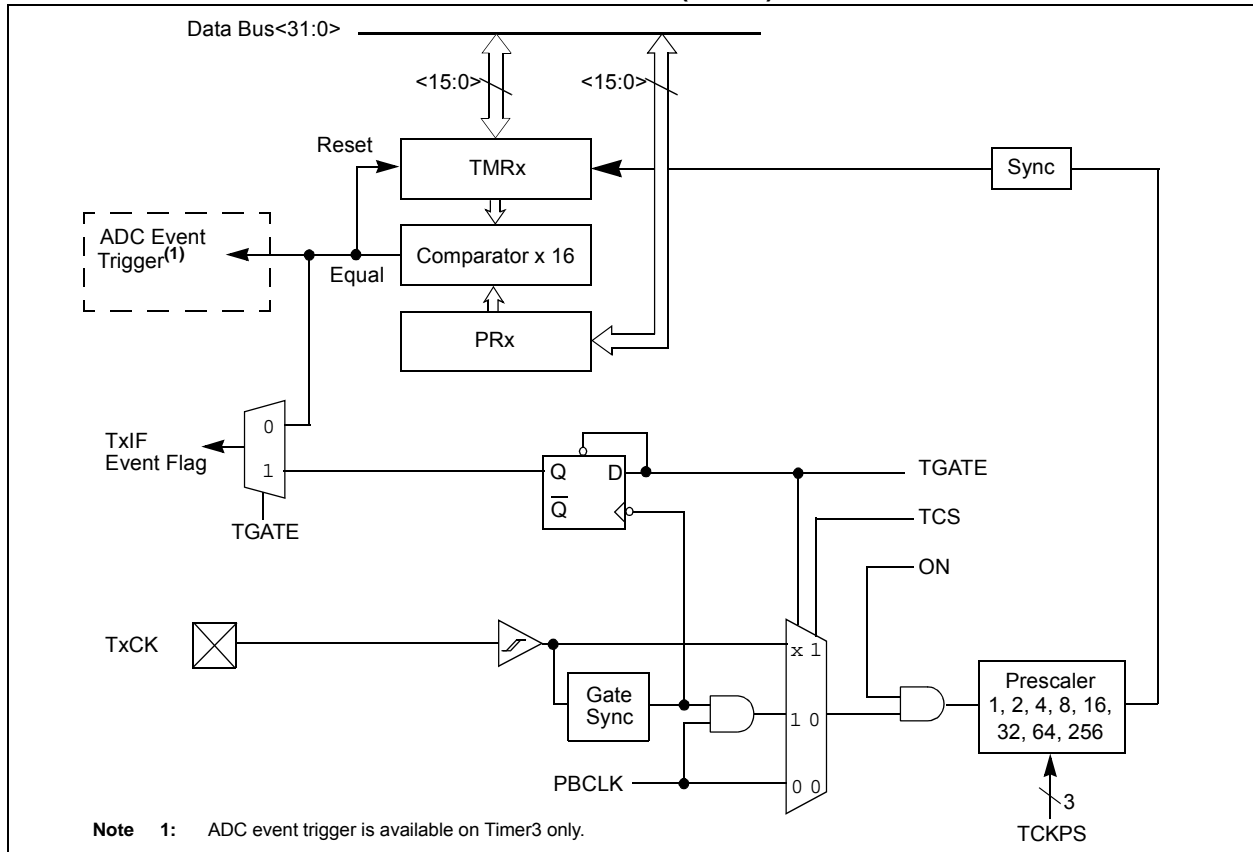
**Note:** In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through Timer5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or Timer4 and 'y' represents Timer3 or Timer5.

### 13.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 in 16-bit mode, Timer2/3 in 32-bit mode)
- Fast bit manipulation using CLR, SET and INV registers

Figure 13-1 and Figure 13-2 illustrate block diagrams of Timer2/3 and Timer4/5.

**FIGURE 13-1: TIMER2-TIMER5 BLOCK DIAGRAM (16-BIT)**





# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

- bit 3      **T32:** 32-Bit Timer Mode Select bit<sup>(2)</sup>  
1 = Odd numbered and even numbered timers form a 32-bit timer  
0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2      **Unimplemented:** Read as '0'
- bit 1      **TCS:** Timer Clock Source Select bit<sup>(3)</sup>  
1 = External clock from TxCK pin  
0 = Internal peripheral clock
- bit 0      **Unimplemented:** Read as '0'

- Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit is available only on even numbered timers (Timer2 and Timer4).
- 3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
- 4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		—	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0> <sup>(1)</sup>		WAITM<3:0> <sup>(1)</sup>			WAITE<1:0> <sup>(1)</sup>		

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)

- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> = 11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits

- 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle<sup>(2)</sup>
- 01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle<sup>(2)</sup>
- 00 = No increment or decrement of address

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits

- 11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)
- 10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)
- 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
- 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits<sup>(1)</sup>

- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits<sup>(1)</sup>

- 1111 = Wait of 16 TPB
- .
- .
- .
- 0001 = Wait of 2 TPB
- 0000 = Wait of 1 TPB (default)

**Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

**2:** Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

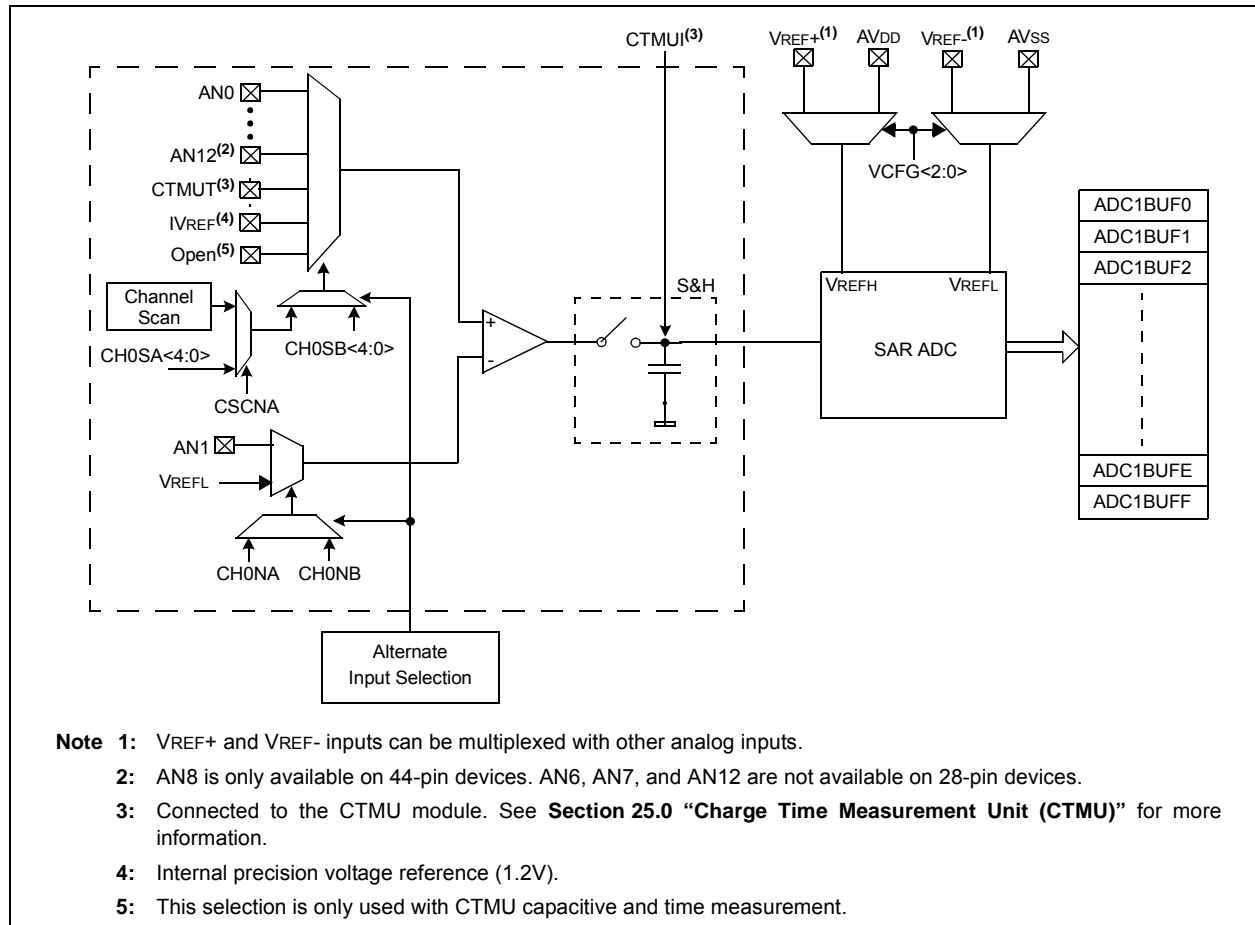
The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed

- Up to 13 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. Figure 22-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

**FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON <sup>(1)</sup>	COE	CPOL <sup>(2)</sup>	—	—	—	—	COU <sup>T</sup>
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 31-16 **Unimplemented:** Read as '0'
- bit 15 **ON:** Comparator ON bit<sup>(1)</sup>
  - 1 = Module is enabled. Setting this bit does not affect the other bits in this register
  - 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register
- bit 14 **COE:** Comparator Output Enable bit
  - 1 = Comparator output is driven on the output CxOUT pin
  - 0 = Comparator output is not driven on the output CxOUT pin
- bit 13 **CPOL:** Comparator Output Inversion bit<sup>(2)</sup>
  - 1 = Output is inverted
  - 0 = Output is not inverted
- bit 12-9 **Unimplemented:** Read as '0'
- bit 8 **COU<sup>T</sup>:** Comparator Output bit
  - 1 = Output of the Comparator is a '1'
  - 0 = Output of the Comparator is a '0'
- bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
  - 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
  - 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
  - 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
  - 00 = Comparator interrupt generation is disabled
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **CREF:** Comparator Positive Input Configure bit
  - 1 = Comparator non-inverting input is connected to the internal CVREF
  - 0 = Comparator non-inverting input is connected to the CxINA pin
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
  - 11 = Comparator inverting input is connected to the IVREF
  - 10 = Comparator inverting input is connected to the CxIND pin
  - 01 = Comparator inverting input is connected to the CxINC pin
  - 00 = Comparator inverting input is connected to the CxINB pin

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

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**REGISTER 23-2: CMSTAT: COMPARATOR STATUS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	C3OUT	C2OUT	C1OUT

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit

- 1 = All Comparator modules are disabled when the device enters Idle mode
- 0 = All Comparator modules continue to operate when the device enters Idle mode

bit 12-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator Output bit

- 1 = Output of Comparator 3 is a '1'
- 0 = Output of Comparator 3 is a '0'

bit 1 **C2OUT:** Comparator Output bit

- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit

- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

## 25.1 CTMU Control Registers

**TABLE 25-1: CTMU REGISTER MAP**

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits														All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2		17/1
A200	CTMUCON	31:16	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>			—	—	0000
		15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	ITRIM<5:0>					IRNG<1:0>		0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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NOTES:

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
	—	—	—	—	—	—	FWDTWINSZ<1:0>	
23:16	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

### Legend:

R = Readable bit

-n = Value at POR

r = Reserved bit

W = Writable bit

'1' = Bit is set

P = Programmable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ<1:0>**: Watchdog Timer Window Size bits

11 = Window size is 25%

10 = Window size is 37.5%

01 = Window size is 50%

00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit

1 = Watchdog Timer is enabled and cannot be disabled by software

0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit

1 = Watchdog Timer is in non-Window mode

0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>**: Watchdog Timer Postscale Select bits

10100 = 1:1048576

10011 = 1:524288

10010 = 1:262144

10001 = 1:131072

10000 = 1:65536

01111 = 1:32768

01110 = 1:16384

01101 = 1:8192

01100 = 1:4096

01011 = 1:2048

01010 = 1:1024

01001 = 1:512

01000 = 1:256

00111 = 1:128

00110 = 1:64

00101 = 1:32

00100 = 1:16

00011 = 1:8

00010 = 1:4

00001 = 1:2

00000 = 1:1

All other combinations not shown result in operation = 10100

**Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)		
			Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp		
Param. No.	Typical <sup>(2)</sup>	Max.	Units	Conditions	
<b>Power-Down Current (IPD) (Notes 1, 5)</b>					
DC40k	44	70	μA	-40°C	Base Power-Down Current
DC40l	44	70	μA	+25°C	
DC40n	168	259	μA	+85°C	
DC40m	335	536	μA	+105°C	
<b>Module Differential Current</b>					
DC41e	5	20	μA	3.6V	Watchdog Timer Current: ΔI <sub>WDT</sub> ( <b>Note 3</b> )
DC42e	23	50	μA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI <sub>RTCC</sub> ( <b>Note 3</b> )
DC43d	1000	1100	μA	3.6V	ADC: ΔI <sub>ADC</sub> ( <b>Notes 3,4</b> )

- Note 1:** The test conditions for IPD current measurements are as follows:
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
  - OSC2/CLKO is configured as an I/O input pin
  - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
  - CPU is in Sleep mode, and SRAM data memory Wait states = 1
  - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
  - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
  - All I/O pins are configured as inputs and pulled to V<sub>SS</sub>
  - $\overline{\text{MCLR}} = V_{DD}$
  - RTCC and JTAG are disabled
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS**

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp					
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical	Max.	Units	Conditions
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	3.92	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes
OS51	FSYS	On-Chip VCO System Frequency	60	—	120	MHz	—
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	—
OS53	DCLK	CLKO Stability <sup>(2)</sup> (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**Note 2:** This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 40 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{40}{20}}} = \frac{D_{CLK}}{1.41}$$

**TABLE 30-19: INTERNAL FRC ACCURACY**

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
<b>Internal FRC Accuracy @ 8.00 MHz<sup>(1)</sup></b>						
F20b	FRC	-0.9	—	+0.9	%	—

**Note 1:** Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

**TABLE 30-20: INTERNAL LPRC ACCURACY**

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
<b>LPRC @ 31.25 kHz<sup>(1)</sup></b>						
F21	LPRC	-15	—	+15	%	—

**Note 1:** Change of LPRC frequency as VDD changes.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-35: 10-BIT CONVERSION RATE PARAMETERS**

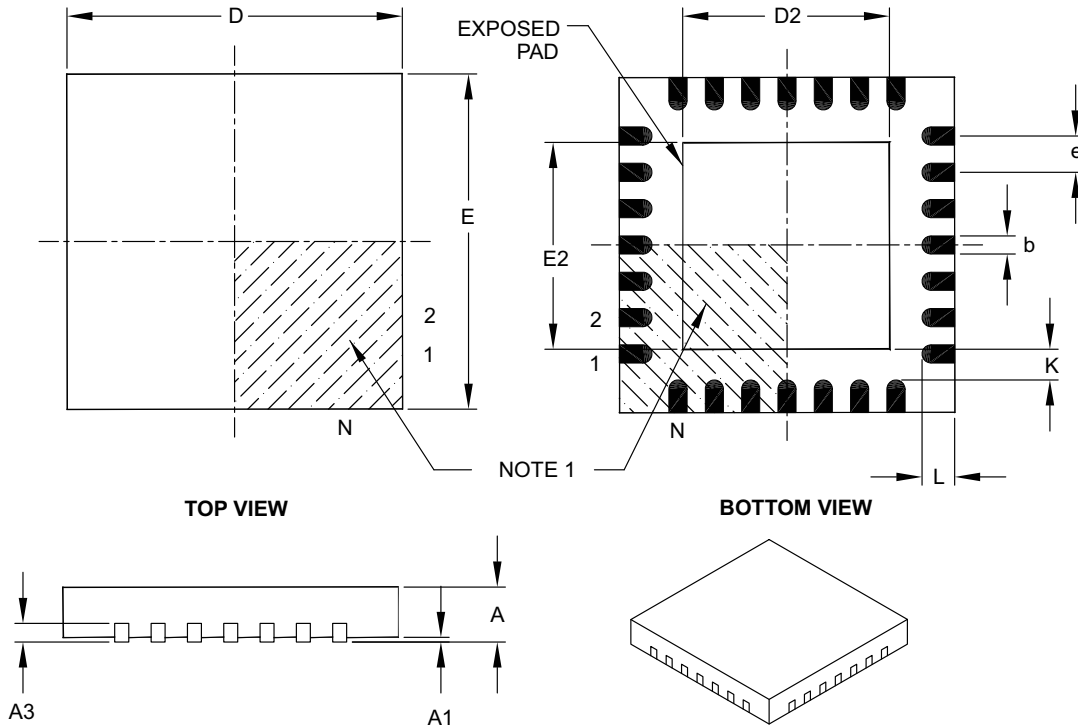
AC CHARACTERISTICS <sup>(2)</sup>			Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp		
ADC Speed	TAD Min.	Sampling Time Min.	Rs Max.	VDD	ADC Channels Configuration
1 Msps to 400 ksps <sup>(1)</sup>	65 ns	132 ns	500Ω	3.0V to 3.6V	
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	

- Note 1:** External VREF- and VREF+ pins must be used for correct operation.
- 2:** These parameters are characterized, but not tested in manufacturing.
- 3:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

Section	Update Description
<b>4.0 “Memory Organization”</b>	<p>Added Memory Maps for the new devices (see Figure 4-3 and Figure 4-4).</p> <p>Removed the BMXCHEDMA bit from the Bus Matrix Register map (see Table 4-1).</p> <p>Added the REFOTRIM register, added the DIVSWEN bit to the REFOCON registers, added Note 4 to the ULOCK and SOSSEN bits and added the PBDIVRDY bit in the OSCCON register in the in the System Control Register map (see Table 4-16).</p> <p>Removed the ALTI2C1 and ALTI2C2 bits from the DEVCFG3 register and added Note 1 to the UPLEN and UPLLIDIV&lt;2:0&gt; bits of the DEVCFG2 register in the Device Configuration Word Summary (see Table 4-17).</p> <p>Updated Note 1 in the Device and Revision ID Summary (see Table 4-18).</p> <p>Added Note 2 to the PORTA Register map (see Table 4-19).</p> <p>Added the ANSB6 and ANSB12 bits to the ANSELB register in the PORTB Register map (see Table 4-20).</p> <p>Added Notes 2 and 3 to the PORTC Register map (see Table 4-21).</p> <p>Updated all register names in the Peripheral Pin Select Register map (see Table 4-23).</p> <p>Added values in support of new devices (16 KB RAM and 32 KB RAM) in the Data RAM Size register (see Register 4-5).</p> <p>Added values in support of new devices (64 KB Flash and 128 KB Flash) in the Data RAM Size register (see Register 4-5).</p>
<b>8.0 “Oscillator Configuration”</b>	<p>Added Note 5 to the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1).</p> <p>Added the PBDIVRDY bit and Note 2 to the Oscillator Control register (see Register 8-1).</p> <p>Added the DIVSWEN bit and Note 3 to the Reference Oscillator Control register (see Register 8-3).</p> <p>Added the REFOTRIM register (see Register 8-4).</p>
<b>21.0 “10-bit Analog-to-Digital Converter (ADC)”</b>	<p>Updated the ADC1 Module Block Diagram (see Figure 21-1).</p> <p>Updated the Notes in the ADC Input Select register (see Register 21-4).</p>
<b>24.0 “Charge Time Measurement Unit (CTMU)”</b>	<p>Updated the CTMU Block Diagram (see Figure 24-1).</p> <p>Added Note 3 to the CTMU Control register (see Register 24-1)</p>
<b>26.0 “Special Features”</b>	<p>Added Note 1 and the PGEC4/PGED4 pin pair to the ICESSEL&lt;1:0&gt; bits in DEVCFG0: Device Configuration Word 0 (see Register 26-1).</p> <p>Removed the ALTI2C1 and ALTI2C2 bits from the Device Configuration Word 3 register (see Register 26-4).</p> <p>Removed 26.3.3 “Power-up Requirements”.</p> <p>Added Note 3 to the Connections for the On-Chip Regulator diagram (see Figure 26-2).</p> <p>Updated the Block Diagram of Programming, Debugging and Trace Ports diagram (see Figure 26-3).</p>