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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256bt-50i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 9: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

44-PIN QFN (TOP VIEW)^(1,2,3,5)

PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	Vdd
7	VCAP	29	Vss
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVDD	39	Vss
18	MCLR	40	Vdd
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

44

1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

5: Shaded pins are 5V tolerant.

	-		-	-				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	_	—	_	—	—	_	_	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
10.0	_	_	_	—	—	—	_	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
7:0	_	_	_	_	_	_	_	SWRST ⁽¹⁾

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Legend:	HC = Cleared by hardwar	re	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 Unimplemented: Read as '0'

- bit 0 SWRST: Software Reset Trigger bit⁽¹⁾ 1 = Enable Software Reset event
 - 0 = No effect
- Note 1: The system unlock sequence must be performed before the SWRST bit is written. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

	-								
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	R/W-y	R/W-y	R/W-y	R/W-0	R/W-0	R/W-1	
31:24	—	—	P	LLODIV<2:0	>	FRCDIV<2:0>			
00.40	U-0	R-0	R-1	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	
23:10	—	SOSCRDY	PBDIVRDY	PBDI\	/<1:0>	P	LLMULT<2:0>	>	
45.0	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y	
15:8	—		COSC<2:0>		—	NOSC<2:0>			
7.0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-y	R/W-0	
7:0	CLKLOCK	ULOCK ⁽¹⁾	SLOCK	SLPEN	CF	UFRCEN ⁽¹⁾	SOSCEN	OSWEN	

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Legend: y = Value set from Configuration bits on POR								
R = Readable bit	W = Writable bit	V = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 26-24 FRCDIV<2:0>: Internal Fast RC (FRC) Oscillator Clock Divider bits

- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2 (default setting)
- 000 = FRC divided by 1
- bit 23 Unimplemented: Read as '0'
- bit 22 SOSCRDY: Secondary Oscillator (Sosc) Ready Indicator bit
 - 1 = The Secondary Oscillator is running and is stable
 - 0 = The Secondary Oscillator is still warming up or is turned off
- bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit
 - 1 = PBDIV<1:0> bits can be written
 - 0 = PBDIV<1:0> bits cannot be written
- bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits
 - 11 = PBCLK is SYSCLK divided by 8 (default)
 - 10 = PBCLK is SYSCLK divided by 4
 - 01 = PBCLK is SYSCLK divided by 2
 - 00 = PBCLK is SYSCLK divided by 1

Note 1: This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

10.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 27. "USB On-The-Go (OTG)" (DS60001126), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 Full-Speed and Low-Speed embedded host, Full-Speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 10-1.

The clock generator provides the 48 MHz clock required for USB Full-Speed and Low-Speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module. The PIC32 USB module includes the following features:

- · USB Full-Speed support for Host and Device
- Low-Speed Host support
- USB OTG support
- · Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- · Transaction handshaking performed by hardware
- · Endpoint buffering anywhere in system RAM
- · Integrated DMA to access system RAM and Flash
- Note: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc., also referred to as USB-IF (www.usb.org). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
15.6	ON ⁽¹⁾	—	SIDL	TWDIS	TWIP	—	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
7.0	TGATE		TCKP	S<1:0>		TSYNC	TCS	_

REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Timer On bit⁽¹⁾
 - 1 = Timer is enabled
 - 0 = Timer is disabled

bit 14 Unimplemented: Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit

- 1 = Writes to Timer1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:

- 1 = Asynchronous write to the Timer1 register in progress
- 0 = Asynchronous write to Timer1 register is complete
- In Synchronous Timer mode:

This bit is read as '0'.

- bit 10-8 **Unimplemented:** Read as '0'
- bit 7 TGATE: Timer Gated Time Accumulation Enable bit
 - When TCS = 1:

This bit is ignored.

When TCS = 0:

- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 Unimplemented: Read as '0'

bit 5-4 TCKPS<1:0>: Timer Input Clock Prescale Select bits

- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value
- **Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

13.2 Timer Control Registers

TABLE 13-1: TIMER2-TIMER5 REGISTER MAP

ess										Bi	its								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	TOCON	31:16	_	_			—	—	_	—	—	_	_		_		—	—	0000
0800	12001	15:0	ON	—	SIDL		_				TGATE	-	TCKPS<2:0	>	T32	_	TCS	_	0000
0010		31:16	—	_	_	_	_	_	-		_	_	_	_	_	_	_	_	0000
0810	TIVIRZ	15:0								TMR2	<15:0>								0000
0000	002	31:16	_	_	_	_	-	_	_	_	—	_	-	_	-	_	_	_	0000
0820	PR2	15:0								PR2<	15:0>								FFFF
0.4.00	TACON	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_		0000
0A00	13CON	15:0	ON	_	SIDL		_	_	_	_	TGATE	-	TCKPS<2:0	>	_	_	TCS	_	0000
0.440		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
UATU	TMR3	15:0								TMR3	<15:0>								0000
0.4.00	000	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_		0000
0A20	PR3	15:0								PR3<	15:0>								FFFF
0000	TACON	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_		0000
0000	14CON	15:0	ON	_	SIDL		_	_	_	_	TGATE	-	TCKPS<2:0	>	T32	_	TCS	_	0000
0040		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0010	TMR4	15:0					•			TMR4	<15:0>								0000
0000	004	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_		0000
0020	PR4	15:0					•			PR4<	15:0>								FFFF
0500	TEOON	31:16	—	_	_		_	—	_	_	—	_	_	_	_	_		_	0000
0E00	15CON	15:0	ON	_	SIDL	_	_	_	_	_	TGATE	-	TCKPS<2:0	>	_	_	TCS	—	0000
0540	TMDC	31:16	—	_	_	_	_	_	_	_	_	_	—	—	_	_	—	—	0000
0E10	IMR5	15:0								TMR5	<15:0>								0000
0500	005	31:16	—	—	_		_	_	—	—	_	—	_	—	_	_	—	—	0000
0E20	PK5	15:0								PR5<	15:0>								FFFF

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

15.1 **Input Capture Control Registers**

AB	LE 15-1:	IN	PUT CA	PTURE	E 1-INPU		URE 5	REGIST	ER MA	2							
ess		â								Bi	ts						
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1
2000		31:16				—	—	_	—						—	—	—
2000	IC ICON.	15:0	ON		SIDL	_	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2010	IC1BUF	31:16 15:0		IC1BUF<31:0>													
2200		31:16	_	_	_	—	—	_	—	—	_	_	-	_	—	—	_
2200	1020011	15:0	ON		SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2210	IC2BUF	31:16 15:0	IC2BUF<31:0>														
2400		31:16	—	—	_	_	_	_	_	—	_	—	_	—	_	—	_
2400	IC3CON /	15:0	ON	_	SIDL	—	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2410	IC3BUF	31:16 15:0								IC3BUF	<31:0>						
2600		31:16	_		_	-	-		—	—	_				—	_	_
2000	1040011	15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2610	IC4BUF	31:16 15:0	IC4BUF<31:0>														
2800		31:16	_		_	-	-		—	—	_				—	_	—
2000	1000010	15:0	ON	_	SIDL	—	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2810	IC5BUF	31:16 15:0								IC5BUF	<31:0>						

T

Legend:

This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information. Note 1:

All Resets

0000

0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx

16/0

—

REGISTE	R 18-1:	I2CxCON: I ² C CONTROL REGISTER (CONTINUED)
bit 7	GCEN: Ge	neral Call Enable bit (when operating as I ² C slave)
	1 = Enable (module)	interrupt when a general call address is received in the I2CxRSR e is enabled for reception)
	0 = Genera	al call address is disabled
bit 6	STREN: S	CLx Clock Stretch Enable bit (when operating as I ² C slave)
	Used in co	njunction with SCLREL bit.
	1 = Enable	software or receive clock stretching
b:+ F		$\frac{1}{2}$ solution of the constant of $\frac{1}{2}$ constant of the during sector receives
DILS	ACKDI: A	is transmitted when the software initiates on Asknowledge assumes
	1 = Send a	ACK during an Acknowledge sequence
	0 = Send a	an ACK during an Acknowledge sequence
bit 4	ACKEN: A receive)	cknowledge Sequence Enable bit (when operating as I ² C master, applicable during maste
	1 = Initiate Hardwa 0 = Acknow	Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. are clear at end of master Acknowledge sequence. wledge sequence not in progress
bit 3	RCEN: Re	ceive Enable bit (when operating as I ² C master)
	1 = Enable 0 = Receiv	s Receive mode for I ² C. Hardware clear at end of eighth bit of master receive data byte. re sequence not in progress
bit 2	PEN: Stop	Condition Enable bit (when operating as I ² C master)
	1 = Initiate 0 = Stop co	Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence. ondition not in progress
bit 1	RSEN: Re	peated Start Condition Enable bit (when operating as I ² C master)
	1 = Initiate master	Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of Repeated Start sequence.
	0 = Repeat	ted Start condition not in progress
bit 0	SEN: Start	Condition Enable bit (when operating as I ² C master)
	1 = Initiate 0 = Start co	Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence. ondition not in progress

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0						
31.24	—	—	—	—	—	-	—	_
00.40	U-0	U-0						
23:10	-	—	—	—	—		—	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	F	ORM<2:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
7.0		SSRC<2:0>		CLRASAM		ASAM	SAMP ⁽²⁾	DONE ⁽³⁾

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit⁽¹⁾
 - 1 = ADC module is operating
 - 0 = ADC module is not operating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode

bit 12-11 Unimplemented: Read as '0'

- bit 10-8 **FORM<2:0>:** Data Output Format bits
 - 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
 - 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
 - 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
 - 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
 - 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
 - 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)

 - 000 =Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 4 CLRASAM: Stop Conversion Sequence bit (when the first ADC interrupt is generated)

- 1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
 - 0 = Normal operation, buffer contents will be overwritten by the next conversion sequence
- bit 3 Unimplemented: Read as '0'
- bit 2 **ASAM:** ADC Sample Auto-Start bit

1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.

- 0 = Sampling begins when SAMP bit is set
- bit 1 SAMP: ADC Sample Enable bit⁽²⁾

1 = The ADC sample and hold amplifier is sampling

0 = The ADC sample/hold amplifier is holding

When ASAM = 0, writing '1' to this bit starts sampling.

- When SSRC = 000, writing '0' to this bit will end sampling and start conversion.
- bit 0 DONE: Analog-to-Digital Conversion Status bit⁽³⁾
 1 = Analog-to-digital conversion is done
 0 = Analog-to-digital conversion is not done or has not started Clearing this bit will not affect any operation in progress.
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

24.1 Comparator Voltage Reference Control Register

ess			Bits																
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	CVRCON	31:16	_	—	_	_	_	—	_	_	_	—	-	_	-	—	—	_	0000
9000	CVRCON	15:0	ON	_		_	_	_	_	_	_	CVROE	CVRR	CVRSS		CVR<	3:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

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26.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid. To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 26-1 for more information.

Note: Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TARI E 26-1·	PERIPHERAL MODULE DISABLE BITS AND LOCATIONS
TADLL 20-1.	FERIFILICAL MODULE DISABLE DITS AND LOCATIONS

Peripheral ⁽¹⁾	PMDx bit Name ⁽¹⁾	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
СТМU	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Comparator 3	CMP3MD	PMD2<2>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
I2C1	I2C1MD	PMD5<16>
12C2	I2C2MD	PMD5<17>
USB ⁽²⁾	USBMD	PMD5<24>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

Note 1: Not all modules and associated PMDx bits are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

2: The module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	
31:24	—	—	—	—	—	—	—	—	
00.40	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P	
23:10	—	—	—	—	—	FPLLODIV<2:0>			
45.0	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P	
15:8	UPLLEN ⁽¹⁾	—	—	_	_	UPLLIDIV<2:0> ⁽¹⁾			
7:0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P	
	_	F	PLLMUL<2:0>	•	_	FPLLIDIV<2:0>			

DEVCFG2: DEVICE CONFIGURATION WORD 2 REGISTER 27-3:

Legend:	r = Reserved bit P = Programmable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-19 Reserved: Write '1'

bit 15

bit 7

bit 18-16 FPLLODIV<2:0>: Default PLL Output Divisor bits

- 111 = PLL output divided by 256 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2 000 = PLL output divided by 1 UPLLEN: USB PLL Enable bit⁽¹⁾ 1 = Disable and bypass USB PLL 0 = Enable USB PLL bit 14-11 Reserved: Write '1' bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits⁽¹⁾ 111 = 12x divider 110 = 10x divider 101 = 6x divider100 = 5x divider 011 = 4x divider 010 = 3x divider 010 = 3x divider 001 = 2x divider000 = 1x divider Reserved: Write '1'
- bit 6-4 FPLLMUL<2:0>: PLL Multiplier bits
 - 111 = 24x multiplier 110 = 21x multiplier
 - 101 = 20x multiplier
 - 100 = 19x multiplier
 - 011 = 18x multiplier
 - 010 = 17x multiplier
 - 001 = 16x multiplier
 - 000 = 15x multiplier
- bit 3 Reserved: Write '1'

Note 1: This bit is only available on PIC32MX2XX devices.

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 4): 2.3V to 3.6 (unless otherwise stated) \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments	
D300	VIOFF	Input Offset Voltage	-	±7.5	±25	mV	AVDD = VDD, AVSS = VSS	
D301	VICM	Input Common Mode Voltage	0	_	Vdd	V	AVDD = VDD, AVss = Vss (Note 2)	
D302	CMRR	Common Mode Rejection Ratio	55	—	_	dB	Max VICM = (VDD - 1)V (Note 2)	
D303A	TRESP	Large Signal Response Time	—	150	400	ns	AVDD = VDD, AVSS = VSS (Note 1,2)	
D303B	TSRESP	Small Signal Response Time	-	1	_	μs	This is defined as an input step of 50 mV with 15 mV of overdrive (Note 2)	
D304	ON2ov	Comparator Enabled to Output Valid	-		10	μS	Comparator module is configured before setting the comparator ON bit (Note 2)	
D305	IVREF	Internal Voltage Reference	1.14	1.2	1.26	V	—	
D312	TSET	Internal Comparator Voltage DRC Reference Setting time			10	μs	(Note 3)	

TABLE 30-13: COMPARATOR SPECIFICATIONS

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from Vss to VDD.

2: These parameters are characterized but not tested.

3: Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

4: The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.







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AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions	
PM1	Tlat	PMALL/PMALH Pulse Width	_	1 Трв		—	_	
PM2	Tadsu	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 Трв	_	—	_	
PM3	Tadhold	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 Трв	_	_	_	
PM4	Tahold	PMRD Inactive to Address Out Invalid (address hold time)	5	_	_	ns	_	
PM5	Trd	PMRD Pulse Width	_	1 Трв	_		—	
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	_	ns	_	
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	_	ns		

TABLE 30-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

Note 1: These parameters are characterized, but not tested in manufacturing.





31.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX 28/36/44-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 30.0** "Electrical Characteristics", with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "M", which denotes 50 MHz operation. For example, parameter DC29a in **Section 30.0** "**Electrical Characteristics**", is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/36/44-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	40°C to +85°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss (Note 3)	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 2.3V$ (Note 3)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 2.3V (Note 3)	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of Vss pin(s)	
Maximum current into VDD pin(s) (Note 2)	
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	
Maximum current sourced by all ports (Note 2)	200 mA

Note 1: Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
- 3: See the "Pin Diagrams" section for the 5V tolerant pins.

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