



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	19
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256bt-50i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Pin Diagrams

TABLE 3: **PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES**

28	-PIN SOIC, SPDIP, SSOP (TOP VIEW) ^{(1,2,3})							
	1 SSOF	2	28	1 SC	DIC	28	1 S	PDIP	28
	PIC32MX110F016B PIC32MX120F032B PIC32MX130F064B PIC32MX130F256B PIC32MX150F128B PIC32MX170F256B								
Pin #	Full Pin Name		Pin #			Full Pin	Name		
1	MCLR		15	PGEC3/RPB	6/PMD6/R	RB6			
2	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0		16	TDI/RPB7/C	ED3/PMD	05/INT0/R	B7		
3	VREF-/CVREF-/AN1/RPA1/CTED2/RA1		17	TCK/RPB8/S	CL1/CTE	D10/PMD4	4/RB8		
4	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0		18	TDO/RPB9/S	DA1/CTE	D4/PMD3	/RB9		
5	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1		19	Vss					
6	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2		20	VCAP					
7			24						
	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3		21	PGED2/RPB	10/CTED1	1/PMD2/F	RB10		
8	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss		21	PGED2/RPB PGEC2/TMS	10/CTED1 /RPB11/PI	11/PMD2/F MD1/RB1	RB10 1		
8 9	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2		21 22 23	PGED2/RPB PGEC2/TMS AN12/PMD0/	10/CTED1 /RPB11/PI RB12	11/PMD2/F MD1/RB1 [,]	RB10 1		
8 9 10	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3		21 22 23 24	PGED2/RPB PGEC2/TMS AN12/PMD0/ AN11/RPB13	10/CTED1 /RPB11/Pl RB12 /CTPLS/P	11/PMD2/F MD1/RB1 [,] PMRD/RB1	RB10 1 13		
8 9 10 11	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4		21 22 23 24 25	PGED2/RPB PGEC2/TMS AN12/PMD0/ AN11/RPB13 CVREFOUT/AI	10/CTED1 /RPB11/PI /RB12 /CTPLS/P N10/C3INE	I1/PMD2/F MD1/RB1 MRD/RB1 B/RPB14/S	RB10 1 13 SCK1/CTE	D5/PMW	R/RB14
8 9 10 11 12	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4 SOSCO/RPA4/T1CK/CTED9/PMA1/RA4		21 22 23 24 25 26	PGED2/RPB PGEC2/TMS AN12/PMD0/ AN11/RPB13 CVREFOUT/AI AN9/C3INA/F	10/CTED1 /RPB11/PI RB12 /CTPLS/P N10/C3INE RPB15/SC	I1/PMD2/F MD1/RB1 PMRD/RB1 B/RPB14/S K2/CTED	RB10 1 13 SCK1/CTE 6/PMCS1/	D5/PMW RB15	R/RB14
8 9 10 11 12 13	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4 SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 VDD		21 22 23 24 25 26 27	PGED2/RPB PGEC2/TMS AN12/PMD0/ AN11/RPB13 CVREFOUT/AI AN9/C3INA/F AVSS	10/CTED1 /RPB11/PI RB12 /CTPLS/P N10/C3INE RPB15/SC	I1/PMD2/F MD1/RB1 PMRD/RB1 B/RPB14/S K2/CTED	RB10 1 13 SCK1/CTE 6/PMCS1/	ED5/PMW RB15	R/RB14

1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

Shaded pins are 5V tolerant. 3:

TABLE 4:PIN NAMES FOR 28-PIN USB DEVICES

28	PIN SOIC, SPDIP, SSOP (TOP VIEW) ^(1,2,3)					
	1 SSOP	28	1 SOIC	28	1	28 SPDIP
	PIC32MX210F016B PIC32MX220F032B PIC32MX230F064B PIC32MX230F256B PIC32MX250F128B PIC32MX270F256B					
Pin #	Full Pin Name	Pin #		Full Pin N	Name	
Pin #	Full Pin Name	Pin #	VBUS	Full Pin N	Name	
Pin # 1 2	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	Pin # 15 16	VBUS TDI/RPB7/CTED3/PM	Full Pin N	Name	
Pin # 1 2 3	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	Pin # 15 16 17	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE	Full Pin N D5/INT0/RE	Name 37 /RB8	
Pin # 1 2 3 4	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	Pin # 15 16 17 18	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	Pin # 15 16 17 18 19	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5 6	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	Pin # 15 16 17 18 19 20	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5 6 7	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	Pin # 15 16 17 18 19 20 21	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I FED11/RB10	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INB/C3IND/RPB0/PMD0/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss	Pin # 15 16 17 18 19 20 21 22	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I FED11/RB10 11	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8 9	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2	Pin # 15 16 17 18 19 20 21 22 23	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I FED11/RB10 11	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8 9 10	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3	Pin # 15 16 17 18 19 20 21 22 23 24	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/F	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I TED11/RB10 11 PMRD/RB13	Name 37 /RB8 RB9 0 3	
Pin # 1 2 3 4 5 6 7 8 9 10 11	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4	Pin # 15 16 17 18 19 20 21 22 23 24 25	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/I CVREFOUT/AN10/C3IN	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I FED11/RB10 11 IB/RPB14/V	Name 37 /RB8 RB9 0 3 /BUSON/S	SCK1/CTED5/RB14
Pin # 1 2 3 4 5 6 7 8 9 10 11 12	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INB/C3IND/RPB0/PMD0/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	Pin # 15 16 17 18 19 20 21 22 23 24 25 26	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/f CVREFOUT/AN10/C3IN AN9/C3INA/RPB15/SC	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I TED11/RB10 11 PMRD/RB11 IB/RPB14/V CK2/CTED6	Name 37 /RB8 RB9 0 0 3 /BUSON/S 5/PMCS1	SCK1/CTED5/RB14 1/RB15
Pin # 1 2 3 4 5 6 7 8 9 10 11 12 13	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4 SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 VpD	Pin # 15 16 17 18 19 20 21 22 23 24 25 26 27	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/F CVREFOUT/AN10/C3IN AN9/C3INA/RPB15/SC AVSS	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I TED11/RB10 11 PMRD/RB13 IB/RPB14/V CK2/CTED6	Name 37 /RB8 RB9 0 0 3 /BUSON/S 6)/PMCS1	SCK1/CTED5/RB14 1/RB15

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: Shaded pins are 5V tolerant.

TABLE 5: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES

28-PIN QFN (TOP VIEW)^(1,2,3.4)

PIC32MX110F016B PIC32MX120F032B PIC32MX130F064B PIC32MX130F256B PIC32MX150F128B PIC32MX170F256B

28

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	16	Vss
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	17	VCAP
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	18	PGED2/RPB10/CTED11/PMD2/RB10
5	Vss	19	PGEC2/TMS/RPB11/PMD1/RB11
6	OSC1/CLKI/RPA2/RA2	20	AN12/PMD0/RB12
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/RB4	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	Vdd	24	AVss
11	PGED3/RPB5/PMD7/RB5	25	AVdd
12	PGEC3/RPB6/PMD6/RB6	26	MCLR
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	VREF-/CVREF-/AN1/RPA1/CTED2/RA1
Note	1: The RPn pins can be used by remappable peripherals. See T	able 1 for th	e available peripherals and Section 11.3 "Peripheral Pin

1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: Shaded pins are 5V tolerant.

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). This document contains device-specific information for PIC32MX1XX/2XX 28/36/44-pin Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/36/44-pin Family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.



FIGURE 1-1: BLOCK DIAGRAM

		Pin Nu	mber ⁽¹⁾				
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
OC1	PPS	PPS	PPS	PPS	0	_	Output Compare Output 1
OC2	PPS	PPS	PPS	PPS	0	—	Output Compare Output 2
OC3	PPS	PPS	PPS	PPS	0	—	Output Compare Output 3
OC4	PPS	PPS	PPS	PPS	0	—	Output Compare Output 4
OC5	PPS	PPS	PPS	PPS	0	—	Output Compare Output 5
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault B Input
INT0	13	16	17	43	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4
RA0	27	2	33	19	I/O	ST	PORTA is a bidirectional I/O port
RA1	28	3	34	20	I/O	ST	1
RA2	6	9	7	30	I/O	ST	1
RA3	7	10	8	31	I/O	ST	1
RA4	9	12	10	34	I/O	ST	1
RA7	_	_	_	13	I/O	ST	1
RA8	_	_	_	32	I/O	ST	
RA9	_	_	_	35	I/O	ST	1
RA10	_	_	_	12	I/O	ST	
RB0	1	4	35	21	I/O	ST	PORTB is a bidirectional I/O port
RB1	2	5	36	22	I/O	ST	7
RB2	3	6	1	23	I/O	ST	7
RB3	4	7	2	24	I/O	ST	
RB4	8	11	9	33	I/O	ST	
RB5	11	14	15	41	I/O	ST	
RB6	12 ⁽²⁾	15 (2)	16 (2)	42 ⁽²⁾	I/O	ST	
RB7	13	16	17	43	I/O	ST	
RB8	14	17	18	44	I/O	ST	
RB9	15	18	19	1	I/O	ST	
RB10	18	21	24	8	I/O	ST	
RB11	19	22	25	9	I/O	ST	
RB12	20 ⁽²⁾	23 ⁽²⁾	26 ⁽²⁾	10 ⁽²⁾	I/O	ST	1
RB13	21	24	27	11	I/O	ST	1
RB14	22	25	28	14	I/O	ST	1
RB15	23	26	29	15	I/O	ST	
Legend:	CMOS = CN	MOS compa	atible input	or output		Analog =	Analog input P = Power
	SI = Schmi	tt Irigger in	put with CN	VIOS levels		O = Outp	out I = Input
Note 1.			lod for rofo	ronco only	See the	"Pin Diag	$m_{\text{rem}} = N/A$

DINOUT I/O DESCRIPTIONS (CONTINUED)

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
23:16	—	—	—	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	-	—	_	—
	U-0	R/W-1	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1
7:0	_	BMX WSDRM	_	_	_	E	3MXARB<2:0	>

REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-21 Unimplemented: Read as '0'

	Ommplemented. Read as 0
bit 20	BMXERRIXI: Enable Bus Error from IXI bit
	 1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus 0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus
bit 19	BMXERRICD: Enable Bus Error from ICD Debug Unit bit
	 1 = Enable bus error exceptions for unmapped address accesses initiated from ICD 0 = Disable bus error exceptions for unmapped address accesses initiated from ICD
bit 18	BMXERRDMA: Bus Error from DMA bit
	 1 = Enable bus error exceptions for unmapped address accesses initiated from DMA 0 = Disable bus error exceptions for unmapped address accesses initiated from DMA
bit 17	BMXERRDS: Bus Error from CPU Data Access bit (disabled in Debug mode)
	 1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access 0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access
bit 16	BMXERRIS: Bus Error from CPU Instruction Access bit (disabled in Debug mode)
	 1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access 0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access
bit 15-7	Unimplemented: Read as '0'
bit 6	BMXWSDRM: CPU Instruction or Data Access from Data RAM Wait State bit
	 1 = Data RAM accesses from CPU have one wait state for address setup 0 = Data RAM accesses from CPU have zero wait states for address setup
bit 5-3	Unimplemented: Read as '0'
bit 2-0	BMXARB<2:0>: Bus Matrix Arbitration Mode bits
	111 = Reserved (using these Configuration modes will produce undefined behavior)
	•
	•
	011 = Reserved (using these Configuration modes will produce undefined behavior)010 = Arbitration Mode 2
	001 = Arbitration Mode 1 (default) 000 = Arbitration Mode 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R	R	R	R	R	R	R	R		
31:24				BMXPFN	1SZ<31:24>					
22:46	R	R	R	R	R	R	R	R		
23.10	BMXPFMSZ<23:16>									
45.0	R	R	R	R	R	R	R	R		
15:8	BMXPFMSZ<15:8>									
7.0	R	R	R	R	R	R	R	R		
7:0				BMXPF	MSZ<7:0>					

REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BMXPFMSZ<31:0>: Program Flash Memory (PFM) Size bits

Static value that indicates the size of the PFM in bytes: 0x00004000 = Device has 16 KB Flash 0x00008000 = Device has 32 KB Flash 0x00010000 = Device has 64 KB Flash 0x00020000 = Device has 128 KB Flash 0x00040000 = Device has 256 KB Flash

REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	R	R	R	R	R	R	R	R		
31:24				BMXBOO	TSZ<31:24>					
22.16	R	R	R	R	R	R	R	R		
23.10	BMXBOOTSZ<23:16>									
45.0	R	R	R	R	R	R	R	R		
15:8	BMXBOOTSZ<15:8>									
	R	R	R	R	R	R	R	R		
7:0		BMXBOOTSZ<7:0>								

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits Static value that indicates the size of the Boot PFM in bytes: 0x00000C00 = Device has 3 KB boot Flash

REGISTE	R 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)
bit 4	CHDHIF: Channel Destination Half Full Interrupt Flag bit
	 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2) 0 = No interrupt is pending
bit 3	CHBCIF: Channel Block Transfer Complete Interrupt Flag bit
	 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs 0 = No interrupt is pending
bit 2	CHCCIF: Channel Cell Transfer Complete Interrupt Flag bit
	1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)0 = No interrupt is pending
bit 1	CHTAIF: Channel Transfer Abort Interrupt Flag bit
	 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted 0 = No interrupt is pending
bit 0	CHERIF: Channel Address Error Interrupt Flag bit
	 1 = A channel address error has been detected (either the source or the destination address is invalid) 0 = No interrupt is pending

DS60001168J-page 96

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	—	—		—	—	—	_	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—		—	—	—	_	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—		—	—	—	_	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R-0	R/WC-0, HS
	STALLE	STALLIF ATTACHIF ⁽¹⁾	RESUMEIF ⁽²⁾	IDLEIF	TONIE(3)	SOFIE		URSTIF ⁽⁵⁾
	UTALLI					0011		DETACHIF ⁽⁶⁾

REGISTER 10-6: U1IR: USB INTERRUPT REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable	bit
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7		STALLIF: STALL Handshake Interrupt bit
	-	1 = In Host mode a STALL handshake was received during the handshake phase of the transaction
	I	In Device mode a STALL handshake was transmitted during the handshake phase of the transaction
	(0 = STALL handshake has not been sent
bit 6		ATTACHIF: Peripheral Attach Interrupt bit ⁽¹⁾
	-	1 = Peripheral attachment was detected by the USB module
	(0 = Peripheral attachment was not detected
bit 5		RESUMEIF: Resume Interrupt bit ⁽²⁾
	-	$1 = K$ -State is observed on the D+ or D- pin for 2.5 μ s
	(0 = K-State is not observed
bit 4	I	IDLEIF: Idle Detect Interrupt bit
	-	1 = Idle condition detected (constant Idle state of 3 ms or more)
L:1 0	-	U = NO IDE CONDITION DELECTED
DIT 3		IRNIF: Token Processing Complete Interrupt Dit ^{ery}
	-	$\Gamma = \Gamma$ recessing of current token not complete.
hit 2	Ċ	SOFIE: SOF Taken Interrunt hit
		1 = SOE token received by the peripheral or the SOE threshold reached by the host
	(0 = SOF token was not received nor threshold reached
bit 1	I	UERRIF: USB Error Condition Interrupt bit ⁽⁴⁾
		1 = Unmasked error condition has occurred
	(0 = Unmasked error condition has not occurred
bit 0	l	URSTIF: USB Reset Interrupt bit (Device mode) ⁽⁵⁾
	-	1 = Valid USB Reset has occurred
	(0 = No USB Reset has occurred
		DETACHIF: USB Detach Interrupt bit (Host mode) ⁽⁶⁾
	-	1 = Peripheral detachment was detected by the USB module
	(0 = Peripheral detachment was not detected
Note	1:	This bit is valid only if the HOSTEN bit is set (see Register 10-11), there is no activity on the USB for
		2.5 μ s, and the current bus state is not SE0.
	2:	When not in Suspend mode, this interrupt should be disabled.
	3:	Clearing this bit will cause the STAT FIFO to advance.
	4:	Only error conditions enabled through the U1FIF register will set this bit
	5:	
	6.	Host mode
	υ.	nost mode.

14.0 WATCHDOG TIMER (WDT)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog, Deadman, and Power-up Timers" (DS60001114), which are available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32). The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- · Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle mode

Figure 14-1 illustrates a block diagram of the WDT and Power-up timer.

FIGURE 14-1: WATCHDOG TIMER AND POWER-UP TIMER BLOCK DIAGRAM



REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED) bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bit 11 = Reserved; do not use 10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters) 01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters) 00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character) bit 5 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect. 0 = Address Detect mode is disabled bit 4 **RIDLE:** Receiver Idle bit (read-only) 1 =Receiver is Idle 0 = Data is being received PERR: Parity Error Status bit (read-only) bit 3 1 = Parity error has been detected for the current character 0 = Parity error has not been detected bit 2 FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character 0 = Framing error has not been detected **OERR:** Receive Buffer Overrun Error Status bit. bit 1 This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state. 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)

- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

PIC32MX1XX/2XX 28/36/44-PIN FAMILY





22.1 **ADC Control Registers**

TABLE 22-1: ADC REGISTER MAP

ess										В	its								
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000		31:16	_	_	_	—	—	—	_	_	—	_	_	_	_	—	—	_	0000
9000	ADICONT	15:0	ON	_	SIDL	—	_		FORM<2:0	>		SSRC<2:0	>	CLRASAM	_	ASAM	SAMP	DONE	0000
0010	AD1CON2(1)	31:16		—		_	—	—	—	_	—		—	—	—	—	—	—	0000
9010	ADICONZ	15:0		VCFG<2:0>	>	OFFCAL	—	CSCNA	—	—	BUFS	—		SMPI	<3:0>	-	BUFM	ALTS	0000
9020		31:16	—	—	—		—	—	—	—	—	—	—	—	—	—	—	—	0000
0020		15:0	ADRC	—				SAMC<4:0>	>					ADCS	\$<7:0>				0000
9040	AD1CHS(1)	31:16	CH0NB	—	—	—		CH0SI	3<3:0>		CH0NA	—	—	—		CH0S	A<3:0>		0000
00.0		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9050	AD1CSSL ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16							ADC Re:	sult Word 0	(ADC1BUF	0<31:0>)							0000
		15:0									·	,							0000
9080	ADC1BUF1	31:16							ADC Re	sult Word 1	(ADC1BUF	1<31:0>)							0000
		15:0																	0000
9090	ADC1BUF2	31:10							ADC Re	sult Word 2	(ADC1BUF	2<31:0>)							0000
		10.0																	0000
90A0	ADC1BUF3	15.0	ADC Result Word 3 (ADC1BUF3<31:0>)										0000						
		31.16										0000							
90B0	ADC1BUF4	15.0							ADC Re	sult Word 4	(ADC1BUF	4<31:0>)							0000
		31 16																	0000
90C0	ADC1BUF5	15.0							ADC Re	sult Word 5	(ADC1BUF	5<31:0>)							0000
		31:16																	0000
90D0	ADC1BUF6	15:0							ADC Re	sult Word 6	(ADC1BUF	6<31:0>)							0000
		31:16																	0000
90E0	ADC1BUF7	15:0							ADC Re	sult Word 7	(ADC1BUF	7<31:0>)							0000
		31:16																	0000
90F0	ADC1BUF8	15:0							ADC Re	sult Word 8	(ADC1BUF	8<31:0>)							0000
0400		31:16										· · · · · · · · · · · · · · · · · · ·							0000
9100	ADC1BUF9	15:0							ADC Re	suit word 9	(ADC1BUF	9<31:0>)							0000
0110		31:16								ult Mord A		A-21.0>							0000
9110	ADCIBUFA	15:0							ADC Res	Suit Word A	(ADC IBUF	ASJ1:U>)							0000
Lege	end: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.																		

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV registers" for details. Note 1:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
15:8	ON ⁽¹⁾	COE	CPOL ⁽²⁾	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL	_<1:0>	_	CREF	_	_	CCH	<1:0>

REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER

Legend:

5			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Comparator ON bit⁽¹⁾
 - 1 = Module is enabled. Setting this bit does not affect the other bits in this register
 - 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register
- bit 14 **COE:** Comparator Output Enable bit
 - 1 = Comparator output is driven on the output CxOUT pin
 - 0 = Comparator output is not driven on the output CxOUT pin
- bit 13 **CPOL:** Comparator Output Inversion bit⁽²⁾
 - 1 = Output is inverted
 - 0 = Output is not inverted
- bit 12-9 Unimplemented: Read as '0'
- bit 8 **COUT:** Comparator Output bit
 - 1 = Output of the Comparator is a '1'
 - 0 = Output of the Comparator is a '0'
- bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
 - 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
 - 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
 - 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
 - 00 = Comparator interrupt generation is disabled
- bit 5 Unimplemented: Read as '0'
- bit 4 CREF: Comparator Positive Input Configure bit
 - 1 = Comparator non-inverting input is connected to the internal CVREF
 - 0 = Comparator non-inverting input is connected to the CXINA pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Negative Input Select bits for Comparator
 - 11 = Comparator inverting input is connected to the IVREF
 - 10 = Comparator inverting input is connected to the CxIND pin
 - 01 = Comparator inverting input is connected to the CxINC pin
 - 00 = Comparator inverting input is connected to the CxINB pin
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- · MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- · MPLAB X IDE compatibility

33.1 Package Marking Information (Continued)



44-Lead VTLA



44-Lead QFN



44-Lead TQFP



Example



Example



Example



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((a))
		can be found on the outer packaging for this package.
Note:	If the full N line, thus	Aicrochip part number cannot be marked on one line, it is carried over to the next limiting the number of available characters for customer-specific information.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	N		28	-	
Pitch	е		1.27 BSC		
Overall Height	A	-	-	2.65	
Molded Package Thickness	A2	2.05	-	-	
Standoff §	A1	0.10	-	0.30	
Overall Width	E		10.30 BSC		
Molded Package Width	E1	7.50 BSC			
Overall Length	D		17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75	
Foot Length	L	0.40	-	1.27	
Footprint	L1		1.40 REF		
Lead Angle	Θ	0°	-	-	
Foot Angle	φ	0°	-	8°	
Lead Thickness	С	0.18	-	0.33	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	-	15°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section	Update Description				
4.0 "Memory Organization"	Added Memory Maps for the new devices (see Figure 4-3 and Figure 4-4).				
	Removed the BMXCHEDMA bit from the Bus Matrix Register map (see Table 4-1).				
	Added the REFOTRIM register, added the DIVSWEN bit to the REFOCON registers, added Note 4 to the ULOCK and SOSCEN bits and added the PBDIVRDY bit in the OSCCON register in the in the System Control Register map (see Table 4-16).				
	Removed the ALTI2C1 and ALTI2C2 bits from the DEVCFG3 register and added Note 1 to the UPLLEN and UPLLIDIV<2:0> bits of the DEVCFG2 register in the Device Configuration Word Summary (see Table 4-17).				
	Updated Note 1 in the Device and Revision ID Summary (see Table 4-18).				
	Added Note 2 to the PORTA Register map (see Table 4-19).				
	Added the ANSB6 and ANSB12 bits to the ANSELB register in the PORTB Register map (see Table 4-20).				
	Added Notes 2 and 3 to the PORTC Register map (see Table 4-21).				
	Updated all register names in the Peripheral Pin Select Register map (see Table 4-23).				
	Added values in support of new devices (16 KB RAM and 32 KB RAM) in the Data RAM Size register (see Register 4-5).				
	Added values in support of new devices (64 KB Flash and 128 KB Flash) in the Data RAM Size register (see Register 4-5).				
8.0 "Oscillator Configuration"	Added Note 5 to the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1).				
	Added the PBDIVRDY bit and Note 2 to the Oscillator Control register (see Register 8-1).				
	Added the DIVSWEN bit and Note 3 to the Reference Oscillator Control register (see Register 8-3).				
	Added the REFOTRIM register (see Register 8-4).				
21.0 "10-bit Analog-to-Digital	Updated the ADC1 Module Block Diagram (see Figure 21-1).				
Converter (ADC)"	Updated the Notes in the ADC Input Select register (see Register 21-4).				
24.0 "Charge Time Measurement	Updated the CTMU Block Diagram (see Figure 24-1).				
	Added Note 3 to the CTMU Control register (see Register 24-1)				
26.0 "Special Features"	Added Note 1 and the PGEC4/PGED4 pin pair to the ICESEL<1:0> bits in DEVCFG0: Device Configuration Word 0 (see Register 26-1).				
	Removed the ALTI2C1 and ALTI2C2 bits from the Device Configuration Word 3 register (see Register 26-4).				
	Removed 26.3.3 "Power-up Requirements".				
	Added Note 3 to the Connections for the On-Chip Regulator diagram (see Figure 26-2).				
	Updated the Block Diagram of Programming, Debugging and Trace Ports diagram (see Figure 26-3).				

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

(64 KB RAM, 256 KB Flash)	42
Memory Organization	37
Microchip Internet Web Site	341
MPLAB ASM30 Assembler, Linker, Librarian	254
MPLAB Integrated Development Environment Software	253
MPLAB PM3 Device Programmer	255
MPLAB REAL ICE In-Circuit Emulator System	255
MPLINK Object Linker/MPLIB Object Librarian	254

0

Oscillator Configuration	73
Output Compare	161

Ρ

-	
Packaging	
Details	313
Marking	
Parallel Master Port (PMP)	
PIC32 Family USB Interface Diagram	104
Pinout I/O Descriptions (table)	20
Power-on Reset (POR)	
and On-Chip Voltage Regulator	
Power-Saving Features	
CPU Halted Methods	233
Operation	
with CPU Running	
-	

R

Real-Time Clock and Calendar (RTCC)	199
Register Maps	5–??
Registers	
[pin name]R (Peripheral Pin Select Input)	141
AD1CHS (ADC Input Select)	217
AD1CON1 (ADC Control 1)	213
AD1CON2 (ADC Control 2)	215
AD1CON3 (ADC Control 3)	216
AD1CSSL (ADC Input Scan Select)	218
ALRMDATE (Alarm Date Value)	208
ALRMTIME (Alarm Time Value)	207
BMXBOOTSZ (Boot Flash (IFM) Size	51
BMXCON (Bus Matrix Configuration)	46
BMXDKPBA (Data RAM Kernel Program	
Base Address)	47
BMXDRMSZ (Data RAM Size Register)	50
BMXDUDBA (Data RAM User Data Base Address).	48
BMXDUPBA (Data RAM User Program	
Base Address)	49
BMXPFMSZ (Program Flash (PFM) Size)	51
BMXPUPBA (Program Flash (PFM) User Program	
Base Address)	50
CFGCON (Configuration Control)	248
CM1CON (Comparator 1 Control)	221
CMSTAT (Comparator Status Register)	222
CNCONx (Change Notice Control for PORTx)	142
CTMUCON (CTMU Control)	229
CVRCON (Comparator Voltage Reference Control).	225
DCHxCON (DMA Channel 'x' Control)	93
DCHxCPTR (DMA Channel 'x' Cell Pointer)	100
DCHxCSIZ (DMA Channel 'x' Cell-Size)	100
DCHxDAT (DMA Channel 'x' Pattern Data)	101
DCHxDPTR (Channel 'x' Destination Pointer)	99
DCHxDSA (DMA Channel 'x' Destination	
Start Address)	97
DCHxDSIZ (DMA Channel 'x' Destination Size)	98
DCHxECON (DMA Channel 'x' Event Control)	94
DCHxINT (DMA Channel 'x' Interrupt Control)	95

DCHxSPTR (DMA Channel 'x' Source Pointer)	9
DCHxSSA (DMA Channel 'x' Source Start Address) 97	7
DCHxSSIZ (DMA Channel 'x' Source Size) 98	В
DCRCCON (DMA CRC Control)	0
DCRCDATA (DMA CRC Data)	2
DCRCXOR (DMA CRCXOR Enable)	2
DEVCFG0 (Device Configuration Word 0) 24	1
DEVCFG1 (Device Configuration Word 1) 243	3
DEVCFG2 (Device Configuration Word 2)	5
DEVCFG3 (Device Configuration Word 3)	7
DEVID (Device and Revision ID)	9
DMAADDR (DMA Address)	9
DMACON (DMA Controller Control)	R
DMASTAT (DMA Status)	q
I2CxCON (I2C Control)	6
120x8001 (120 001110)	g
ICvCON (Input Capture 'x' Control)	a
IECx (Interrupt Enable Control)	9
IECX (Interrupt Eleg Status)	
IFSX (Interrupt Flag Status)	0
INTCON (Interrupt Control)	0
INTSTAT (Interrupt Status)	9
IPCX (Interrupt Priority Control)	1
IPIMR (Interrupt Proximity Timer)	9
NVMADDR (Flash Address)	6
NVMCON (Programming Control)	5
NVMDATA (Flash Program Data)57	7
NVMKEY (Programming Unlock) 56	6
NVMSRCADDR (Source Data Address) 57	7
OCxCON (Output Compare 'x' Control) 163	3
OSCCON (Oscillator Control)76	6
OSCTUN (FRC Tuning)79	9
PMADDR (Parallel Port Address) 195	5
PMAEN (Parallel Port Pin Enable) 196	6
PMAEN (Parallel Port Pin Enable)	6 1
PMAEN (Parallel Port Pin Enable)	6 1 3
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193	6 1 3 7
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80	6 1 3 7 0
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82	6 1 3 7 0 2
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147	6 1 3 7 2 1
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62	6 1 3 7 2 1 2
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 200	6 1 3 7 2 1 2 3
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCCON (RTC Control) 203	6 1 3 7 2 1 2 3 1
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCCON (RTC Control) 204 RTCOATE (RTC Date Value) 204	6 1 3 7 0 2 1 2 3 1 6
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 86 REFOTRIM (Reference Oscillator Trim) 86 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCCON (RTC Control) 204 RTCDATE (RTC Date Value) 204 RTCTIME (BTC Time Value) 204	6 1 3 7 0 2 1 2 3 1 6 5
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 88 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCCON (RTC Control) 203 RTCON (RTC Control) 204 RTCTIME (RTC Time Value) 206 RTCTIME (RTC Time Value) 206 RTCTIME (RTC Time Value) 206 RTCON (SPI Control) 207 RTCONE (RTC Time Value) 206 RTCIME (RTC Time Value) 206 RTCIME (RTC Time Value) 206 RTCIME (RTC Time Value) 206 RTCON (SPI Control) 207 RTCTIME (RTC Time Value) 206	6137021231657
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 86 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCCON (RTC Control) 200 RTCON (RTC Control) 200 RTCDATE (RTC Date Value) 206 SPIXCON (SPI Control) 205 SPIXCON(2 (SPI Control) 167	6 1 3 7 0 2 1 2 3 1 6 5 7 0
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCCON (RTC Control) 200 RTCDATE (RTC Date Value) 206 RTCTIME (RTC Time Value) 206 SPIXCON (SPI Control 2) 170 SPIXCON2 (SPI Control 2) 170	613702123165701
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 144 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCON (RTC Control) 204 RTCDATE (RTC Date Value) 205 SPIXCON (SPI Control) 167 SPIXCON2 (SPI Control 2) 170 SPIXSTAT (SPI Status) 177 SPIXSTAT (SPI Status) 177	6137021231657015
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCON (RTC Control) 204 RTCDATE (RTC Date Value) 205 SPIXCON (SPI Control) 167 SPIXCON2 (SPI Control 2) 170 SPIXSTAT (SPI Status) 177 T1CON (Type A Timer Control) 147	61370212316570150
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCON (RTC Control) 204 RTCDATE (RTC Date Value) 204 RTCTIME (RTC Time Value) 205 SPIXCON (SPI Control) 167 SPIXCON2 (SPI Control 2) 170 SPIXSTAT (SPI Status) 177 T1CON (Type A Timer Control) 144 TXCON (Lype B Timer Control) 145 TXCON (Type A Idmerce) 160	61370212316570150
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCON (RTC Control) 204 RTCDATE (RTC Date Value) 204 RTCTIME (RTC Time Value) 205 SPIXCON (SPI Control) 167 SPIXCON2 (SPI Control 2) 170 SPIXSTAT (SPI Status) 177 T1CON (Type A Timer Control) 143 TXCON (Type B Timer Control) 150 U14DDTD1 (USB Address) 120	613702123165701501
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 80 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCON (RTC Control) 204 RTCDATE (RTC Date Value) 204 RTCTIME (RTC Time Value) 204 SPIXCON (SPI Control) 167 SPIXCON2 (SPI Control 2) 177 SPIXSTAT (SPI Status) 177 T1CON (Type A Timer Control) 143 TXCON (Type B Timer Control) 143 TXCON (Type B Timer Control) 150 U1ADDR (USB Address) 127 U1BDTP1 (USB BDT Page 1) 122	61370212316570150134
PMAEN (Parallel Port Pin Enable) 196 PMCON (Parallel Port Control) 197 PMMODE (Parallel Port Mode) 193 PMSTAT (Parallel Port Status (Slave Modes Only) 193 REFOCON (Reference Oscillator Control) 86 REFOTRIM (Reference Oscillator Trim) 82 RPnR (Peripheral Pin Select Output) 147 RSWRST (Software Reset) 62 RTCALRM (RTC Alarm Control) 203 RTCON (RTC Control) 204 RTCDATE (RTC Time Value) 204 SPIXCON (SPI Control) 165 SPIXCON2 (SPI Control) 165 SPIXSTAT (SPI Status) 177 T1CON (Type A Timer Control) 144 TXCON (Type B Timer Control) 145 U1ADDR (USB Address) 122 U1BDTP1 (USB BDT Page 1) 122 U1BDTP2 (USB BDT Page 2) 124	61370212316570150134
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)197REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCDATE (RTC Date Value)204SPIXCON (SPI Control)165SPIXCON2 (SPI Control 2)177SPIXSTAT (SPI Status)177T1CON (Type A Timer Control)144TxCON (Type B Timer Control)145U1ADDR (USB Address)122U1BDTP1 (USB BDT Page 1)122U1BDTP3 (USB BDT Page 3)124	6 1 3 7 0 2 1 2 3 1 6 5 7 0 1 5 0 1 3 4 4 -
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)193REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCDATE (RTC Date Value)204SPIxCON (SPI Control)165SPIxCON2 (SPI Control 2)177SPIxSTAT (SPI Status)177T1CON (Type A Timer Control)144TxCON (Type B Timer Control)145U1ADDR (USB Address)122U1BDTP1 (USB BDT Page 1)122U1BDTP3 (USB BDT Page 3)124U12OKFG1 (USB Configuration 1)124	61370212316570150134455
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)197REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCDATE (RTC Date Value)204SPIXCON (SPI Control)165SPIXCON2 (SPI Control 2)177SPIXSTAT (SPI Status)177T1CON (Type A Timer Control)144TxCON (Type B Timer Control)145U1ADDR (USB Address)122U1BDTP1 (USB BDT Page 1)122U1BDTP3 (USB BDT Page 3)124U1CNN (USB Control)115U1CON (USB Control)124U1CON (USB Control)125U1CON (USB Control)126U1CON (USB Control)126U1CON (USB Control)126U1CON (USB Control)126U1CON (USB Control)115U1CON (USB Control)115U1CO	61370212316570150134459-
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)197REFOCON (Reference Oscillator Control)80REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCDATE (RTC Date Value)204SPIxCON (SPI Control)165SPIxCON2 (SPI Control 2)177SPIxSTAT (SPI Status)177T1CON (Type A Timer Control)144TxCON (Type B Timer Control)145U1ADDR (USB Address)122U1BDTP1 (USB BDT Page 1)122U1BDTP3 (USB BDT Page 3)122U1CNFG1 (USB Control)115U1CON (USB Control)115U1	613702123165701501344597
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)197REFOCON (Reference Oscillator Control)80REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCDATE (RTC Date Value)204SPIxCON (SPI Control)165SPIxCON2 (SPI Control 2)177SPIxSTAT (SPI Status)177T1CON (Type A Timer Control)144TxCON (Type B Timer Control)145U1BDTP1 (USB BDT Page 1)122U1BDTP3 (USB BDT Page 3)124U1CNFG1 (USB Configuration 1)125U1EIE (USB Error Interrupt Enable)115U1EIR (USB Error Interrupt Status)115U1EIR (USB Error Interrupt Status)115	6137021231657015013445975
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)193REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCTIME (RTC Time Value)206SPIxCON2 (SPI Control)165SPIxCON2 (SPI Control 2)177SPIxSTAT (SPI Status)177T1CON (Type A Timer Control)165U1ADDR (USB Address)122U1BDTP1 (USB BDT Page 1)122U1BDTP3 (USB BDT Page 3)124U1CNFG1 (USB Configuration 1)125U1CON (USB Control)115U1EIE (USB Error Interrupt Enable)115U1EIR (USB Error Interrupt Status)114U1EIP0-U1EP15 (USB Endpoint Control)126	6 1 3 7 0 2 1 2 3 1 6 5 7 0 1 5 0 1 3 4 4 5 9 7 5 6 5 7
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)197REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)207RTCCON (RTC Control)207RTCCON (RTC Control)206RTCTIME (RTC Time Value)206SPIxCON2 (SPI Control)167SPIxCON2 (SPI Control 2)177SPIxSTAT (SPI Status)177T1CON (Type A Timer Control)144TxCON (Type B Timer Control)145U1ADDR (USB Address)122U1BDTP1 (USB BDT Page 1)122U1BDTP3 (USB BDT Page 3)124U1CNFG1 (USB Configuration 1)125U1CON (USB Control)115U1EIE (USB Error Interrupt Enable)117U1EIR (USB Error Interrupt Status)114U1ERMH (USB Frame Number High)124	6 1 3 7 0 2 1 2 3 1 6 5 7 0 1 5 0 1 3 4 4 5 9 7 5 6 2
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)193REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCDATE (RTC Date Value)204SPIxCON (SPI Control)205SPIxCON (SPI Control 2)176SPIxCON2 (SPI Control 2)177T1CON (Type A Timer Control)145TxCON (Type B Timer Control)145TxCON (Type B Timer Control)142TxCON (USB Address)122U1BDTP1 (USB BDT Page 1)122U1CNFG1 (USB Configuration 1)124U1CON (USB Control)115U12CON (USB Control)115U12EIE (USB Error Interrupt Enable)117U1EIR (USB Frame Number High)122U1FRMH (USB Frame Number High)122U1FRML (USB Frame Number Low)124	6137021231657015013445975621
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)197REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)147RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)207RTCCON (RTC Control)207RTCON (RTC Control)206RTCTIME (RTC Time Value)206SPIXCON (SPI Control)167SPIXCON2 (SPI Control 2)177T1CON (Type A Timer Control)147TXCON (Type B Timer Control)147TXCON (Type B Timer Control)147TXCON (USB Address)122U1BDTP1 (USB BDT Page 1)122U1CNFG1 (USB Configuration 1)124U1CNFG1 (USB Control)114U1CON (USB Control)115U1EIE (USB Error Interrupt Enable)117U1ERMH (USB Frame Number High)122U1FRMH (USB Frame Number High)122U1IE (USB Interrupt Enable)114	61370212316570150134459756214
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)193REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)144RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCTIME (RTC Time Value)204SPIXCON (SPI Control)205SPIXCON (SPI Control 2)176SPIXCON2 (SPI Control 2)177T1CON (Type A Timer Control)144TxCON (Type B Timer Control)145TxCON (USB Address)122U1BDTP1 (USB BDT Page 1)122U1SB TP3 (USB BDT Page 2)124U1CON (USB Control)115U1CON (USB Control)115U1EIE (USB Error Interrupt Enable)117U1EIR (USB Frame Number High)122U1FRMH (USB Frame Number High)122U1IE (USB Interrupt Enable)114U1IR (USB Interrupt Enabl	613702123165701501344597562143
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)193REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)144RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCTIME (RTC Time Value)204RTCTIME (RTC Time Value)205SPIXCON (SPI Control)165SPIXCON (SPI Control 2)177T1CON (Type A Timer Control)144TxCON (Type B Timer Control)145TxCON (Type B Timer Control)145TxCON (USB Address)122U1BDTP1 (USB BDT Page 1)122U1CNFG1 (USB Control)115U1CON (USB Control)115U1EIE (USB Error Interrupt Enable)117U1EIR (USB Frame Number High)122U1FRMH (USB Frame Number High)122U1FRMH (USB Frame Number Low)124U1R (USB Interrupt Enable)114U1R (USB Interrupt Enable)114U1IR (USB Interrupt)	6137021231657015013445975621431
PMAEN (Parallel Port Pin Enable)196PMCON (Parallel Port Control)197PMMODE (Parallel Port Mode)193PMSTAT (Parallel Port Status (Slave Modes Only)193REFOCON (Reference Oscillator Control)86REFOTRIM (Reference Oscillator Trim)82RPnR (Peripheral Pin Select Output)144RSWRST (Software Reset)62RTCALRM (RTC Alarm Control)203RTCCON (RTC Control)204RTCTIME (RTC Time Value)204RTCTIME (RTC Time Value)205SPIXCON (SPI Control)165SPIXCON (SPI Control 2)177T1CON (Type A Timer Control)144TXCON (Type B Timer Control)145TXCON (Type B Trage 2)122U1BDTP1 (USB BDT Page 1)122U1CNFG1 (USB Configuration 1)122U1CNFG1 (USB Control)115U12ER (USB Error Interrupt Enable)117U14ER (USB Frame Number High)122U1FRMH (USB Frame Number High)122U1FRMH (USB Frame Number Low)124U1CGON (USB OTG Control)117U10TGCON (USB OTG Control)117U10TGE (USB OTG Interrupt Enable)114U11R (USB Interrupt)115U10TGIE (USB OTG Interrupt Enable)117U10TGIE (USB OTG Interrupt Enable)116	61370212316570150134459756214319

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV = ISO/TS 16949=

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

 $\ensuremath{\mathsf{SQTP}}$ is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2011-2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN:978-1-5224-0471-2