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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256d-i-tl

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

1.0 DEVICE OVERVIEW

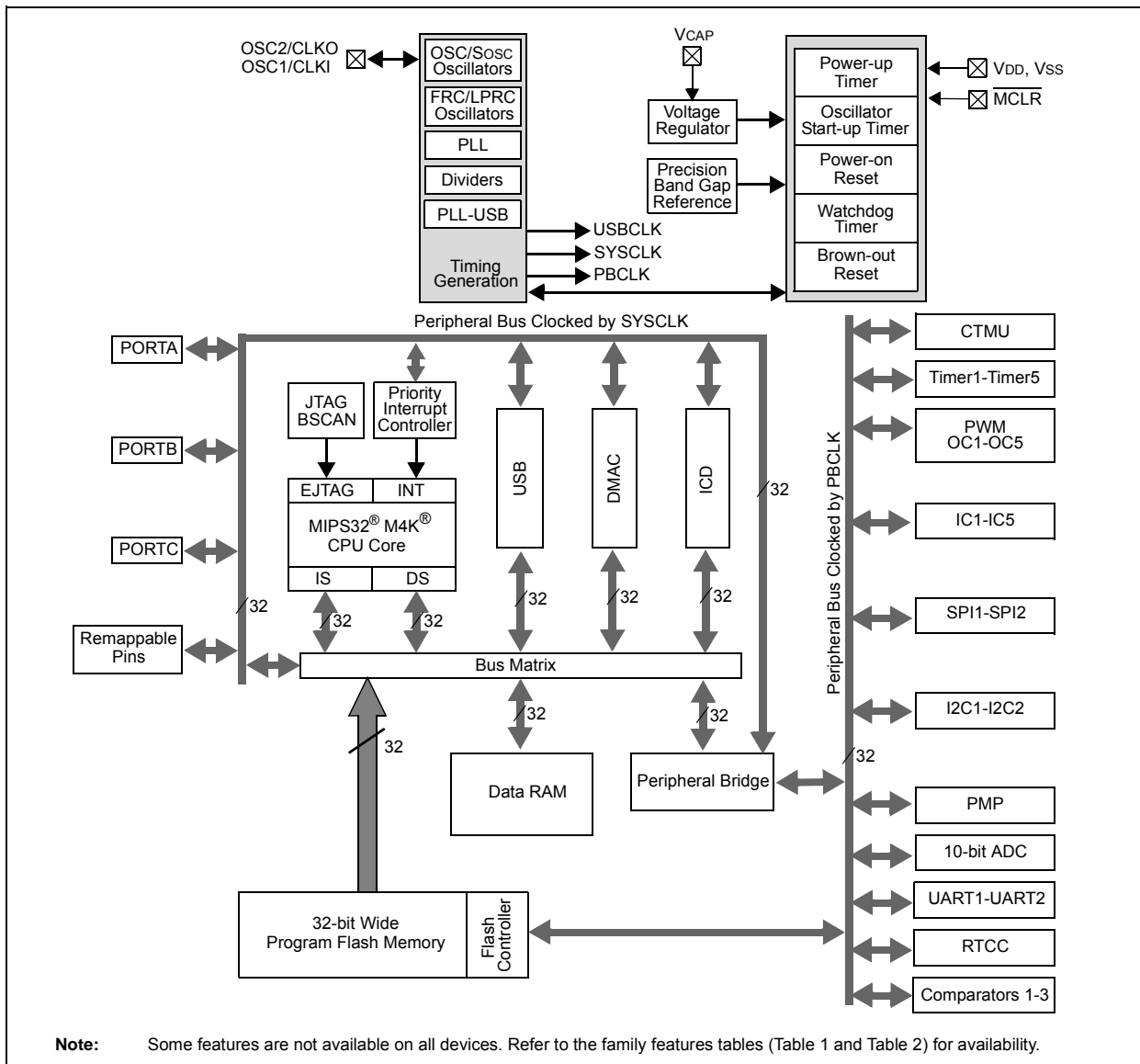
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX1XX/2XX 28/36/44-pin Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/36/44-pin Family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM



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2.9 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-5 and Figure 2-6.

FIGURE 2-5: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION

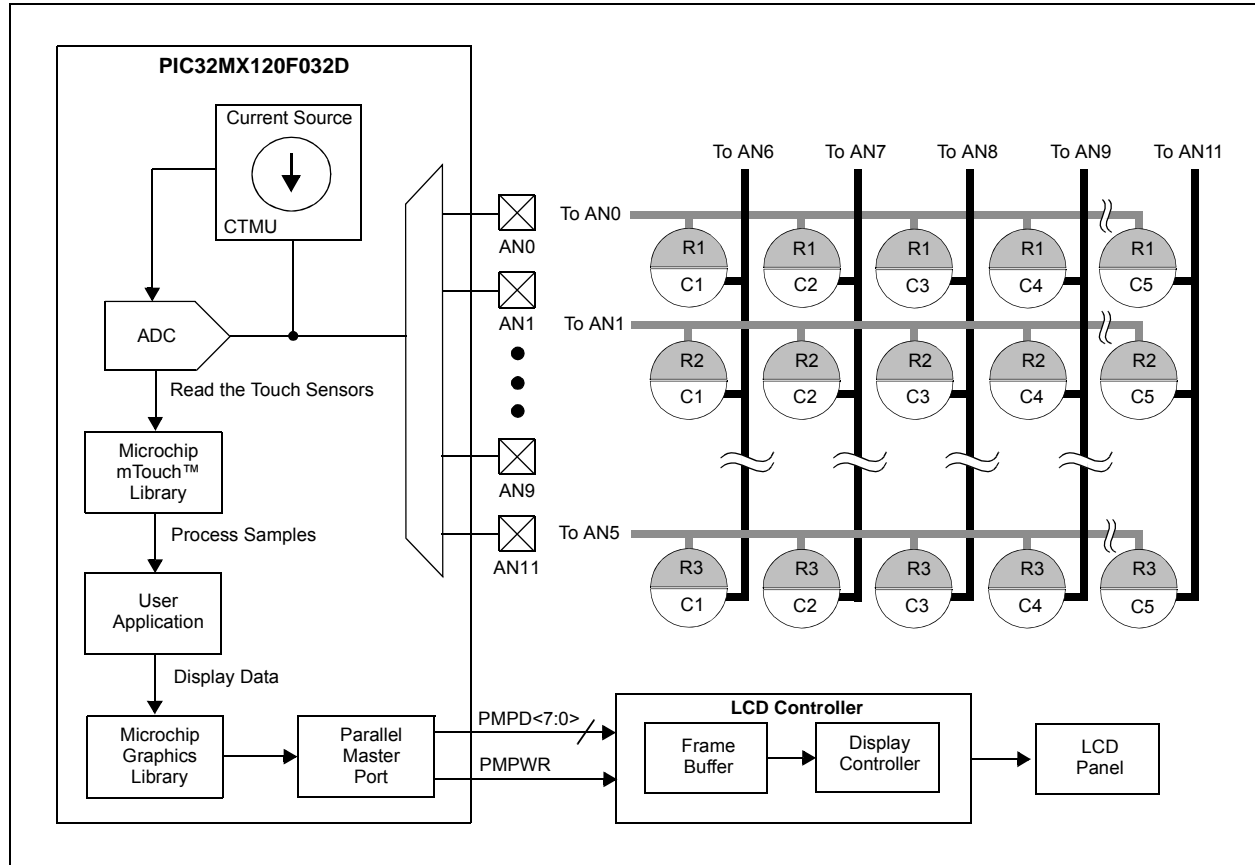
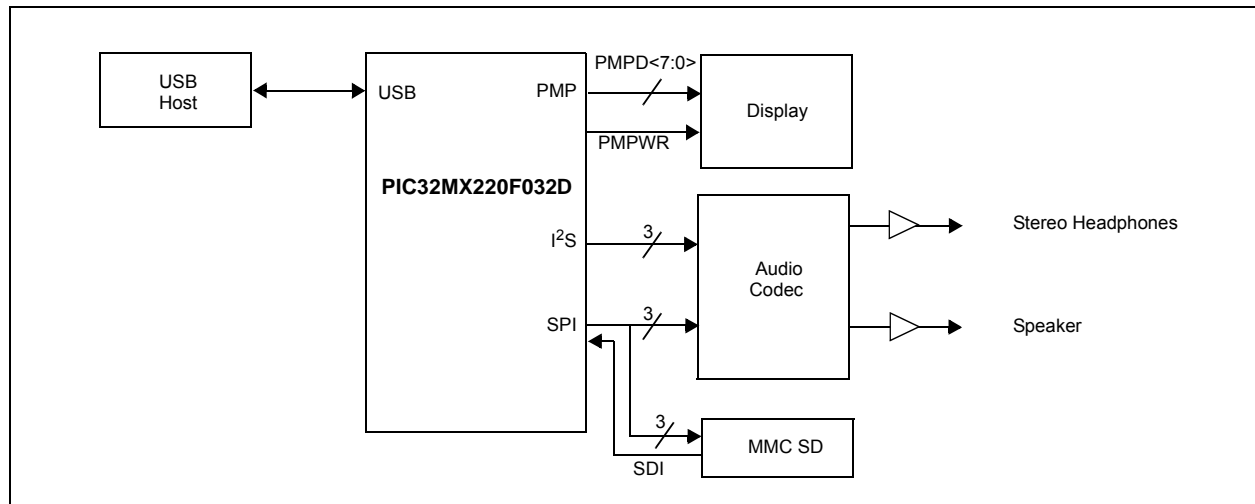


FIGURE 2-6: AUDIO PLAYBACK APPLICATION



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e® Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS32® M4K® PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul <i>rt</i>) (div <i>rs</i>)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU, MSUB/MSUBU	16 bits	1	1
	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

5.1 Flash Controller Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F400	NVMCON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	—	—	—	—	—	—	—	NVMOP<3:0>				0000
F410	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
F420	NVMADDR ⁽¹⁾	31:16	NVMADDR<31:0>																0000
		15:0																	0000
F430	NVMDATA	31:16	NVMDATA<31:0>																0000
		15:0																	0000
F440	NVMSRCADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

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REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
	—	—	—	—	—	—	CMR	VREGS
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR ⁽¹⁾	POR ⁽¹⁾

Legend:	HS = Set by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
 1 = Configuration mismatch Reset has occurred
 0 = Configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
 1 = Regulator is enabled and is on during Sleep mode
 0 = Regulator is disabled and is off during Sleep mode

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin Flag bit
 1 = Master Clear (pin) Reset has occurred
 0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
 1 = Software Reset was executed
 0 = Software Reset as not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
 1 = WDT Time-out has occurred
 0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
 1 = Device was in Sleep mode
 0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
 1 = Device was in Idle mode
 0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit⁽¹⁾
 1 = Brown-out Reset has occurred
 0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit⁽¹⁾
 1 = Power-on Reset has occurred
 0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view next detection.

7.1 Interrupt Control Registers

TABLE 7-2: INTERRUPT REGISTER MAP

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	FCEIF	RTCCIF	FSCMIF	AD1IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	DMA3IF	DMA2IF	DMA1IF	DMA0IF	CTMUIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	SPI2RXIF	SPI2EIF	PMPEIF	PMPIF	0000
		15:0	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	USBIF ⁽²⁾	CMP3IF	CMP2IF	CMP1IF	0000
1060	IEC0	31:16	FCEIE	RTCCIE	FSCMIE	AD1IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	DMA3IE	DMA2IE	DMA1IE	DMA0IE	CTMUIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	SPI2RXIE	SPI2EIE	PMPEIE	PMPIE	0000
		15:0	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	USBIE ⁽²⁾	CMP3IE	CMP2IE	CMP1IE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>			—	—	—	CS1IP<2:0>			CS1IS<1:0>	0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>			—	—	—	CTIP<2:0>			CTIS<1:0>	0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>			—	—	—	OC1IP<2:0>			OC1IS<1:0>	0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>			—	—	—	T1IP<2:0>			T1IS<1:0>	0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>			—	—	—	OC2IP<2:0>			OC2IS<1:0>	0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>			—	—	—	T2IP<2:0>			T2IS<1:0>	0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>			—	—	—	OC3IP<2:0>			OC3IS<1:0>	0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>			—	—	—	T3IP<2:0>			T3IS<1:0>	0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>			—	—	—	OC4IP<2:0>			OC4IS<1:0>	0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>			—	—	—	T4IP<2:0>			T4IS<1:0>	0000
10E0	IPC5	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>			—	—	—	OC5IP<2:0>			OC5IS<1:0>	0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>			—	—	—	T5IP<2:0>			T5IS<1:0>	0000
10F0	IPC6	31:16	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>			—	—	—	FCEIP<2:0>			FCEIS<1:0>	0000
		15:0	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>			—	—	—	FSCMP<2:0>			FSCMIS<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.
- 2:** These bits are not available on PIC32MX1XX devices.
- 3:** This register does not have associated CLR, SET, INV registers.

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REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-y	R/W-y	R/W-y	R/W-0	R/W-0	R/W-1
	—	—	PLLODIV<2:0>			FRCDIV<2:0>		
23:16	U-0	R-0	R-1	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>		
15:8	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-y	R/W-0
	CLKLOCK	ULOCK ⁽¹⁾	SLOCK	SLPEN	CF	UFRocen ⁽¹⁾	SOSCEN	OSWEN

Legend: y = Value set from Configuration bits on POR
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2 (default setting)
- 000 = FRC divided by 1

bit 23 **Unimplemented:** Read as '0'

bit 22 **SOSCRDY:** Secondary Oscillator (Sosc) Ready Indicator bit

- 1 = The Secondary Oscillator is running and is stable
- 0 = The Secondary Oscillator is still warming up or is turned off

bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit

- 1 = PBDIV<1:0> bits can be written
- 0 = PBDIV<1:0> bits cannot be written

bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits

- 11 = PBCLK is SYSCLK divided by 8 (default)
- 10 = PBCLK is SYSCLK divided by 4
- 01 = PBCLK is SYSCLK divided by 2
- 00 = PBCLK is SYSCLK divided by 1

Note 1: This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

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REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

bit 18-16 **PLLMULT<2:0>**: Phase-Locked Loop (PLL) Multiplier bits

- 111 = Clock is multiplied by 24
- 110 = Clock is multiplied by 21
- 101 = Clock is multiplied by 20
- 100 = Clock is multiplied by 19
- 011 = Clock is multiplied by 18
- 010 = Clock is multiplied by 17
- 001 = Clock is multiplied by 16
- 000 = Clock is multiplied by 15

bit 15 **Unimplemented**: Read as '0'

bit 14-12 **COSC<2:0>**: Current Oscillator Selection bits

- 111 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (OSCCON<26:24>)
- 110 = Internal Fast RC (FRC) Oscillator divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (Sosc)
- 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (Posc) (XT, HS or EC)
- 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast RC (FRC) Oscillator

bit 11 **Unimplemented**: Read as '0'

bit 10-8 **NOOSC<2:0>**: New Oscillator Selection bits

- 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC Oscillator (FRC) divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (Sosc)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (XT, HS or EC)
- 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK**: Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):

- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):

Clock and PLL selections are never locked and may be modified.

bit 6 **ULOCK**: USB PLL Lock Status bit⁽¹⁾

- 1 = The USB PLL module is in lock or USB PLL module start-up timer is satisfied
- 0 = The USB PLL module is out of lock or USB PLL module start-up timer is in progress or the USB PLL is disabled

bit 5 **SLOCK**: PLL Lock Status bit

- 1 = The PLL module is in lock or PLL module start-up timer is satisfied
- 0 = The PLL module is out of lock, the PLL start-up timer is running, or the PLL is disabled

bit 4 **SLPEN**: Sleep Mode Enable bit

- 1 = The device will enter Sleep mode when a WAIT instruction is executed
- 0 = The device will enter Idle mode when a WAIT instruction is executed

Note 1: This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

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REGISTER 9-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	CHBUSY	—	—	—	—	—	—	CHCHNS ⁽¹⁾
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN ⁽²⁾	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit

1 = Channel is active or has been enabled

0 = Channel is inactive or has been disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit⁽¹⁾

1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)

0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit⁽²⁾

1 = Channel is enabled

0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit

1 = Channel start/abort events will be registered, even if the channel is disabled

0 = Channel start/abort events will be ignored if the channel is disabled

bit **CHCHN:** Channel Chain Enable bit

1 = Allow channel to be chained

0 = Do not allow channel to be chained

bit 4 **CHAEN:** Channel Automatic Enable bit

1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete

0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit

1 = An event has been detected

0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits

11 = Channel has priority 3 (highest)

10 = Channel has priority 2

01 = Channel has priority 1

00 = Channel has priority 0

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE ⁽¹⁾ EOFEE ⁽²⁾	PIDEE

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit

1 = BTSEF interrupt is enabled

0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit

1 = BMXEF interrupt is enabled

0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit

1 = DMAEF interrupt is enabled

0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit

1 = BTOEF interrupt is enabled

0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit

1 = DFN8EF interrupt is enabled

0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit

1 = CRC16EF interrupt is enabled

0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit⁽¹⁾

1 = CRC5EF interrupt is enabled

0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit⁽²⁾

1 = EOF interrupt is enabled

0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit

1 = PIDEF interrupt is enabled

0 = PIDEF interrupt is disabled

Note 1: Device mode.

2: Host mode.

Note: For an interrupt to propagate the USBIF register, the UERRIE (U1IE<1>) bit must be set.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

REGISTER 10-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
	UTEYE	UOEMON	—	USBSIDL	—	—	—	UASUSPND

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit

1 = Eye-Pattern Test is enabled

0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB $\overline{\text{OE}}$ Monitor Enable bit

1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving

0 = OE signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit

1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 10-5.

0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock.

11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable port number.

11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin.

Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

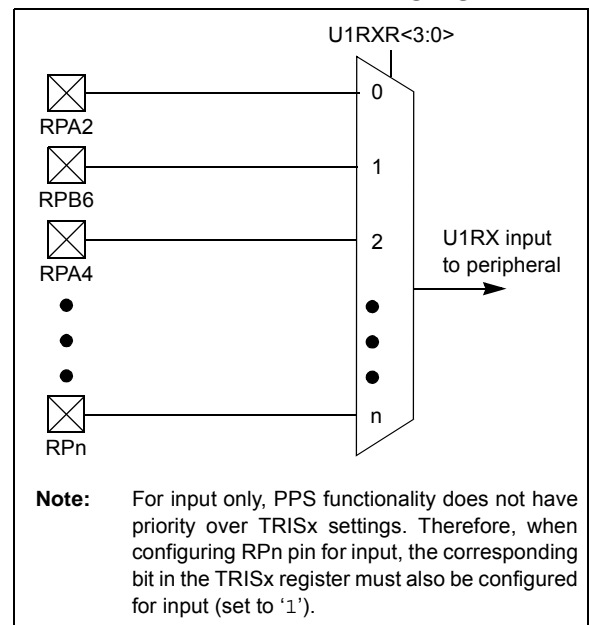
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [pin name]R registers, where [pin name] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 20-4: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	PTEN14	—	—	—	PTEN<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 15-14 **PTEN14:** PMCS1 Address Port Enable bits

1 = PMA14 functions as either PMA14 or PMCS1⁽¹⁾

0 = PMA14 functions as port I/O

bit 13-11 **Unimplemented:** Read as '0'

bit 10-2 **PTEN<10:2>:** PMP Address Port Enable bits

1 = PMA<10:2> function as PMP address lines

0 = PMA<10:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits

1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL⁽²⁾

0 = PMA1 and PMA0 pads functions as port I/O

Note 1: The use of this pin as PMA14 or CS1 is selected by the CSF<1:0> bits in the PMCON register.

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by bits ADRMUX<1:0> in the PMCON register.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	MONTH10	MONTH01<3:0>			
15:8	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	DAY10<1:0>		DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	—	—	—	—	—	WDAY01<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MONTH10:** Binary Coded Decimal value of months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAY10<1:0>:** Binary Coded Decimal value of days bits, 10s place digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY01<2:0>:** Binary Coded Decimal value of weekdays bits; contains a value from 0 to 6

23.1 Comparator Control Registers

TABLE 23-1: COMPARATOR REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A020	CM3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

27.3 On-Chip Voltage Regulator

All PIC32MX1XX/2XX 28/36/44-pin Family devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX1XX/2XX 28/36/44-pin Family family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 30.1 "DC Characteristics"**.

Note: It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

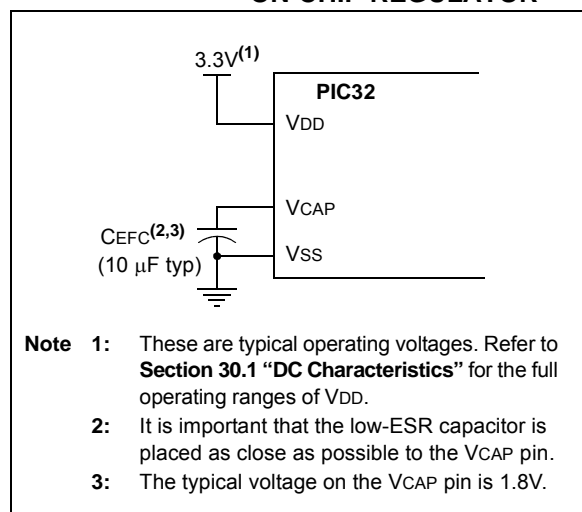
27.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

27.3.2 ON-CHIP REGULATOR AND BOR

PIC32MX1XX/2XX 28/36/44-pin Family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 30.1 "DC Characteristics"**.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



27.4 Programming and Diagnostics

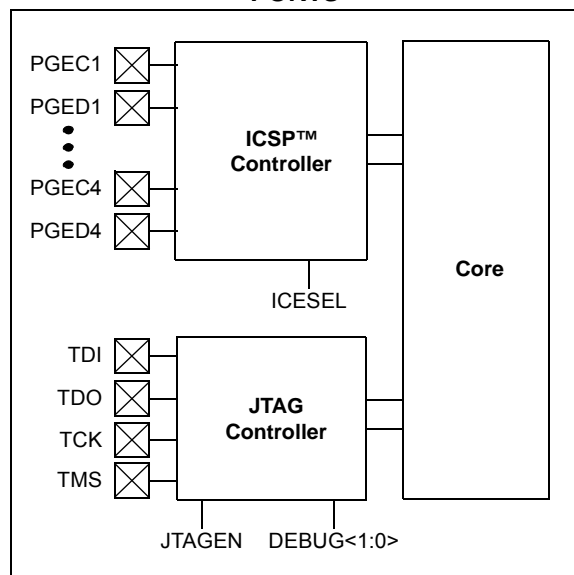
PIC32MX1XX/2XX 28/36/44-pin Family devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

Figure 27-2 illustrates a block diagram of the programming, debugging, and trace ports.

FIGURE 27-2: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/librarian features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-39: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
PM11	TWR	PMWR Pulse Width	—	1 TPB	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPB	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPB	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 30-40: OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	—
USB321	VoL	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	VoH	Voltage Output High	2.8	—	3.6	V	1.425 kΩ load connected to ground

Note 1: These parameters are characterized, but not tested in manufacturing.