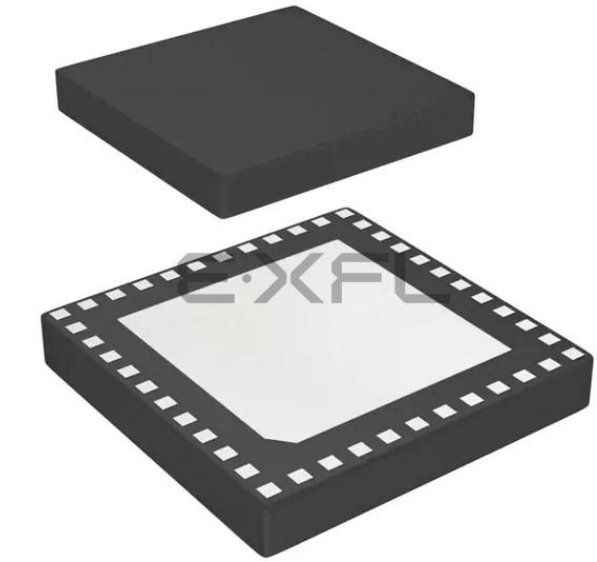
Microchip Technology - PIC32MX270F256DT-50I/TL Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256dt-50i-tl

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		—	—	27	O	—	Parallel Master Port address (Demultiplexed Master modes)
PMA3		—	—	38	O	—	
PMA4		—	—	37	O	—	
PMA5		—	—	4	O	—	
PMA6		—	—	5	O	—	
PMA7		—	—	13	O	—	
PMA8		—	—	32	O	—	
PMA9		—	—	35	O	—	
PMA10		—	—	12	O	—	
PMCS1	23	26	29	15	O	—	Parallel Master Port Chip Select 1 strobe
PMD0	20(2)	23(2)	26(2)	10(2)	I/O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes)
	1(3)	4(3)	35(3)	21(3)			
PMD1	19(2)	22(2)	25(2)	9(2)	I/O	TTL/ST	
	2(3)	5(3)	36(3)	22(3)			
PMD2	18(2)	21(2)	24(2)	8(2)	I/O	TTL/ST	
	3(3)	6(3)	1(3)	23(3)			
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12(2)	15(2)	16(2)	42(2)	I/O	TTL/ST	
	28(3)	3(3)	34(3)	20(3)			
PMD7	11(2)	14(2)	15(2)	41(2)	I/O	TTL/ST	
	27(3)	2(3)	33(3)	19(3)			
PMRD	21	24	27	11	O	—	Parallel Master Port read strobe
PMWR	22(2)	25(2)	28(2)	14(2)	O	—	Parallel Master Port write strobe
	4(3)	7(3)	2(3)	24(3)			
VBUS	12(3)	15(3)	16(3)	42(3)	I	Analog	USB bus power monitor
VUSB3V3	20(3)	23(3)	26(3)	10(3)	P	—	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22(3)	25(3)	28(3)	14(3)	O	—	USB Host and OTG bus power control output
D+	18(3)	21(3)	24(3)	8(3)	I/O	Analog	USB D+
D-	19(3)	22(3)	25(3)	9(3)	I/O	Analog	USB D-

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

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TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
Watchdog Timer	0xBF80	0x0000
RTCC		0x0200
Timer1-5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
IC1 and IC2		0x5000
SPI1 and SPI2		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC		0x9000
CVREF		0x9800
Comparator		0xA000
CTMU		0xA200
Oscillator		0xF000
Device and Revision ID		0xF220
Peripheral Module Disable		0xF240
Flash Controller		0xF400
Reset		0xF600
PPS		0xFA04
Interrupts	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
USB		0x5050
PORTA-PORTC		0x6000
Configuration	0xBFC0	0x0BF0

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REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXPFMSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXPFMSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXPFMSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXPFMSZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXPFMSZ<31:0>:** Program Flash Memory (PFM) Size bits
Static value that indicates the size of the PFM in bytes:
0x00004000 = Device has 16 KB Flash
0x00008000 = Device has 32 KB Flash
0x00010000 = Device has 64 KB Flash
0x00020000 = Device has 128 KB Flash
0x00040000 = Device has 256 KB Flash

REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXBOOTSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXBOOTSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXBOOTSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXBOOTSZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits
Static value that indicates the size of the Boot PFM in bytes:
0x00000C00 = Device has 3 KB boot Flash

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Program Memory"** (DS60001121), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "*PIC32 Flash Programming Specification*" (DS60001145), which can be downloaded from the Microchip web site.

Note: The Flash page size on PIC32MX-1XX/2XX 28/36/44-pin Family devices is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

NOTES:

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REGISTER 9-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0>(1)							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0>(1)							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)
- 11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
- •
- •
- •
- 00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
- 00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)
- 11111111 = Interrupt 255 will initiate a DMA transfer
- •
- •
- •
- 00000001 = Interrupt 1 will initiate a DMA transfer
- 00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit
- 1 = A DMA transfer is forced to begin when this bit is written to a '1'
- 0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit
- 1 = A DMA transfer is aborted when this bit is written to a '1'
- 0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit
- 1 = Abort transfer and clear CHEN on pattern match
- 0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit
- 1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
- 0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit
- 1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
- 0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See **Table 7-1: "Interrupt IRQ, Vector and Bit Location"** for the list of available interrupt IRQ sources.

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REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = A change in the ID state was detected
- 0 = No change in the ID state was detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = A change on the session valid input was detected
- 0 = No change on the session valid input was detected

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REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)

bit 1 **CRC5EF:** CRC5 Host Error Flag bit(4)
1 = Token packet rejected due to CRC5 error
0 = Token packet accepted
EOFEF: EOF Error Flag bit(3,5)
1 = An EOF error condition was detected
0 = No EOF error condition was detected

bit 0 **PIDEF:** PID Check Failure Flag bit
1 = PID check failed
0 = PID check passed

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

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TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FB8C	RPC8R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC8<3:0>				0000
FB90	RPC9R(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC9<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is only available on 44-pin devices.
2: This register is only available on PIC32MX1XX devices.
3: This register is only available on 36-pin and 44-pin devices.

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REGISTER 11-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A, B, C)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit
- 1 = CN is enabled
- 0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Idle mode halts CN operation
- 0 = Idle does not affect CN operation

bit 12-0 **Unimplemented:** Read as '0'

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NOTES:

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21.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

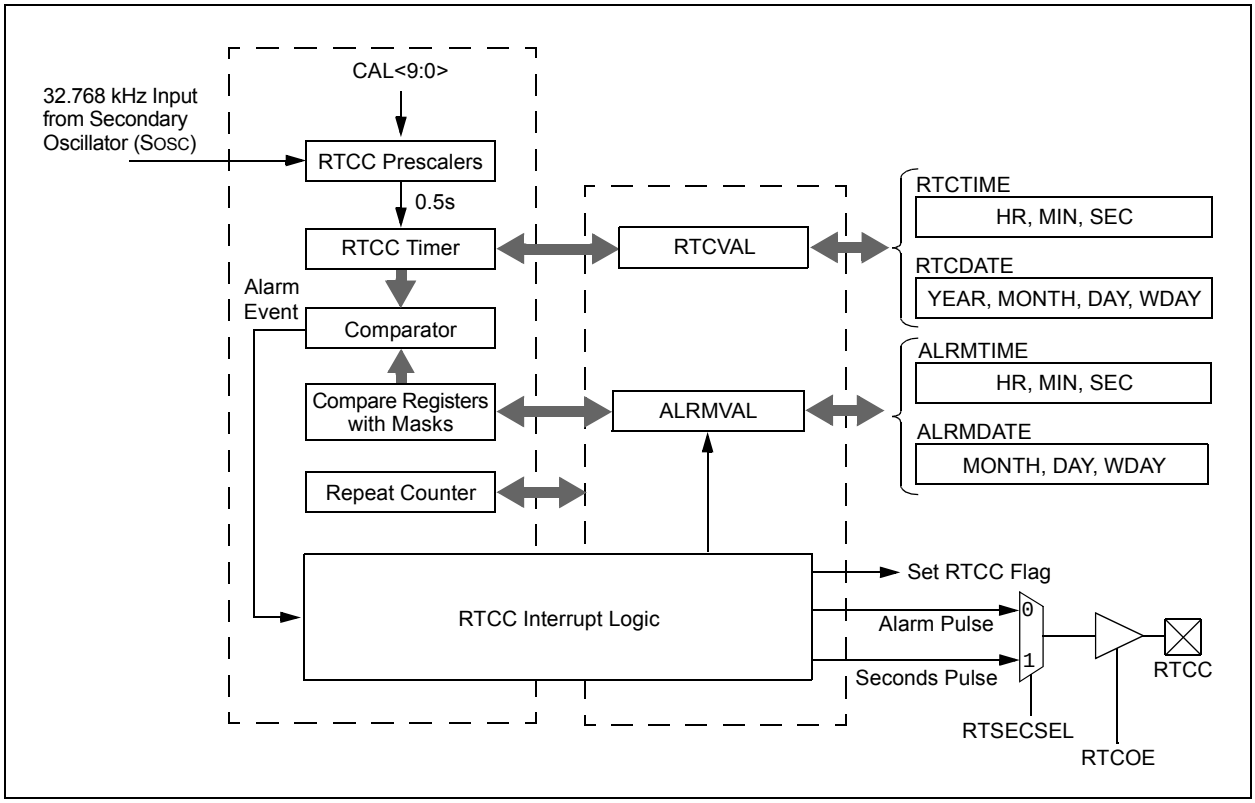
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

Following are some of the key features of this module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: day, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin

FIGURE 21-1: RTCC BLOCK DIAGRAM



22.1 ADC Control Registers

TABLE 22-1: ADC REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	AD1CON1(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE	0000
9010	AD1CON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG<2:0>			OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000
9020	AD1CON3(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>								0000
9040	AD1CHS(1)	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9050	AD1CSSL(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16	ADC Result Word 0 (ADC1BUF0<31:0>)																0000
		15:0																	0000
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)																0000
		15:0																	0000
9090	ADC1BUF2	31:16	ADC Result Word 2 (ADC1BUF2<31:0>)																0000
		15:0																	0000
90A0	ADC1BUF3	31:16	ADC Result Word 3 (ADC1BUF3<31:0>)																0000
		15:0																	0000
90B0	ADC1BUF4	31:16	ADC Result Word 4 (ADC1BUF4<31:0>)																0000
		15:0																	0000
90C0	ADC1BUF5	31:16	ADC Result Word 5 (ADC1BUF5<31:0>)																0000
		15:0																	0000
90D0	ADC1BUF6	31:16	ADC Result Word 6 (ADC1BUF6<31:0>)																0000
		15:0																	0000
90E0	ADC1BUF7	31:16	ADC Result Word 7 (ADC1BUF7<31:0>)																0000
		15:0																	0000
90F0	ADC1BUF8	31:16	ADC Result Word 8 (ADC1BUF8<31:0>)																0000
		15:0																	0000
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)																0000
		15:0																	0000
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for details.

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REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON(1)	COE	CPOL(2)	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit(1)
- 1 = Module is enabled. Setting this bit does not affect the other bits in this register
- 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is driven on the output CxOUT pin
- 0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit(2)
- 1 = Output is inverted
- 0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
- 1 = Output of the Comparator is a '1'
- 0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
- 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
- 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
- 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
- 00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit
- 1 = Comparator non-inverting input is connected to the internal CVREF
- 0 = Comparator non-inverting input is connected to the CXINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
- 11 = Comparator inverting input is connected to the IVREF
- 10 = Comparator inverting input is connected to the CxIND pin
- 01 = Comparator inverting input is connected to the CxINC pin
- 00 = Comparator inverting input is connected to the CxINB pin

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

REGISTER 23-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	C3OUT	C2OUT	C1OUT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = All Comparator modules are disabled when the device enters Idle mode
- 0 = All Comparator modules continue to operate when the device enters Idle mode

bit 12-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator Output bit
- 1 = Output of Comparator 3 is a '1'
- 0 = Output of Comparator 3 is a '0'

bit 1 **C2OUT:** Comparator Output bit
- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit
- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

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TABLE 30-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP51	TSSH2DOZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	5	—	25	ns	—
SP52	TSCH2SSH TSCL2SSH	$\overline{SSx}$ ↑ after SCKx Edge	TSCK + 20	—	—	ns	—
SP60	TSSL2DOV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	25	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns.

4: Assumes 50 pF load on all SPIx pins.

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FIGURE 32-3: TYPICAL IPD CURRENT @ VDD = 3.3V

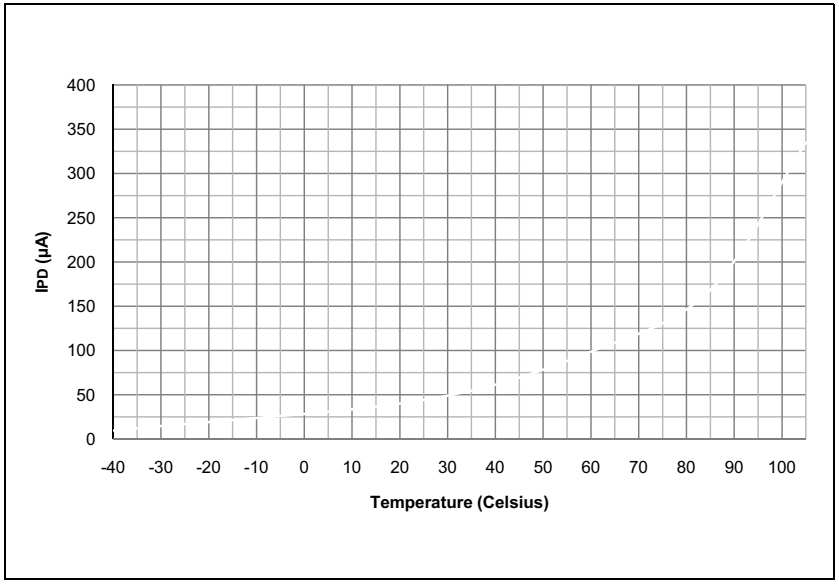


FIGURE 32-4: TYPICAL IDD CURRENT @ VDD = 3.3V

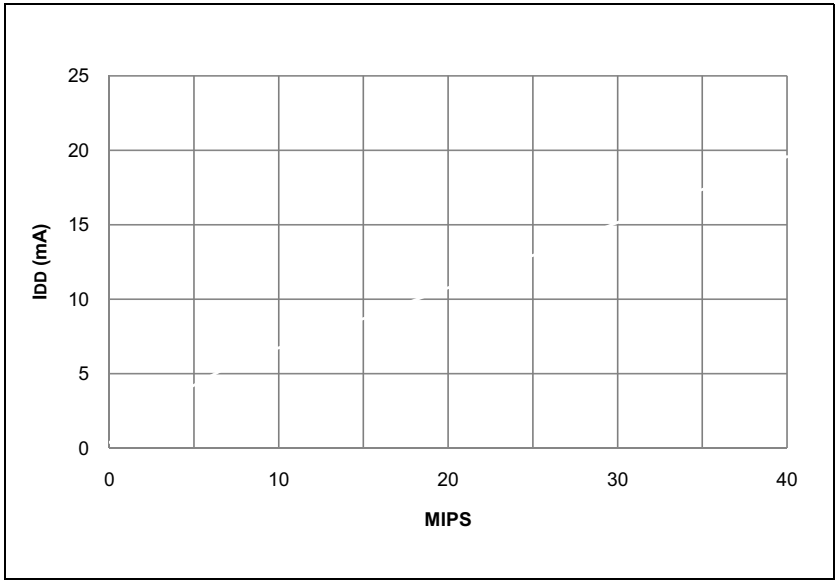
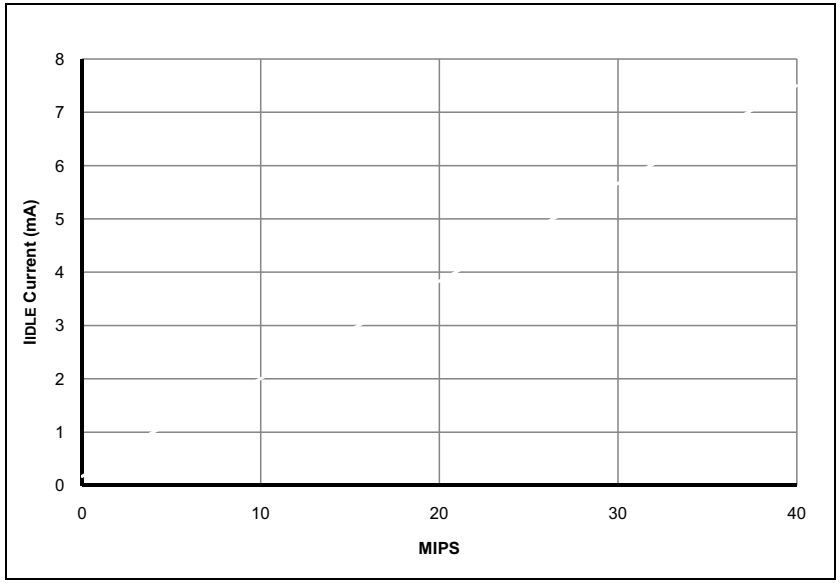


FIGURE 32-5: TYPICAL IIDLE CURRENT @ VDD = 3.3V



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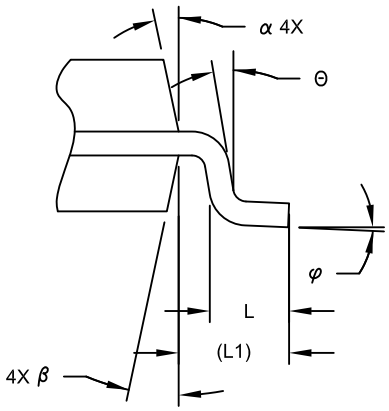
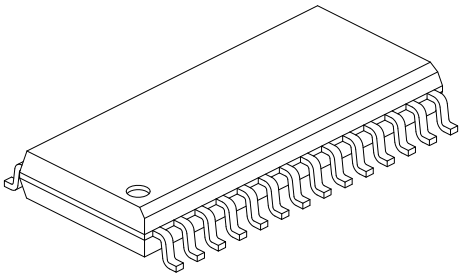
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

Revision G (April 2015)

This revision includes the addition of the following devices:

- PIC32MX130F256B
- PIC32MX230F256B
- PIC32MX130F256D
- PIC32MX230F256D

The title of the document was updated to avoid confusion with the PIC32MX1XX/2XX/5XX 64/100-pin Family data sheet.

All peripheral SFR maps have been relocated from the Memory chapter to their respective peripheral chapters.

In addition, this revision includes the following major changes as described in Table A-6, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-6: MAJOR SECTION UPDATES

Section	Update Description
32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog	Added new devices to the family features (see Table 1 and Table 2). Updated pin diagrams to include new devices (see Pin Diagrams).
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Updated these sections: **2.2 "Decoupling Capacitors"**, **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**, **2.4 "Master Clear (MCLR) Pin"**, **2.8.1 "Crystal Oscillator Design Consideration"**
4.0 "Memory Organization"	Added Memory Map for new devices (see Figure 4-6).
14.0 "Watchdog Timer (WDT)"	New chapter created from content previously located in the Special Features chapter.
30.0 "Electrical Characteristics"	Removed parameter D312 (TSET) from the Comparator Specifications (see Table 30-12). Added the Comparator Voltage Reference Specifications (see Table 30-13). Updated Table 30-12.

Revision H (July 2015)

This revision includes the following major changes as described in Table A-7, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-7: MAJOR SECTION UPDATES

Section	Update Description
2.0 "Guidelines for Getting Started with 32-bit MCUs"	**Section 2.9 "Sosc Design Recommendation"** was removed.
8.0 "Oscillator Configuration"	The Primary Oscillator (POSC) logic in the Oscillator diagram was updated (see Figure 8-1).
30.0 "Electrical Characteristics"	The Power-Down Current (IPD) DC Characteristics parameter DC40k was updated (see Table 30-7). **Table 30-9: "DC Characteristics: I/O Pin Input Injection current Specifications"** was added.