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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256dt-v-tl">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f256dt-v-tl</a>

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 2: PIC32MX2XX 28/36/44-PIN USB FAMILY FEATURES**

Device	Pins	Program Memory (KB) <sup>(1)</sup>	Data Memory (KB)	Remappable Peripherals					Analog Comparators	USB On-The-Go (OTG)	I <sup>2</sup> C	PMP	DMA Channels (Programmable/Dedicated)	CTMU	10-bit 1 Msps ADC (Channels)	RTCC	I/O Pins	JTAG	Packages
				Remappable Pins	Timers <sup>(2)</sup> /Capture/Compare	UART	SPI <sup>(3)</sup> /S	External Interrupts <sup>(3)</sup>											
PIC32MX210F016B	28	16+3	4	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX210F016C	36	16+3	4	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	25	Y	VTLA
PIC32MX210F016D	44	16+3	4	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX220F032B	28	32+3	8	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX220F032C	36	32+3	8	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX220F032D	44	32+3	8	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX230F064B	28	64+3	16	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX230F064C	36	64+3	16	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX230F064D	44	64+3	16	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX250F128B	28	128+3	32	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX250F128C	36	128+3	32	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX250F128D	44	128+3	32	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX230F256B	28	256+3	16	20	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX230F256D	44	256+3	16	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX270F256B	28	256+3	64	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX270F256D	44	256+3	64	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX270F256DB <sup>(4)</sup>	44	256+3	64	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN

**Note 1:** This device features 3 KB of boot Flash memory.

**2:** Four out of five timers are remappable.

**3:** Four out of five external interrupts are remappable.

**4:** This PIC32 device is targeted to specific audio software packages that are tracked for licensing royalty purposes. All peripherals and electrical characteristics are identical to their corresponding base part numbers.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number <sup>(1)</sup>				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
USBID	11 <sup>(3)</sup>	14 <sup>(3)</sup>	15 <sup>(3)</sup>	41 <sup>(3)</sup>	I	ST	USB OTG ID detect
CTED1	27	2	33	19	I	ST	CTMU External Edge Input
CTED2	28	3	34	20	I	ST	
CTED3	13	16	17	43	I	ST	
CTED4	15	18	19	1	I	ST	
CTED5	22	25	28	14	I	ST	
CTED6	23	26	29	15	I	ST	
CTED7	—	—	20	5	I	ST	
CTED8	—	—	—	13	I	ST	
CTED9	9	12	10	34	I	ST	
CTED10	14	17	18	44	I	ST	
CTED11	18	21	24	8	I	ST	
CTED12	2	5	36	22	I	ST	
CTED13	3	6	1	23	I	ST	
CTPLS	21	24	27	11	O	—	CTMU Pulse Output
PGED1	1	4	35	21	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	2	5	36	22	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	18	21	24	8	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	19	22	25	9	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
PGED3	11 <sup>(2)</sup>	14 <sup>(2)</sup>	15 <sup>(2)</sup>	41 <sup>(2)</sup>	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3
	27 <sup>(3)</sup>	2 <sup>(3)</sup>	33 <sup>(3)</sup>	19 <sup>(3)</sup>			
PGEC3	12 <sup>(2)</sup>	15 <sup>(2)</sup>	16 <sup>(2)</sup>	42 <sup>(2)</sup>	I	ST	Clock input pin for Programming/Debugging Communication Channel 3
	28 <sup>(3)</sup>	3 <sup>(3)</sup>	34 <sup>(3)</sup>	20 <sup>(3)</sup>			
PGED4	—	—	3	12	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 4
PGEC4	—	—	4	13	I	ST	Clock input pin for Programming/Debugging Communication Channel 4

**Legend:** CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels  
TTL = TTL input buffer

Analog = Analog input  
O = Output  
PPS = Peripheral Pin Select

P = Power  
I = Input  
— = N/A

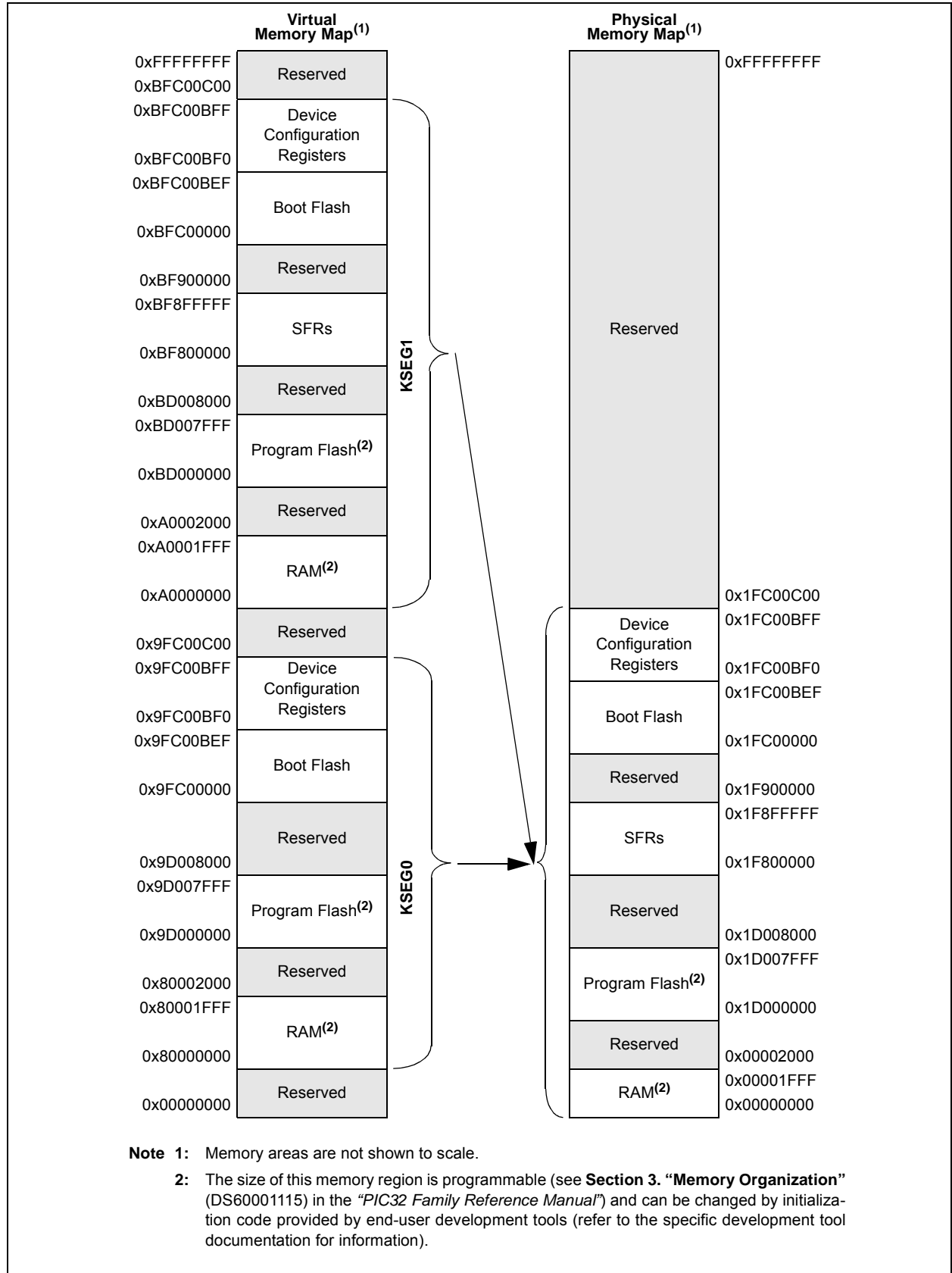
**Note 1:** Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

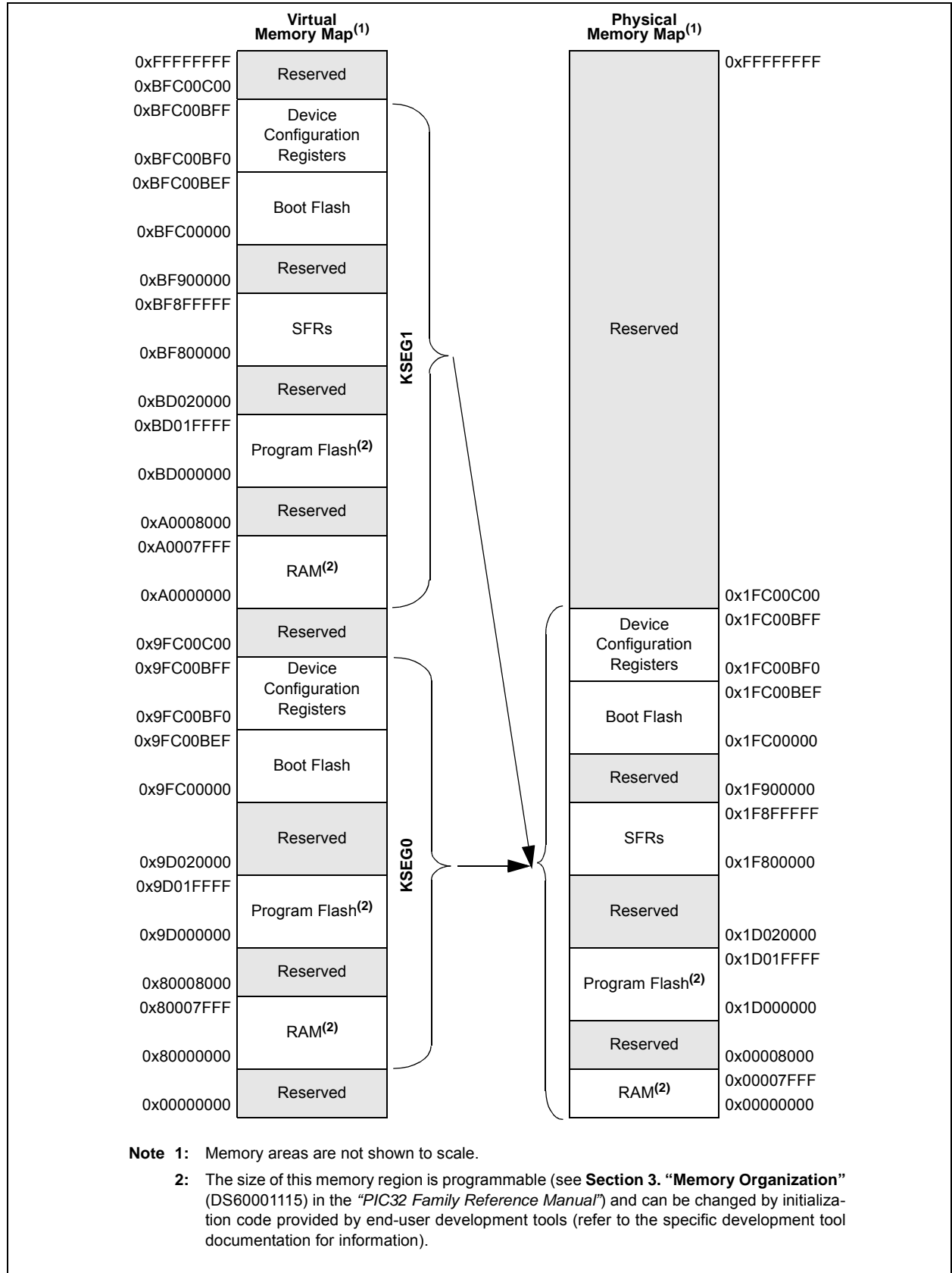
# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX120/220 DEVICES (8 KB RAM, 32 KB FLASH)**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX150/250 DEVICES (32 KB RAM, 128 KB FLASH)**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	R/W-1 BMX ERRIXI	R/W-1 BMX ERRICD	R/W-1 BMX ERRDMA	R/W-1 BMX ERRDS	R/W-1 BMX ERRIS
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	U-0 —	R/W-1 BMX WSDRM	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-1
BMXARB<2:0>								

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **BMXERRIXI:** Enable Bus Error from IXI bit

1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus

0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus

bit 19 **BMXERRICD:** Enable Bus Error from ICD Debug Unit bit

1 = Enable bus error exceptions for unmapped address accesses initiated from ICD

0 = Disable bus error exceptions for unmapped address accesses initiated from ICD

bit 18 **BMXERRDMA:** Bus Error from DMA bit

1 = Enable bus error exceptions for unmapped address accesses initiated from DMA

0 = Disable bus error exceptions for unmapped address accesses initiated from DMA

bit 17 **BMXERRDS:** Bus Error from CPU Data Access bit (disabled in Debug mode)

1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access

0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access

bit 16 **BMXERRIS:** Bus Error from CPU Instruction Access bit (disabled in Debug mode)

1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access

0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **BMXWSDRM:** CPU Instruction or Data Access from Data RAM Wait State bit

1 = Data RAM accesses from CPU have one wait state for address setup

0 = Data RAM accesses from CPU have zero wait states for address setup

bit 5-3 **Unimplemented:** Read as '0'

bit 2-0 **BMXARB<2:0>:** Bus Matrix Arbitration Mode bits

111 = Reserved (using these Configuration modes will produce undefined behavior)

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.

.

011 = Reserved (using these Configuration modes will produce undefined behavior)

010 = Arbitration Mode 2

001 = Arbitration Mode 1 (default)

000 = Arbitration Mode 0

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST <sup>(1)</sup>

### Legend:

HC = Cleared by hardware

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit<sup>(1)</sup>

1 = Enable Software Reset event

0 = No effect

**Note 1:** The system unlock sequence must be performed before the SWRST bit is written. Refer to **Section 6. "Oscillator"** (DS60001168J) in the *"PIC32 Family Reference Manual"* for details.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 9-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0> <sup>(1)</sup>							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0> <sup>(1)</sup>							
7:0	S-0 CFORCE	S-0 CABORT	R/W-0 PATEN	R/W-0 SIRQEN	R/W-0 AIRQEN	U-0 —	U-0 —	U-0 —

<b>Legend:</b>	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>**: Channel Transfer Abort IRQ bits<sup>(1)</sup>

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•  
•  
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>**: Channel Transfer Start IRQ bits<sup>(1)</sup>

11111111 = Interrupt 255 will initiate a DMA transfer

•  
•  
•

00000001 = Interrupt 1 will initiate a DMA transfer

00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE**: DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 **CABORT**: DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 **PATEN**: Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 **SIRQEN**: Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN**: Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.



# 16.1 Output Compare Control Registers

TABLE 16-1: OUTPUT COMPARE 1-OUTPUT COMPARE 5 REGISTER MAP

Virtual Address (BF80_#)	Register Name(r)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
3020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
3200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
3220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
3400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
3420	OC3RS	31:16 15:0	OC3RS<31:0>																xxxx xxxx
3600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
3620	OC4RS	31:16 15:0	OC4RS<31:0>																xxxx xxxx
3800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
3820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 FRMEN	R/W-0 FRMSYNC	R/W-0 FRMPOL	R/W-0 MSSEN	R/W-0 FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0 MCLKSEL <sup>(2)</sup>	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 SPIFE	R/W-0 ENHBUF <sup>(2)</sup>
15:8	R/W-0 ON <sup>(1)</sup>	U-0 —	R/W-0 SIDL	R/W-0 DISSDO	R/W-0 MODE32	R/W-0 MODE16	R/W-0 SMP	R/W-0 CKE <sup>(3)</sup>
7:0	R/W-0 SSEN	R/W-0 CKP <sup>(4)</sup>	R/W-0 MSTEN	R/W-0 DISSDI	STXISEL<1:0>		SRXISEL<1:0>	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **FRMEN:** Framed SPI Support bit  
1 = Framed SPI support is enabled ( $\overline{SSx}$  pin used as FSYNC input/output)  
0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on  $\overline{SSx}$  pin bit (Framed SPI mode only)  
1 = Frame sync pulse input (Slave mode)  
0 = Frame sync pulse output (Master mode)
- bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)  
1 = Frame pulse is active-high  
0 = Frame pulse is active-low
- bit 28 **MSSEN:** Master Mode Slave Select Enable bit  
1 = Slave select SPI support enabled. The  $\overline{SS}$  pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.  
0 = Slave select SPI support is disabled.
- bit 27 **FRMSYPW:** Frame Sync Pulse Width bit  
1 = Frame sync pulse is one character wide  
0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in FRAMED\_SYNC mode.  
111 = Reserved; do not use  
110 = Reserved; do not use  
101 = Generate a frame sync pulse on every 32 data characters  
100 = Generate a frame sync pulse on every 16 data characters  
011 = Generate a frame sync pulse on every 8 data characters  
010 = Generate a frame sync pulse on every 4 data characters  
001 = Generate a frame sync pulse on every 2 data characters  
000 = Generate a frame sync pulse on every data character
- bit 23 **MCLKSEL:** Master Clock Enable bit<sup>(2)</sup>  
1 = REFCLK is used by the Baud Rate Generator  
0 = PBCLK is used by the Baud Rate Generator
- bit 22-18 **Unimplemented:** Read as '0'

- Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLOCK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit can only be written when the ON bit = 0.
- 3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 18-1: I2CxCON: I<sup>2</sup>C CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON <sup>(1)</sup>	U-0 —	R/W-0 SIDL	R/W-1, HC SCLREL	R/W-0 STRICT	R/W-0 A10M	R/W-0 DISSLW	R/W-0 SMEN
7:0	R/W-0 GCEN	R/W-0 STREN	R/W-0 ACKDT	R/W-0, HC ACKEN	R/W-0, HC RCEN	R/W-0, HC PEN	R/W-0, HC RSEN	R/W-0, HC SEN

<b>Legend:</b>	HC = Cleared in Hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** I<sup>2</sup>C Enable bit<sup>(1)</sup>

- 1 = Enables the I<sup>2</sup>C module and configures the SDA and SCL pins as serial port pins
- 0 = Disables the I<sup>2</sup>C module; all I<sup>2</sup>C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I<sup>2</sup>C slave)

- 1 = Release SCLx clock
- 0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:

Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I<sup>2</sup>C Reserved Address Rule Enable bit

- 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
- 0 = Strict I<sup>2</sup>C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Slave Address bit

- 1 = I2CxADD is a 10-bit slave address
- 0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit

- 1 = Slew rate control disabled
- 0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit

- 1 = Enable I/O pin thresholds compliant with SMBus specification
- 0 = Disable SMBus input thresholds

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

- bit 4      **Unimplemented:** Read as '0'
- bit 3      **CS1P:** Chip Select 0 Polarity bit<sup>(2)</sup>  
1 = Active-high ( $\overline{\text{PMCS1}}$ )  
0 = Active-low ( $\text{PMCS1}$ )
- bit 2      **Unimplemented:** Read as '0'
- bit 1      **WRSP:** Write Strobe Polarity bit  
For Slave Modes and Master mode 2 ( $\text{MODE}<1:0> = 00,01,10$ ):  
1 = Write strobe active-high ( $\overline{\text{PMWR}}$ )  
0 = Write strobe active-low ( $\text{PMWR}$ )  
For Master mode 1 ( $\text{MODE}<1:0> = 11$ ):  
1 = Enable strobe active-high ( $\overline{\text{PMENB}}$ )  
0 = Enable strobe active-low ( $\text{PMENB}$ )
- bit 0      **RDSP:** Read Strobe Polarity bit  
For Slave modes and Master mode 2 ( $\text{MODE}<1:0> = 00,01,10$ ):  
1 = Read Strobe active-high ( $\overline{\text{PMRD}}$ )  
0 = Read Strobe active-low ( $\text{PMRD}$ )  
For Master mode 1 ( $\text{MODE}<1:0> = 11$ ):  
1 = Read/write strobe active-high ( $\overline{\text{PMRD/PMWR}}$ )  
0 = Read/write strobe active-low ( $\text{PMRD/PMWR}$ )

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

**2:** These bits have no effect when their corresponding pins are used as address lines.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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NOTES:

## 26.0 POWER-SAVING FEATURES

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. “Power-Saving Features”** (DS60001130), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

This section describes power-saving features for the PIC32MX1XX/2XX 28/36/44-pin Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

### 26.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- Sosc Run mode: the CPU is clocked from the Sosc clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

### 26.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- Posc Idle mode: the system clock is derived from the Posc. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- Sosc Idle mode: the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.

- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

## 26.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

### 26.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See **Section 26.3.3 “Peripheral Bus Scaling Method”** for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## 29.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

## 29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

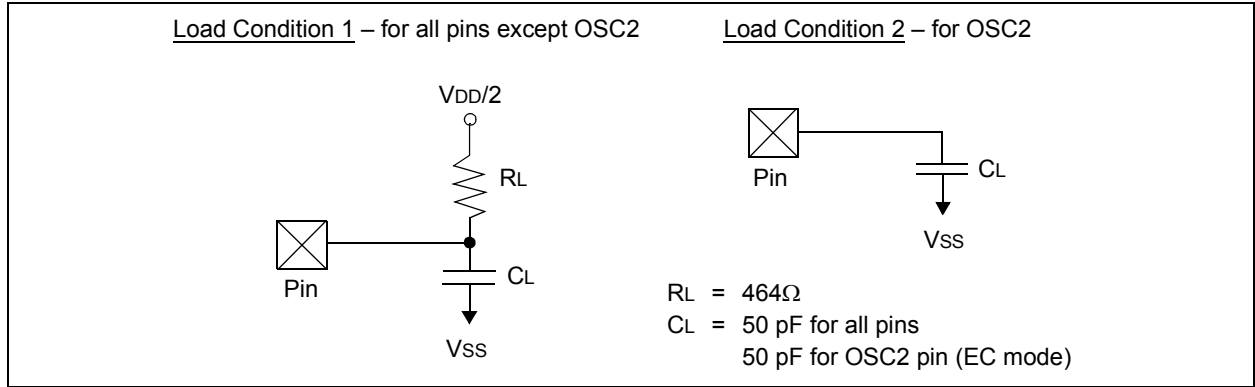
- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 30.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX 28/36/44-pin Family AC characteristics and timing parameters.

**FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

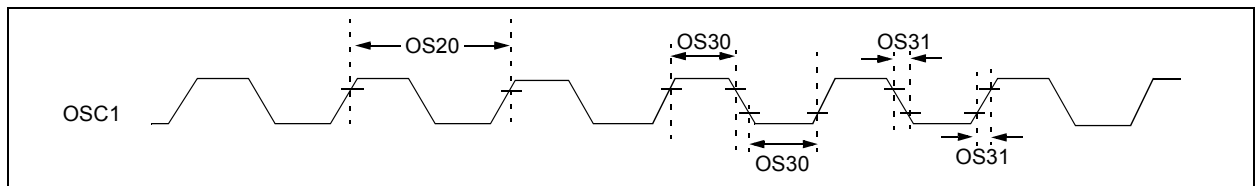


**TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for Industrial $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
DO56	C <sub>IO</sub>	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	C <sub>B</sub>	SCLx, SDAx	—	—	400	pF	In I <sup>2</sup> C mode

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

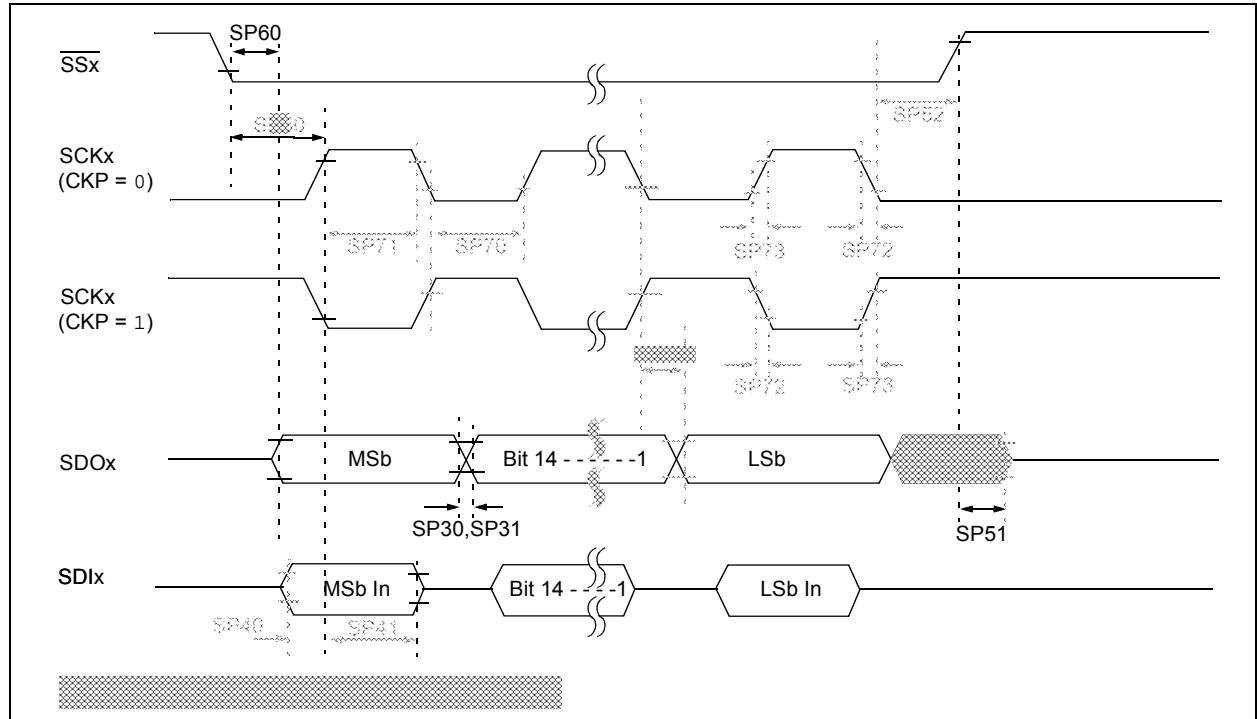
**FIGURE 30-2: EXTERNAL CLOCK TIMING**





# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**FIGURE 30-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**



**TABLE 30-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical <sup>(2)</sup>	Max.	Units	Conditions
SP70	TsCL	SCKx Input Low Time ( <b>Note 3</b> )	TsCK/2	—	—	ns	—
SP71	TsCH	SCKx Input High Time ( <b>Note 3</b> )	TsCK/2	—	—	ns	—
SP72	TsCF	SCKx Input Fall Time	—	5	10	ns	—
SP73	TsCR	SCKx Input Rise Time	—	5	10	ns	—
SP30	TDoF	SDOx Data Output Fall Time ( <b>Note 4</b> )	—	—	—	ns	See parameter DO32
SP31	TDoR	SDOx Data Output Rise Time ( <b>Note 4</b> )	—	—	—	ns	See parameter DO31
SP35	TsCH2DoV, TsCL2DoV	SDOx Data Output Valid after SCKx Edge	—	—	20	ns	VDD > 2.7V
			—	—	30	ns	VDD < 2.7V
SP40	TdIV2sCH, TdIV2sCL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TsCH2dIL, TsCL2dIL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	TssL2sCH, TssL2sCL	SSx ↓ to SCKx ↓ or SCKx ↑ Input	175	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 33.1 Package Marking Information (Continued)

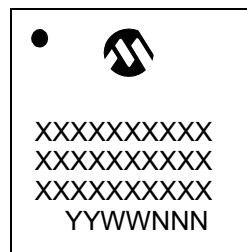
36-Lead VTLA



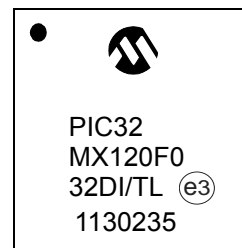
Example



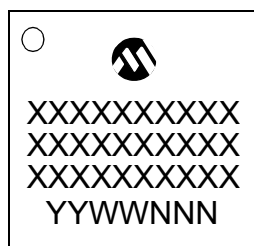
44-Lead VTLA



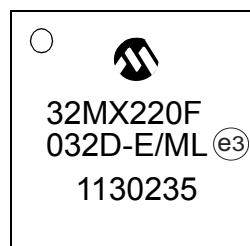
Example



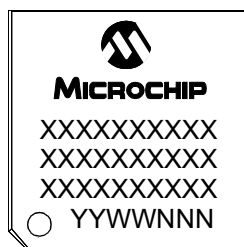
44-Lead QFN



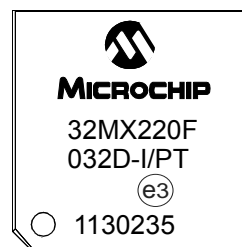
Example



44-Lead TQFP



Example

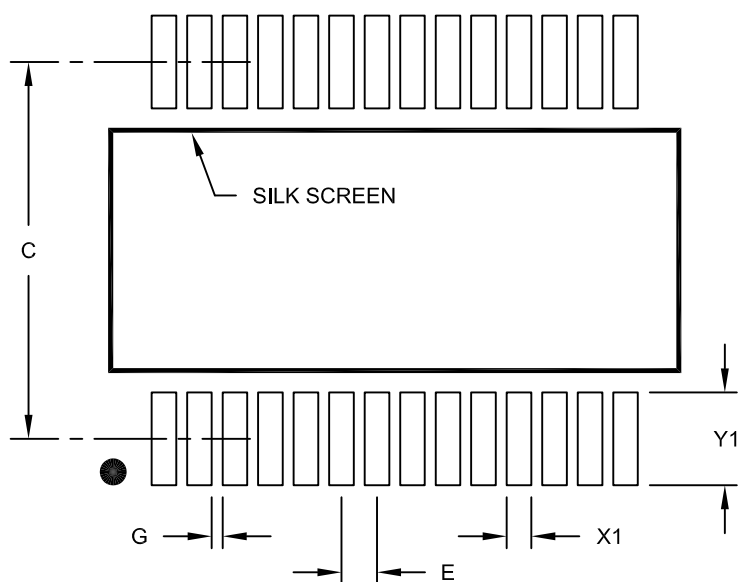


<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	<sup>(e3)</sup>	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( <sup>(e3)</sup> ) can be found on the outer packaging for this package.
<b>Note:</b> If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.		

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## APPENDIX A: REVISION HISTORY

### Revision A (May 2011)

This is the initial released version of this document.

### Revision B (October 2011)

The following two global changes are included in this revision:

- All packaging references to VLAP have been changed to VTLA throughout the document
- All references to VCORE have been removed
- All occurrences of the ASCL1, ASCL2, ASDA1, and ASDA2 pins have been removed
- V-temp temperature range (-40°C to +105°C) was added to all electrical specification tables

This revision includes the addition of the following devices:

- PIC32MX130F064B
- PIC32MX130F064C
- PIC32MX130F064D
- PIC32MX150F128B
- PIC32MX150F128C
- PIC32MX150F128D
- PIC32MX230F064B
- PIC32MX230F064C
- PIC32MX230F064D
- PIC32MX250F128B
- PIC32MX250F128C
- PIC32MX250F128D

Text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-1.

**TABLE A-1: MAJOR SECTION UPDATES**

Section	Update Description
“32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog”	Split the existing Features table into two: PIC32MX1XX General Purpose Family Features (Table 1) and PIC32MX2XX USB Family Features (Table 2). Added the SPDIP package reference (see Table 1, Table 2, and “ <b>Pin Diagrams</b> ”). Added the new devices to the applicable pin diagrams. Changed PGED2 to PGED1 on pin 35 of the 36-pin VTLA diagram for PIC32MX220F032C, PIC32MX220F016C, PIC32MX230F064C, and PIC32MX250F128C devices.
<b>1.0 “Device Overview”</b>	Added the SPDIP package reference and updated the pin number for AN12 for 44-pin QFN devices in the Pinout I/O Descriptions (see Table 1-1). Added the PGEC4/PGED4 pin pair and updated the C1INA-C1IND and C2INA-C2IND pin numbers for 28-pin SSOP/SPDIP/SOIC devices in the Pinout I/O Descriptions (see Table 1-1).
<b>2.0 “Guidelines for Getting Started with 32-bit Microcontrollers”</b>	Updated the Recommended Minimum Connection diagram (see Figure 2-1).

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## Revision J (April 2016)

This revision includes the following major changes as described in Table A-8, as well as minor updates to text and formatting, which were incorporated throughout the document.

**TABLE A-8: MAJOR SECTION UPDATES**

Section	Update Description
<b>“32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog”</b>	The PIC32MX270FDB device and Note 4 were added to <b>TABLE 2: “PIC32MX2XX 28/36/44-pin USB Family Features”</b> .
<b>2.0 “Guidelines for Getting Started with 32-bit MCUs”</b>	<b>EXAMPLE 2-1: “Crystal Load Capacitor Calculation”</b> was updated.
<b>30.0 “Electrical Characteristics”</b>	Parameter DO50a (Csosc) was removed from the Capacitive Loading Requirements on Output Pins AC Characteristics (see Table 30-16).
<b>“Product Identification System”</b>	The device mapping was updated to include type B for Software Targeting.